LOW POWER ECRL BASED ADIABATIC LOGIC FOR POWER RECYCLER

PENUBOLU VIJAY KUMAR N.A.S VIJAYA VARMA P.RANA PRAMODH
S.MAHABOOB BASHA

R.M.K ENGINEERING COLLEGE

ABSTRACT

The relevance of VLSI in performance of the various sectors like computing, telecommunication, consumer electronics has been expanding progressively, and at a very hasty pace. Power minimization has become primary trouble in VLSI design. Several techniques are used to control the dynamic and leakage power in the circuits. ECRL technique is used to improve the energy recycling and validated with a benchmark circuit. The energy dissipation will be reduced when the increase in the circuit implemented. Positive feedback adiabatic logic is used to recover the output nodal capacitances and these can be used to drive the circuit operation. In these, we are using efficient charge recovery logic(ECRL) which is used to improve the energy recycling compared with the existing method. This ECRL method is validated with a benchmark circuit.

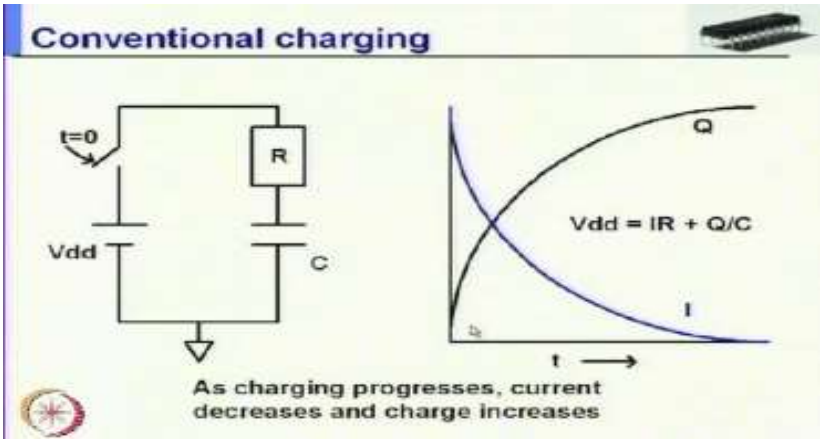
INTRODUCTION

Adiabatic CMOS and here is the agenda of today's lecture, after giving a brief introduction, I shall discuss the basic differences between conventional and adiabatic charging. Then, we shall see how we can do adiabatic amplification and then, we shall discuss about realization of adiabatic logic circuits and after that, we shall have brief discussion on pulsed power supply, which will be required in implementing adiabatic logic circuits. Then, we shall discuss partially adiabatic circuits to reduce the cost of implementation, fully adiabatic circuit. Then, we shall conclude the lecture with some comments. They are known as, as you know static CMOS circuits, static CMOS circuits and in static CMOS circuits we have seen that, there is a voltage swing between V dd and ground. So, there is a rail to rail voltage swing and as we know the basic implementation, which is being done with the help of 1 pmos and 1 nmos logics block. So, we have got this is the pmos and this is the nmos and output is taken from here, input is given here.There is a rail to rail voltage swing and as we know the basic implementation, which is being done with the help of 1 pmos and 1 nmos logics block. So, we have got this is the pmos and this is the nmos and output is taken from here, input is given here That means and that can be done by using a technique known as adiabatic technique. This term adiabatic, has been taken from thermodynamic processes, as you know adiabatic systems do not release energy to the environment or do not take energy from the environment. These are the typical characteristic of adiabatic systems; that means, no energy is transferred from the system to the environment.

CONVENTIONAL CHARGING

The power dissipation switching power, that may dissipation cannot be lowered than, this one by using this conventional static CMOS circuits. Now, is there any way we can do it. The other alternative is adiabatic switching circuits, where the switching power dissipation is below this lower limit; that means, we shall be doing the switching in such a way, that the energy dissipation; that means, energy loss per transition will be lower. That means and that can be done by using a technique known as adiabatic technique. This term adiabatic, has been taken from thermodynamic processes, as you know adiabatic systems do not release energy to the environment or d0

not take energy from the environment. These are the typical characteristic of adiabatic systems; that means, no energy is transferred from the system to the environment. So here also, that is the basic objective, but how far that goal is successful that, we shall see but this term has been taken adiabatic term, has been taken from this thermodynamic process that exchange no heat with the environment.



ADIABATIC CHARGING

This capacitor is typically the load capacitance or it can be any capacitance, this capacitance has to be charged simplest circuit by which you can do it is that, suppose this is your a power source V dd and you can put a a switch and then you can put a resistor and as you close the switch close switch, at t is t is equal to 0, t is equal to 0 then what will happen? this capacitor if, there is no charge initially initially at t is equal to 0, the charge in this capacitor is zero then, it will start charging and as we know in in case of whenever you are charging through a resistor, this is your R and this is your c or c l. Whatever it may be, we know that the initially the current will be current, will be maximum because the voltage across the capacitor is zero. So, the entire voltage will be developed developed across this resistor. So, if this is the voltage V dd.

SOFTWARE DESCRIPTION

Digital VLSI circuits are predominantly CMOS based. The way normal blocks like latches and gates are implemented is different from what students have seen so far, but the behavior remains the same. All the miniaturization involves new things to consider. A lot of thought has to go into actual implementations as well as design. Let us look at some of the factors. Circuit Delays: Large complicated circuits running at very high frequencies have one big proble tackle - the problem of delays in propagation of signals through gates and wires ... even for areas a few micrometers across! The operation speed is so large that as the delays add up. Another effect of high operation frequencies is increased consumption of power. This has two-fold effect - devices consume batteries faster, and heat dissipation increases. Coupled with the fact that surface areas have decreased, heat poses a major.The power dissipation and speed in a circuit present a trade-off; if we try to optimize on one, the other is affected. The choice between the two is determined by the way we chose the layout the circuit components. Layout can also affect the fabrication of VLSI chips, making it either easy or difficult to implement the components on the silicon.

VLSI BASICS

The first semiconductor chips held two transistors each. Subsequent advances added more and more transistors, and, as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistors into a single chip.

VERILOG:

Verilog standardized as IEEE 1364, is a hardware description language (HDL) used to model electronic systems. It is most commonly used in the design and verification of digital circuits at the register-transfer level of

abstraction. It is also used in the verification of analog circuits and mixed-signal circuits. Hardware description languages such as Verilog differ from software programming languages because they include ways of describing the propagation of time and signal dependencies (sensitivity). At the time of Verilog's introduction (1984),Verilog represented a tremendous productivity improvement for circuit designers who were already using graphical schematic capture software and specially written software programs to document and simulate electronic circuits.

Xilinx software:

It is an American technology company, primarily a supplier of programmable logic devices. It is known for inventing the field programmable gate array (FPGA) and as the first semiconductor company with a fabless manufacturing model. Founded in Silicon Valley in 1984.

Xilinx designs, develops and markets programmable logic products, including integrated circuits (ICs), software design tools, predefined system functions delivered as intellectual property (IP) cores, introduced new high capacity 3D FPGAs, including Virtex-7 2000T and Virtex-7 H580T products, these devices began to outpace the capacity of Xilinx's design software, which led the company to completely redesign its tool set.

DESIGN METHODOLOGY:

Adiabatic logic design is the most frequently used methods for the design of ultra-low power hardware of optimal performance applications. These circuits recover a major part of the energy stored in the output nodal capacitances which can be reused for the successive computations. In the existing design the Positive Feedback Symmetric Adiabatic Logic (PFSAL) which reduces the energy dissipated by the S-Box circuit used in the cryptographic designs. The PFSAL is validated by the design of the PFSAL based Rijndael S-Box.. The existing system and proposed system power relations will be compared and tabulated.

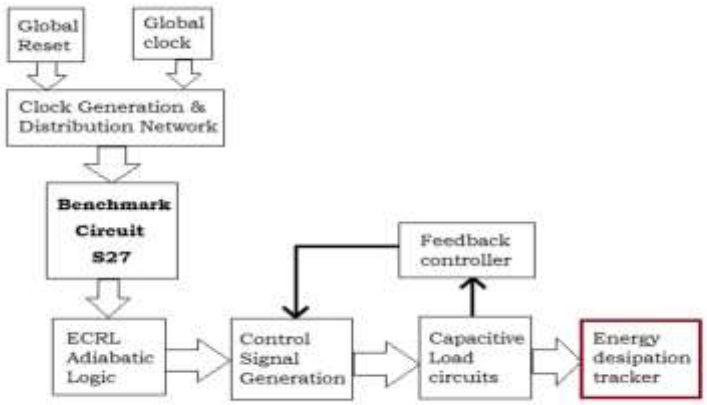
EXISTING SYSTEM:

In the existing design the Positive Feedback Symmetric Adiabatic Logic (PFSAL) which reduces the energy dissipated by the S-Box circuit used in the cryptographic designs. Proposed PFSAL is validated by the design of the PFSAL based Rijndael S-Box. The efficiency of the existing design is validated by comparing it with Rijndael S-Box designed**.**

PROPOSED SYSTEM:

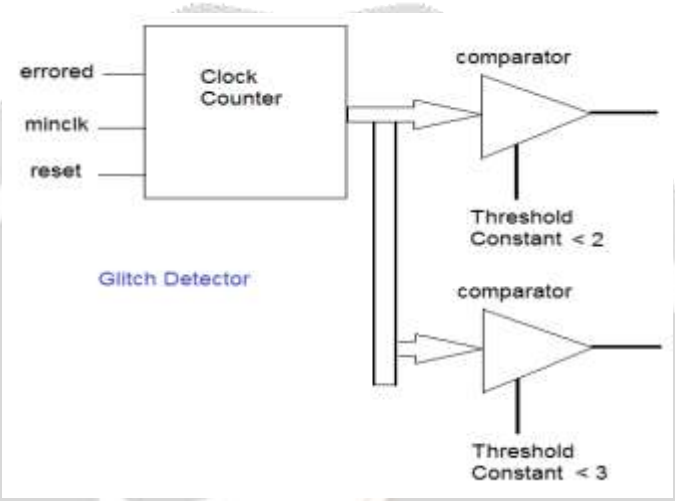
In the proposed system, Efficient charge Recovery logic ECRL adiabatic Logic is used to improve the energy recycling capacity compare with the existing method. The proposed method is also validated with Benchmark circuit. The existing system and proposed system power relations will be compared and tabulated.

BLOCK DIAGRAM:



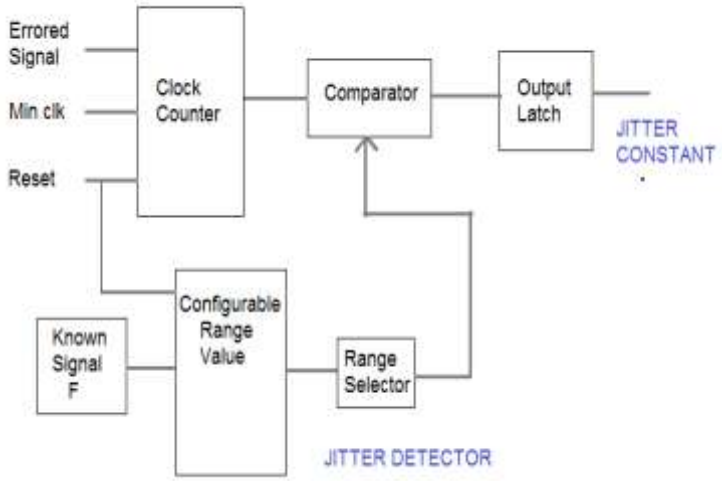
GLITCH DETECTOR:

An electronics glitch or hazard is a transition that occurs on a signal before the signal settles to its intended value, particularly in a digital circuit. Generally this implies an electrical pulse of short duration, often due to a race condition between two signals derived from a common source but with different delays. In some cases, such as a well-timed synchronous circuit, this could be a harmless and well-tolerated effect that occurs normally in a design. In other contexts a glitch can represent an undesirable result of a fault or design error that can produce a malfunction. Some electronic components, such as flip-flops, are triggered by a pulse that must not be shorter than a specified minimum duration in order to function correctly; a pulse shorter than the specified minimum may be called a glitch. A related concept is the runt pulse, a pulse whose amplitude is smaller than the minimum level specified for correct operation, and a spike, a short pulse similar to a glitch but often caused by ringing or crosstalk. other contexts a glitch can represent an undesirable result of a fault or design error that can produce a malfunction. Some electronic components, such as flip-flops, are triggered by a pulse that must not be shorter than a specified minimum duration in order to function correctly.



JITTER DETECTOR:

In electronics and telecommunications, jitter is the deviation from true periodicity of a presumably periodic signal, often in relation to a reference clock signal. In clock recovery applications it is called timing jitter. Jitter is a significant, and usually undesired, factor in the design of almost all communications links. Jitter can be quantified in the same terms as all time-varying signals, e.g., root mean square (RMS), or peak-to-peak displacement. Also like other time-varying signals, jitter can be expressed in terms of spectral density. Jitter period is the interval between two times of maximum effect (or minimum effect) of a signal characteristic that varies regularly with time. Jitter frequency, the more commonly quoted figure, is its inverse. ITU-T G.810 classifies jitter frequencies below 10 Hz as wander and frequencies at or above 10 Hz. Jitter may be caused by electromagnetic interference and crosstalk with carriers of other signals. Jitter can cause a display monitor to flicker, affect the performance of processors in personal computer introduce clicks or other undesired effects in audio signals, and cause loss of transmitted data between network devices. The amount of tolerable jitter depends on the affected application. Jitter can be quantified in the same terms as all time-varying signals, e.g., root mean square (RMS), or peak-to-peak displacement. Also like other time-varying signals, jitter can be expressed in terms of spectral density. Jitter period is the interval between two times of maximum effect (or minimum effect) of a signal characteristic that varies regularly with time. Jitter frequency, the more commonly quoted figure, is its inverse. Also like other time-varying signals, jitter can be expressed in terms of spectral density. Jitter period is the interval between two times of maximum effect (or minimum effect) of a signal characteristic that varies regularly with time. Jitter frequency, the more commonly quoted figure, is its inverse.



MODULE DESCRIPTION:

Module 1: Design of Benchmark

This module consists of one standard benchmark circuit used to test the proposed model. The benchmark circuit is a standard which determines the number of flip flops to be used in the circuit Number of combinational circuits to be enclosed etc. Applying a benchmark circuit enable the test and evaluation even more standard.

MODULE 2:DESIGN OF CAPACITIVE STORAGE MODEL

This module consists of a capacitive storage module to get charged and discharged at every peak rise of the error signal which is nothing but the signal which will generate more energy dissipation.

MODULE 3:DESIGN OF ADIABATIC SAVING MODULE

This module consists of ECRL adiabatic logic, to enable the power saving mode of the design under test. The energy dissipated will be a minimum value, but a large accumulation of energy will dissipate an accountable energy. The proposed algorithm save the minute energy and recycle the energy into a useful level of voltage to trigger other circuits**.**

CONCLUSION:

In this paper, a novel Positive feedback symmetric adiabatic logic (PFSAL) is proposed, which consumes very less energy when compared with the existing security based adiabatic logic circuits. PFSAL has an improvement of about 80.9%, 96%, 95% and 65% when compared with the SAL,CSSAL, SQAL and SAL Circuits. Also, PFSAL reduces the transistor count when compared with SAL and CSSAL. The performance of processors in personal computer introduce clicks or other undesired effects in audio signals, and cause loss of transmitted data between network devices. The amount of tolerable jitter depends on the affected application.

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