MULTIPLE CELL UPSET TOLERANT ERROR DETECTION AND CORRECTION CODE FOR SEMICONDUCTOR MEMORIES USING DSSC

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ABSTRACT

The presented project presents the implementation and evaluation of the Data Segmentation Section Code (DSSC), a new algorithm for the detection and correction of multiple transient faults in volatile memories with low cost implementation. DSSC is an ECC based on two-dimensional (2D) codes, that aims to correct and detect MCUs in memories The proposal in split the data bits in three regions was elaborated in order to select a specific group of bit to operate the correction process. By calculating parity and diagonal check bits and syndrome bits the errors are detected and corrected region wise .This approach reduces considerably the area and power cost. Our proposed system has been coded in Verilog HDL and simulated using Xilinx 12.1

Keyword : - *Data segmentation ,cell upsets, correction codes*

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1. INTRODUCTION

The progress in very large scale integration (VLSI) technologies improved dramatically the reliability of electronic components, restricting the use of fault tolerance in a very restrictive number of application domains. We recently reached a point where these trends are reversed. Drastic device shrinking, increased complexity, power supply reduction, and increasing operating speeds that accompany the technological evolution to nano metric technologies have reduced dramatically the reliability of deep submicron ICs.A significant problem related to soft errors induced on one hand by alpha particles produced by radioactive isotope traces found in packaging, bonding, and die materials and on the other hand by atmospheric neutrons created by the interaction of cosmic rays with the earth atmosphere. While alpha particles are electrically charged and create a track of electron hole pairs when they pass through an IC, neutrons are electrically neutral and create soft errors in an indirect manner: a high energy neutron may interact with a silicon, oxygen, or other atom of the chip to create electrically charged secondary particles able to induce soft errors. It is to noted that the interaction can create numerous secondary particles that could simultaneously affect several circuit nodes. The small size of the transistors or capacitors, combined with cosmic ray effects, causes occasional errors in stored information in large, dense RAM chips, particularly those that are dynamic. These errors can be detected and corrected by employing error-detecting and correcting codes in RAMs

2. EXISTING SYSTEM

Joaquin Gracia-Moran proposes an Improving Error Correction Codes for Multiple-Cell Upsets in Space Applications. Currently, faults suffered by SRAM memory systems have increased due to the aggressive CMOS integration density. Thus, the probability of occurrence of single-cell upsets (SCUs) or multiple-cell upsets (MCUs) augments. One of the main causes of MCUs in space applications is cosmic radiation. A common solution is the use

of error correction codes (ECCs). Nevertheless, when using ECCs in space applications, they must achieve a good balance between error coverage and redundancy, and their encoding/decoding circuits must be efficient in terms of area, power, and delay. Different codes have been proposed to tolerate MCUs. For instance, Matrix codes use Hamming codes and parity checks in a bi-dimensional layout to correct and detect some patterns of MCUs. Recently presented, column–line–code (CLC) has been designed to tolerate MCUs in space applications.

3. PROPOSED SYSTEM

The implementation and evaluation of the Data Segmentation Section Code (DSSC), a new algorithm for the detection and correction of multiple transient faults in volatile memories with low cost implementation. The experimental results measuring error coverage composed by detection and correction analysis, area, power and delay overheads have shown that DSSC is an excellent option to counteract with MCUs.DSSC is an ECC based on two-dimensional (2D) codes, that aims to correct and detect MCUs in memories.

3.1 Encoding And Decoding Process

The code presented in this paper codifies 16 data bits in 32 bits. However, only parity bits are used in encoding data bits to reduce the cost of implementation.Here the diagonal bits ,parity bits and the check bits are being calculated**.**After the calculation of the redundancy bits, the encoding process ends and the 32 bits can be stored. Note that the Di bits and Cb bits are positioned between the data bits and Cb bits, in order to improve the efficiency of DSSC against MCUs characterized by adjacent error patterns.

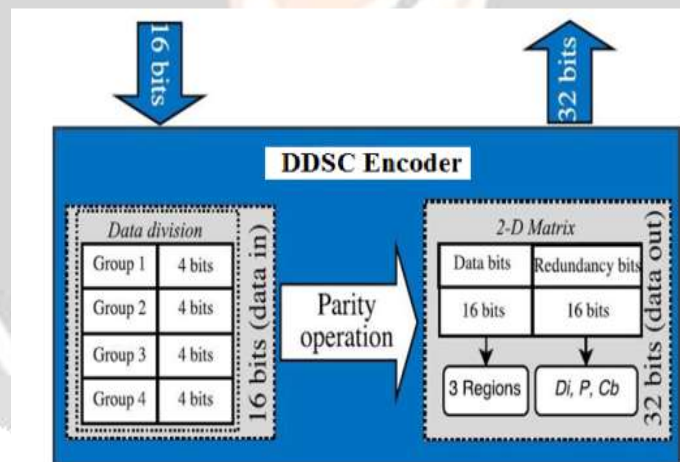

Fig -1 DSSC Encoder

The decoding process of DSSC is done by the syndrome estimation consists of a XOR operation between the redundancy data stored and the recalculated redundancy bits (RDi, RP, and RCb). Therefore, the values for the Syndrome of Diagonal (SDi), Parity (SP) and Check bits (SCb) are estimated.After the calculation of the Syndromes, one of these two conditions need to be satisfied before the error correction execution: (i) both SDi and SP vectors must have at least one value equal to one; (ii) more than one SCb value is equal to one. These conditions allow the algorithm to detect an error in the data bits region. Their applicability will be explained with more details subsequently.In this phase of the decoding process, a specific region of the data bits is selected to be corrected. . The proposal in split the data bits in three regions was elaborated in order to select a specific group of bit to operate the correction process. This approach reduces considerably the area and power cost.

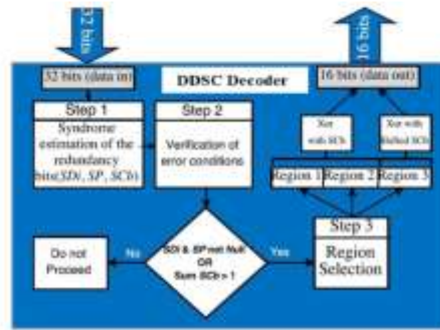

Fig -2 DSSC Decoder

3.2 Results and Analysis

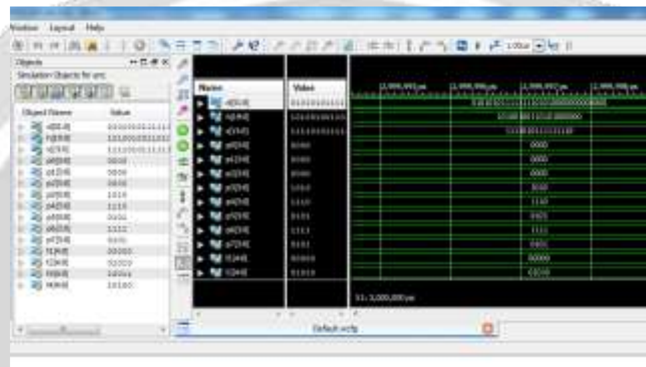

Fig-3 shows the output of the encoder

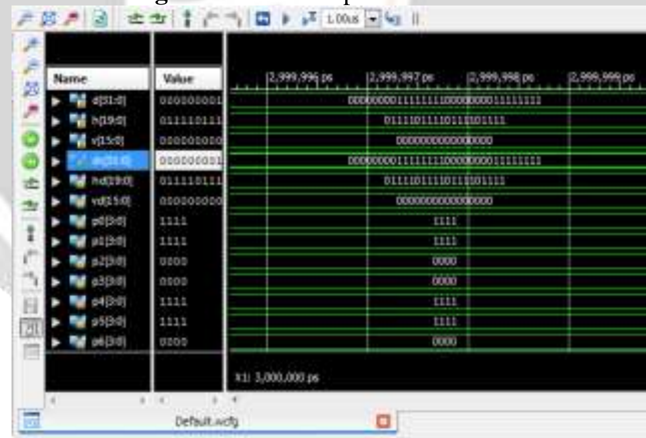

Fig-4 shows the output of the decoder

Fig-5 represents the synthesis analysis of the existing syste

Fig-6 represents the synthesis analysis of the proposed system

4. CONCLUSIONS

The proposed Data Segmentation Section Code (DSSC) an error detection/correction code for memory devices subjected to multiple cell upsets (MCUs). is based on parity codes and interleaving techniques to deal with several patterns of MCUs. DSSC is shown as the lowest cost code among all evaluated codes. The utilization of Hamming and Extended Hamming in the ECCs Matrix and CLC has brought advantages in error coverage. However, this also increased heavily the cost of both codes when compared with DSSC. Regarding the experimental results, DSSC presents the best results for all fault scenarios which means that DSSC has the better tradeoff between error coverage and implementation cost than all codes analyzed

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5. REFERENCES

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