Multilevel Inverter-Eleven level

Nitesh kumar Gopa

[1]*M.Tech Scholar, Department of Electrical Engineering, Aryabhatta college of Engineering & Research Centre, Ajmer, Rajasthan, India*

,

ABSTRACT

In this , the proposed Three-Phase eleven- level Inverter is being implemented by using Pulse width Modulation technique. Convectional inverter are omitted and multilevel inverters are used which will help in mitigation of harmonic level in the circuit and smooth operation of inverter is achieved , balancing capacitors are used to provide the required firing voltages, for controlling the multilevel inverter sinusoidal pulse width modulation technique is used in which sinusoidal wave form is compare with triangular wave

Keywords *- Multilevel inverter, different types of inverter, Renewable energy sources, multilevel inverter topologies, power converter*

INTRODUCTION

Inverter is an electrical power device which used to convert direct current into alternating current. It is also known as power inverter. Industrial application required high power appliance as well as its also required medium and low power. Inverter is electronic device through which power transmit to other electrical equipment such as UPS and servo motor, etc. at the different load output voltage and frequency is changed [1]- [3]. In industrial drive the amount of power equipment is increased. In the power system the harmonic pollution become dangerous [4]-[6].

High power applications are required to meet the industrial requirement and the voltage stress of the power device also affected. An IGBT is a switching device. IGBT is operates on low switching frequency and high power rating, high voltage stress. Gate driver of IGBT is complicated. MOSFET is a switching device which operates on high frequency and its power rating is not good. Several topology of multilevel inverter are used to overcome such problem. In the High-power application low rating component is used. Aim of this scheme is to minimize voltage rating of power switch. The advantages of multilevel inverter are low distortion of input current, low switching frequency and low $\frac{dv}{dt}$ [7], [8].in this dissertation a novel three-phase Eleven-level inverter is design and implement. The proposed topology is used to reduce power component Few most commonly used inverter types are:

Square wave inverters Modified sine wave inverters Multilevel inverters Pure sine wave inverters Resonant inverters Grid tie inverters Synchronous inverters Stand-alone inverters Solar inverters

CIRCUIT CONFIGURATION

Fig 4.1 shows a proposed novel-topology, which is used in eleven-level inverter. Four series capacitor C1, C2, C3 and C4 are comprised in an input voltage divider. From this divided voltage is fed to H-bridge by using four IGBT'S and five Diodes. Then H-bridge is used to fed this voltage to output terminal. Therefore, multilevel inverter gives an output in the form of Eleven-level ac output voltage.

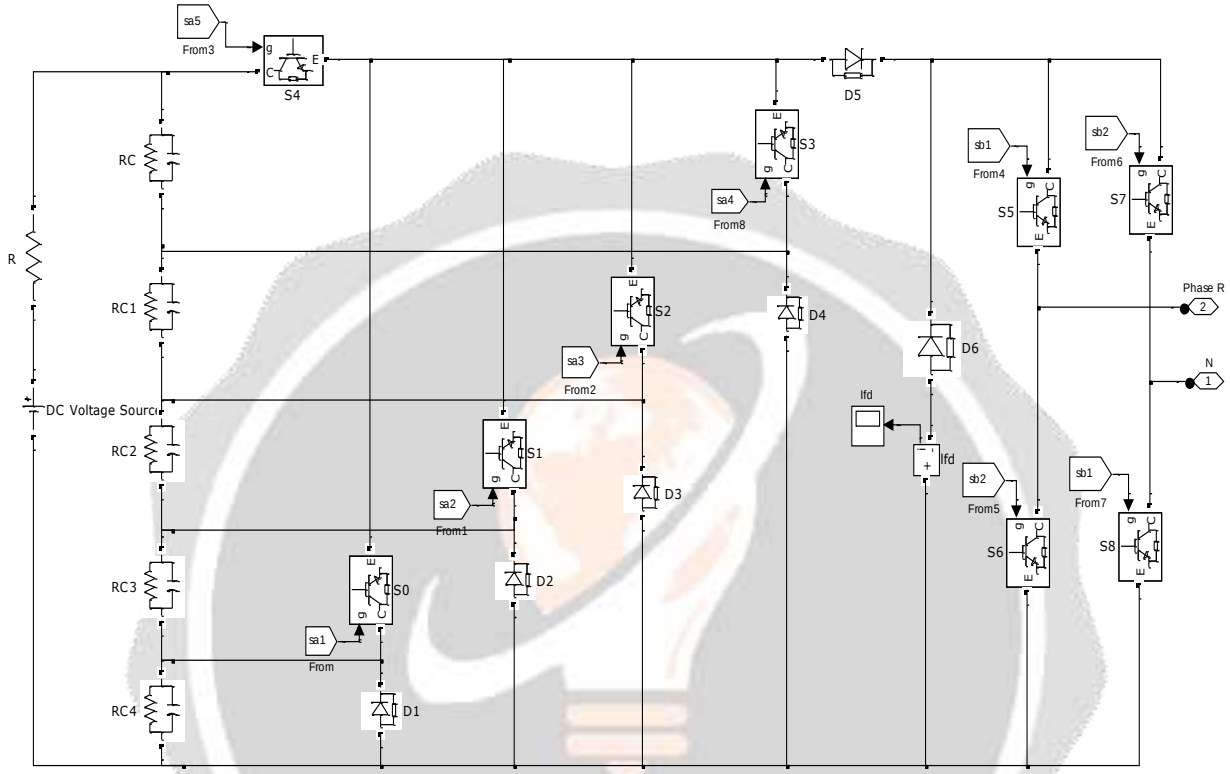


Fig 4.1 Proposed Eleven-level Inverter Topology

DIFFERENT SWITCHING OPERATION OF OUTPUT VOLTAGE LEVEL

Its generate 11-level output voltages are as follow: $(0, \pm\frac{1}{5}V_{dc}, \pm\frac{2}{5}V_{dc}, \pm\frac{3}{5}V_{dc}, \pm\frac{4}{5}V_{dc} \pm V_{dc})$.

1). Generate a voltage level $V_0 = 0$

Switches - S5, S7 and S8 are turned on.

Zero voltage is applied on load terminals.

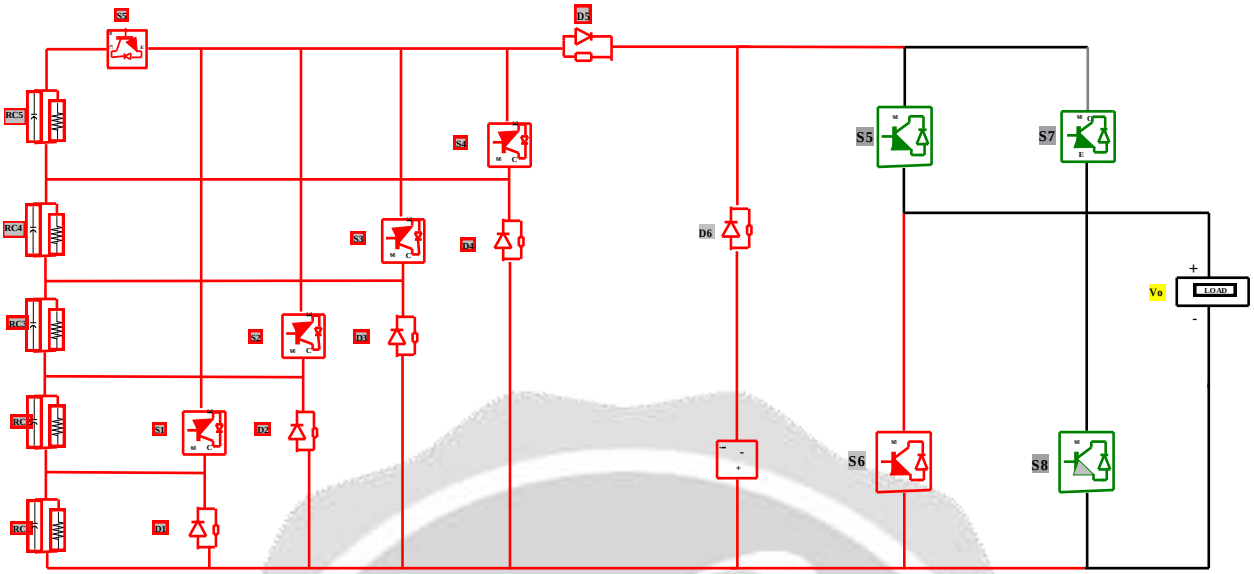


Fig. 4.2 (a) output voltage level 0.

2). Generate a voltage level $V_0 = \frac{1}{5}V_{dc}$

In the positive half cycle switch S1 is turned on. The capacitor C1 is providing energy. Switches S0, S5 and S8 are turned on and $\frac{1}{5}V_{dc}$ voltage applied on the load terminal.

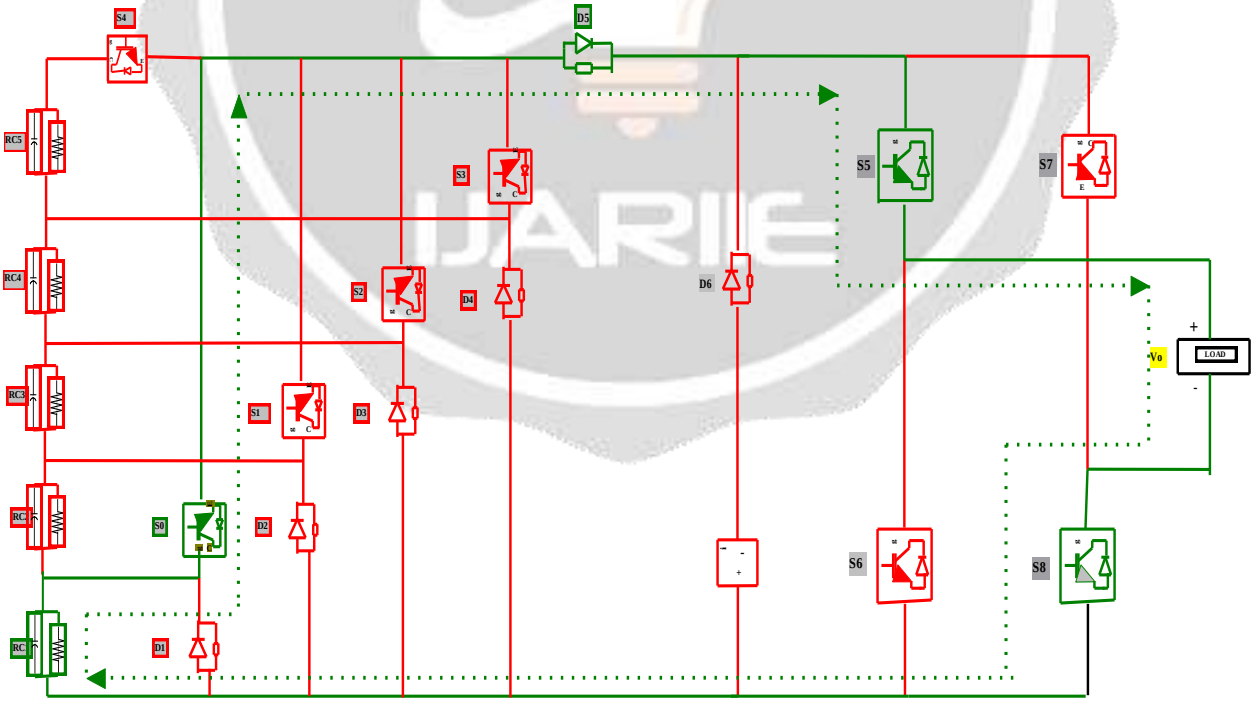


Fig.4.2 (b) output voltage level $\frac{1}{5}V_{dc}$.

3). Generate a voltage level $V_0 = \frac{2}{5}V_{dc}$

Switch S2 is turned on. Capacitor C1 and C2 are providing energy. S1,S5 and S8 are turned on, and the $\frac{2}{5}V_{dc}$voltage applied on the load terminals.

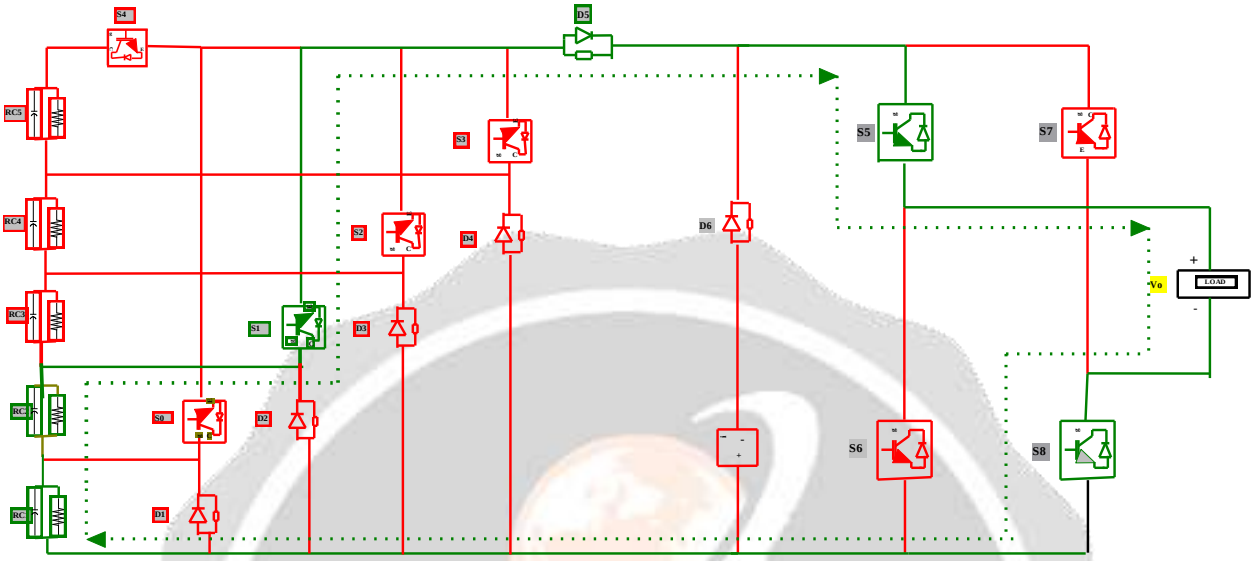


Fig.4.2 (b) output voltage level $\frac{2}{5}\ V_{dc}$.

4). Generate a voltage level $V_0 = \frac{3}{5}V_{dc}$

Switch S3 is turned on. Capacitor C1, C2 and C3 are providing energy. S5 and S8 are turned on, and the $\frac{3}{5}V_{dc}$voltage applied on the load terminal.

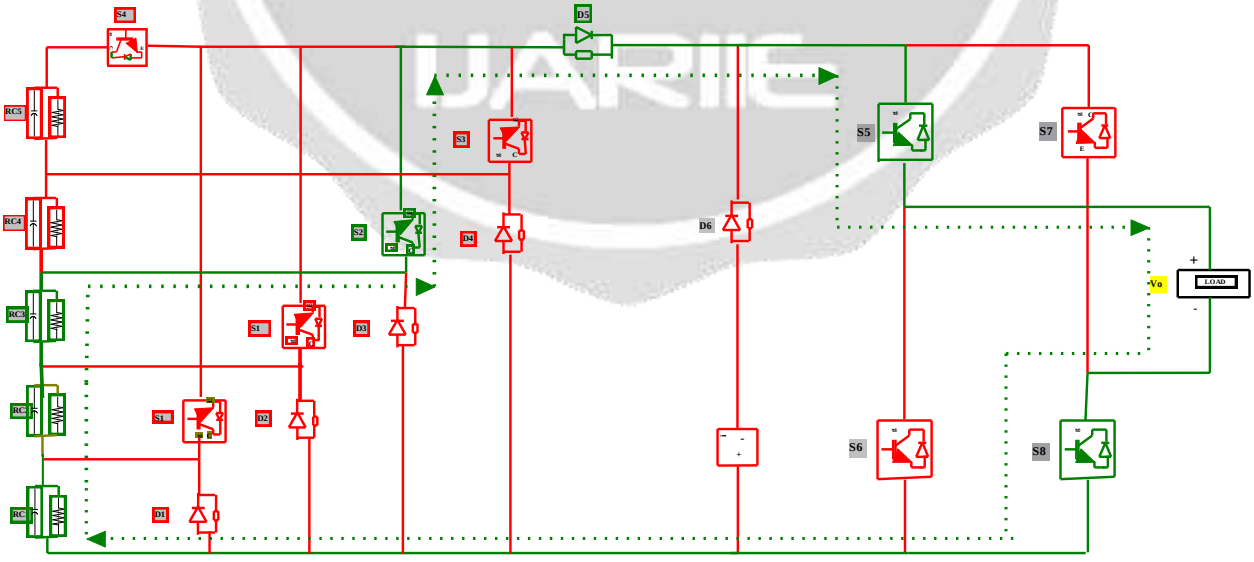


Fig.4.2 (c) output voltage level $\frac{3}{5}\ V_{dc}$.

5). Generate a voltage level $V_0 = \frac{4}{5} V_{dc}$

S4 is turned on. Capacitor C1, C2, C3 and C4 are providing energy. S5 and S8 are turned on, and the V_{dc} voltage applied on the load terminals.

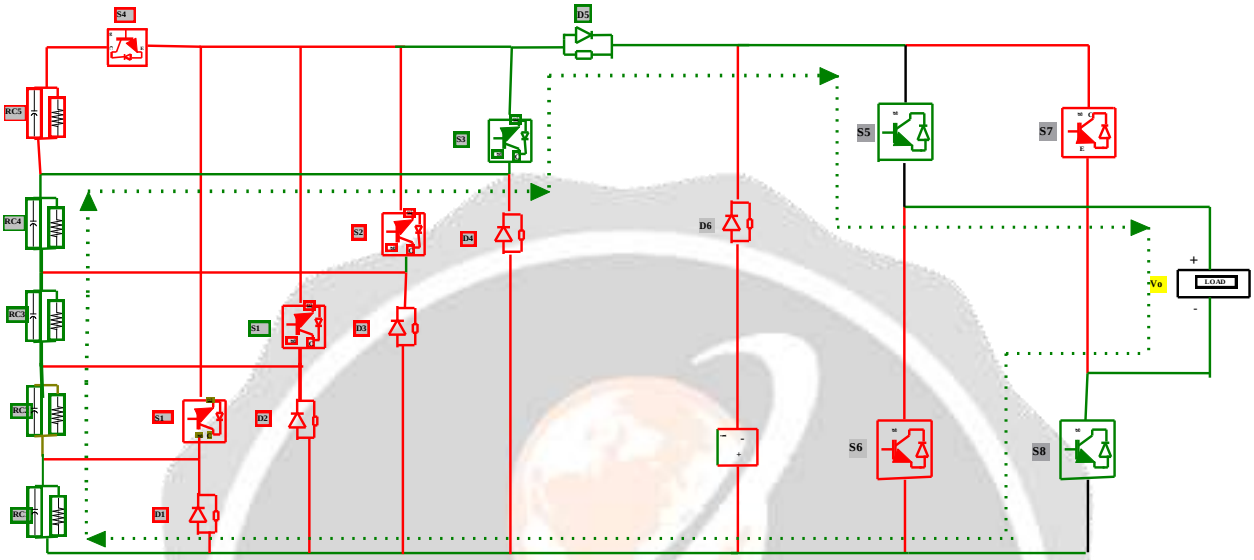


Fig. 4.2 (d) output voltage level $\frac{4}{5} V_{dc}$.

6). Generate a voltage level $V_0 = V_{dc}$,

S5 is turned on. Capacitor C1-C4 is providing energy. S5 and S8 are turned on, and the V_{dc} voltage applied on the load terminals.

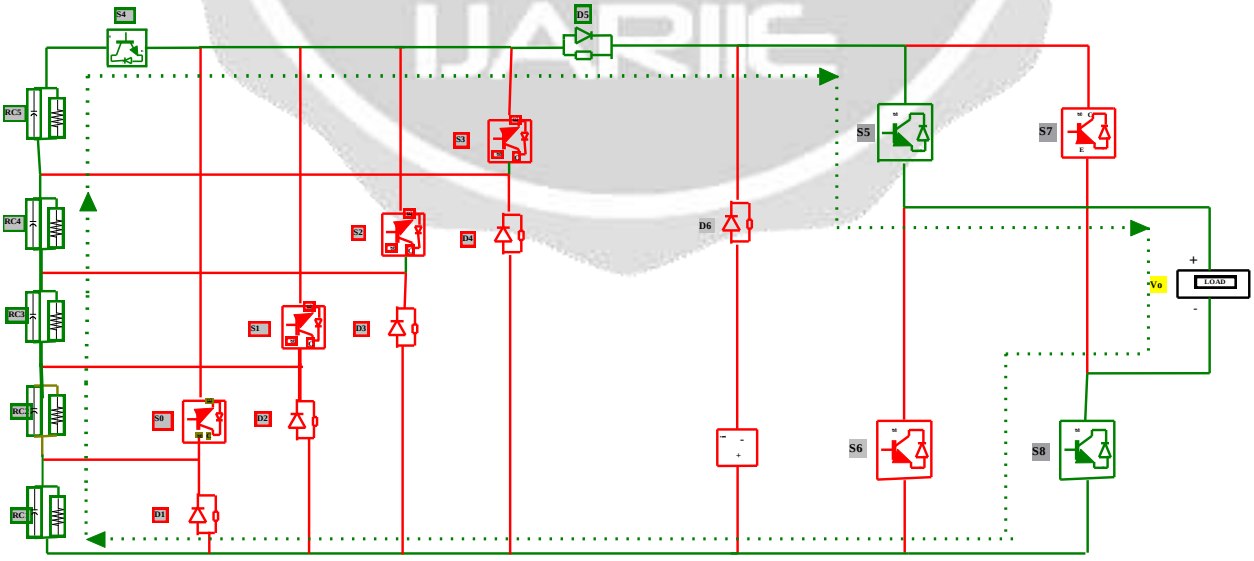


Fig. 4.2 (e) output voltage level V_{dc}.

7). Generate a voltage level $V_0 = -\frac{1}{5}V_{dc}$,

S0 is turned on. Capacitor C3 and C4 are providing energy. S6 and S7 are turned on, and the $-\frac{1}{5}V_{dc}$voltage applied on the load terminals.

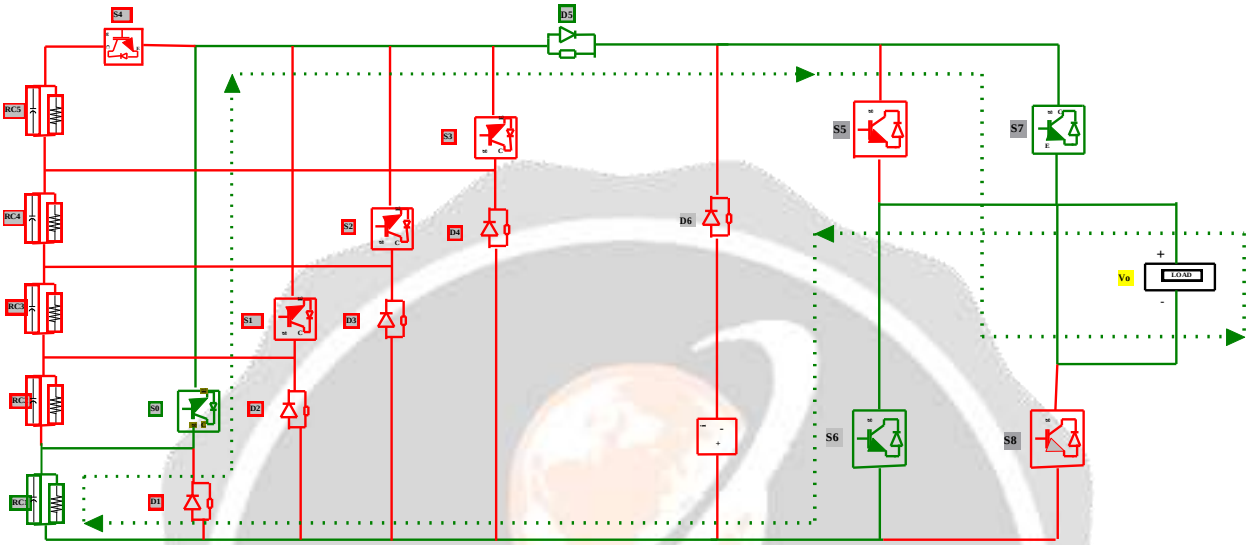


Fig. 4.2 (f) output voltage level$-\frac{1}{5}V_{dc}$.

8). Generate a voltage level $V_0 = -\frac{2}{5}V_{dc}$,

S1 is turned on. Capacitor C2, C3 and C4 are providing energy. S6 and S7 are turned on, and the $-\frac{2}{5}V_{dc}$voltage applied on the load terminals.

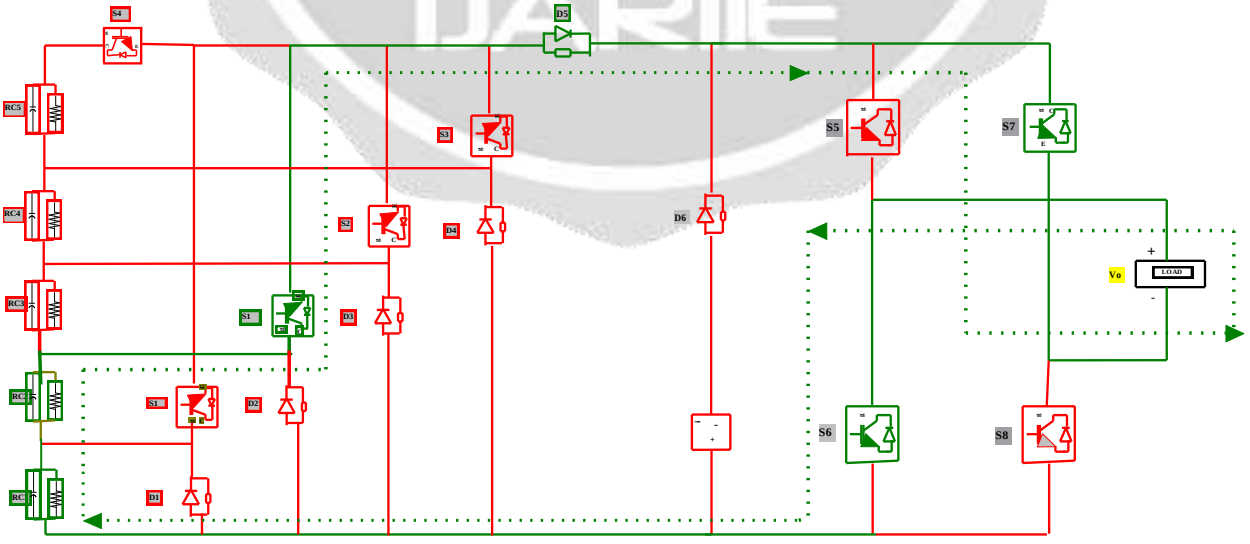


Fig. 4.2 (g) output voltage level $-\frac{2}{5}V_{dc}$.

9). Generate a voltage level $V_0 = -\frac{3}{5}V_{dc}$,

S2 is turned on. Capacitor C1, C2, C3 and C4 are providing energy. S6 and S7 are turned on, and the $-V_{dc}$voltage applied on the load terminals.

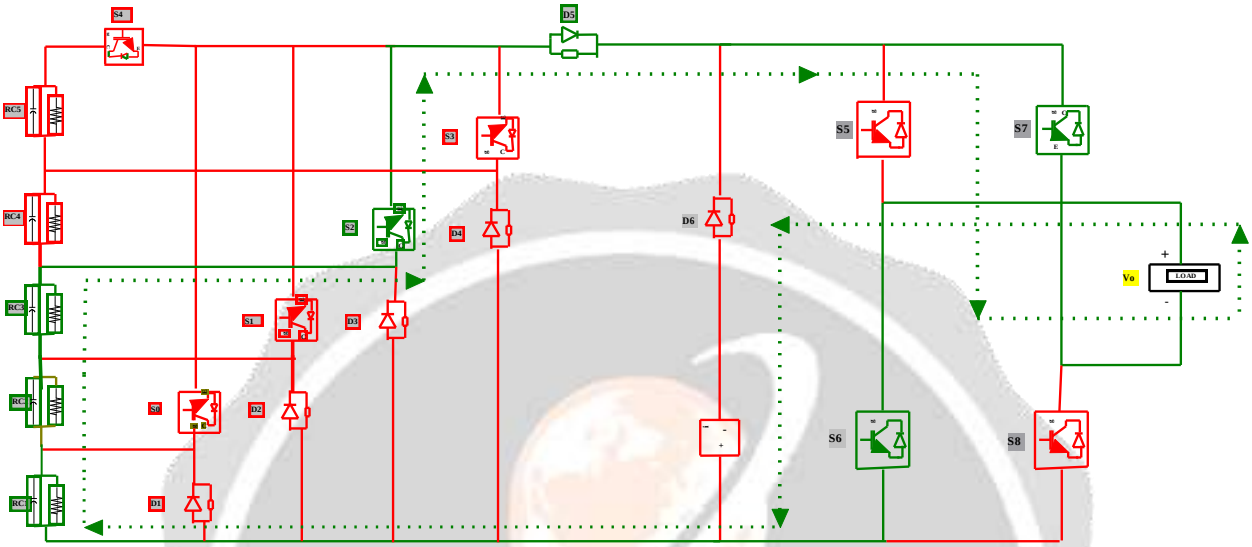


Fig. 4.2 (h) output voltage level $-\frac{3}{5}\ V_{dc}$.

10). Generate a voltage level $V_0 = -\frac{4}{5}V_{dc}$,

S3 is turned on. Capacitor C1, C2, C3 and C4 are providing energy. S6 and S7 are turned on, and the $-V_{dc}$voltage applied on the load terminals.

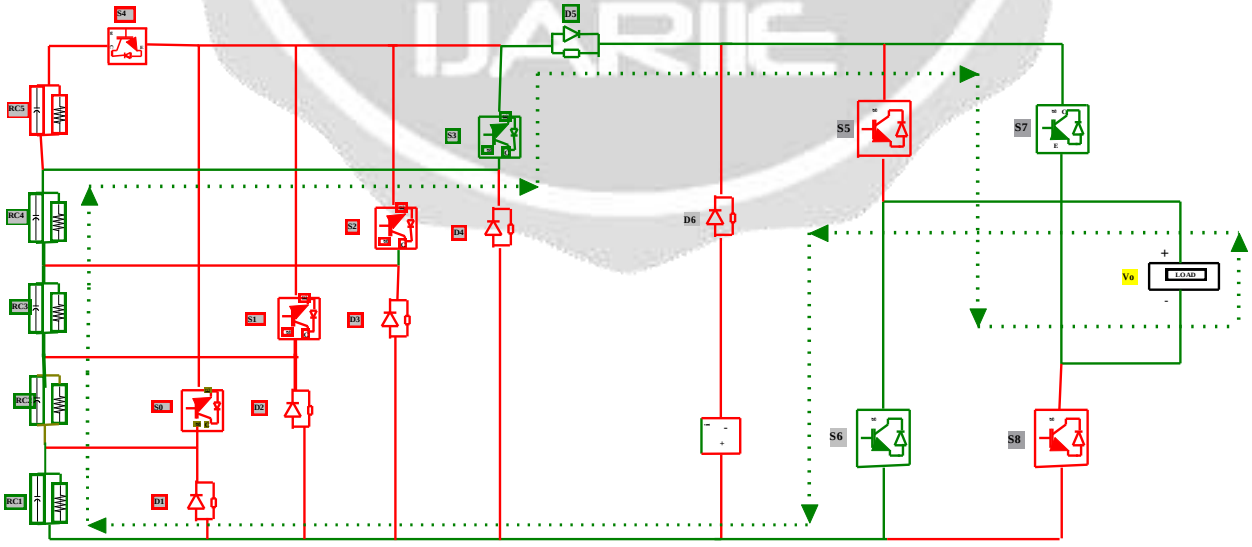


Fig. 4.2 (i) output voltage level $-= -\frac{4}{5}V_{dc}$.

11). Generate a voltage level $V_0 = -V_{dc}$,

S4 is turned on. Capacitor C1, C2, C3 and C4 are providing energy. S6 and S7 are turned on, and the $-V_{dc}$voltage applied on the load terminals.

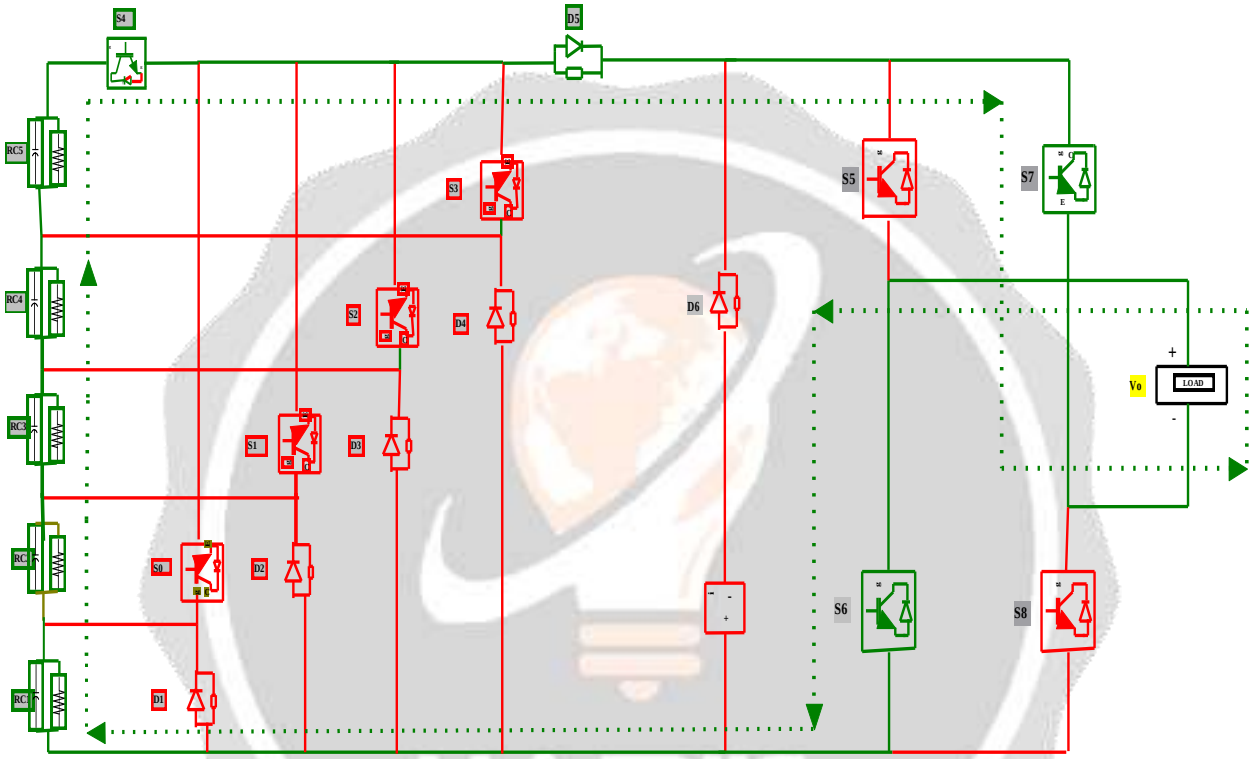


Fig. 4.2 (j) output voltage level $-V_{dc}$.

Table 4.1 switching combinations required to generate the

11-level output voltage waveform

S. No.	O/P Voltage	S0	S1	S2	S3	S4	S5	S6	S7	S8
1.	0	Off	Off	Off	Off	Off	On	Off	On	On
2.	$\frac{1}{5}V_{dc}$	On	Off	Off	Off	Off	On	Off	Off	On
3.	$\frac{2}{5}V_{dc}$	Off	On	Off	Off	Off	On	Off	Off	On
4.	$\frac{3}{5}V_{dc}$	Off	Off	On	Off	Off	On	Off	Off	On
5.	$\frac{4}{5}V_{dc}$	Off	Off	Off	On	Off	On	Off	Off	On
6.	V_{dc}	Off	Off	Off	Off	On	On	Off	Off	On
7.	$-\frac{1}{5}V_{dc}$	On	Off	Off	Off	Off	Off	On	On	Off

8.	$-\frac{2}{5}V_{dc}$	Off	On	Off	Off	Off	Off	On	On	Off
9.	$-\frac{3}{5}V_{dc}$	Off	Off	On	Off	Off	Off	on	On	Off
10.	$-\frac{4}{5}V_{dc}$	Off	Off	Off	On	Off	Off	on	On	Off
11.	$-V_{dc}$	Off	Off	Off	Off	On	Off	on	On	Off

TOPOLOGY COMPARISON

Table 4.2 the proposed topology is required to implement a three-phase eleven-level inverter

TABLE 4.2 DIFFERENTIATE BETWEEN THREE PHASE

ELEVEN-LEVEL INVERTER

	Proposed	Diode-clamped	Flying Capacitor	CDMLI
Switching device and gate drive	27	48	48	48
Flying capacitor	**0**	0	84	0
Diodes	15	168	0	0
DC bus capacitor/isolated supply	**12**	8	8	8

SPWM TECHNIQUE FOR PROPOSED TOPOLOGY

Sinusoidal pulse width modulation (SPWM) scheme is used to generate pulse. Where sinusoidal wave is reference wave and triangular wave is carrier wave. The comparison of both these waves gives rise to the pulses to trigger the switches. Single reference wave is compare with multiple carrier waves. Level shifting SPWM involve three schemes:

a. Phase disposition (PD),
b. Phase opposition disposition (POD)
c. Alternate phase opposition disposition (APOD).

In the proposed three-phase eleven-level inverter phase disposition method is used to generate pulse.
Fig.4.3 (a) represents the pulse logic block of SPWM for three-phase 11-level proposed MLI. The operation of pulse logic block contain relational operator. The sinusoidal waveform and triangular waveform are the input of SPWM logic block. Fig. 4.3 (b) represented the three-phase eleven-level inverter methodology of generating pulses. The ratio of Amplitude of reference wave (A_R) and amplitude of carrier wave (A_c) is known as modulation index.

$$m_a = \frac{A_R}{\frac{(N-1)}{2} \times A_c}$$

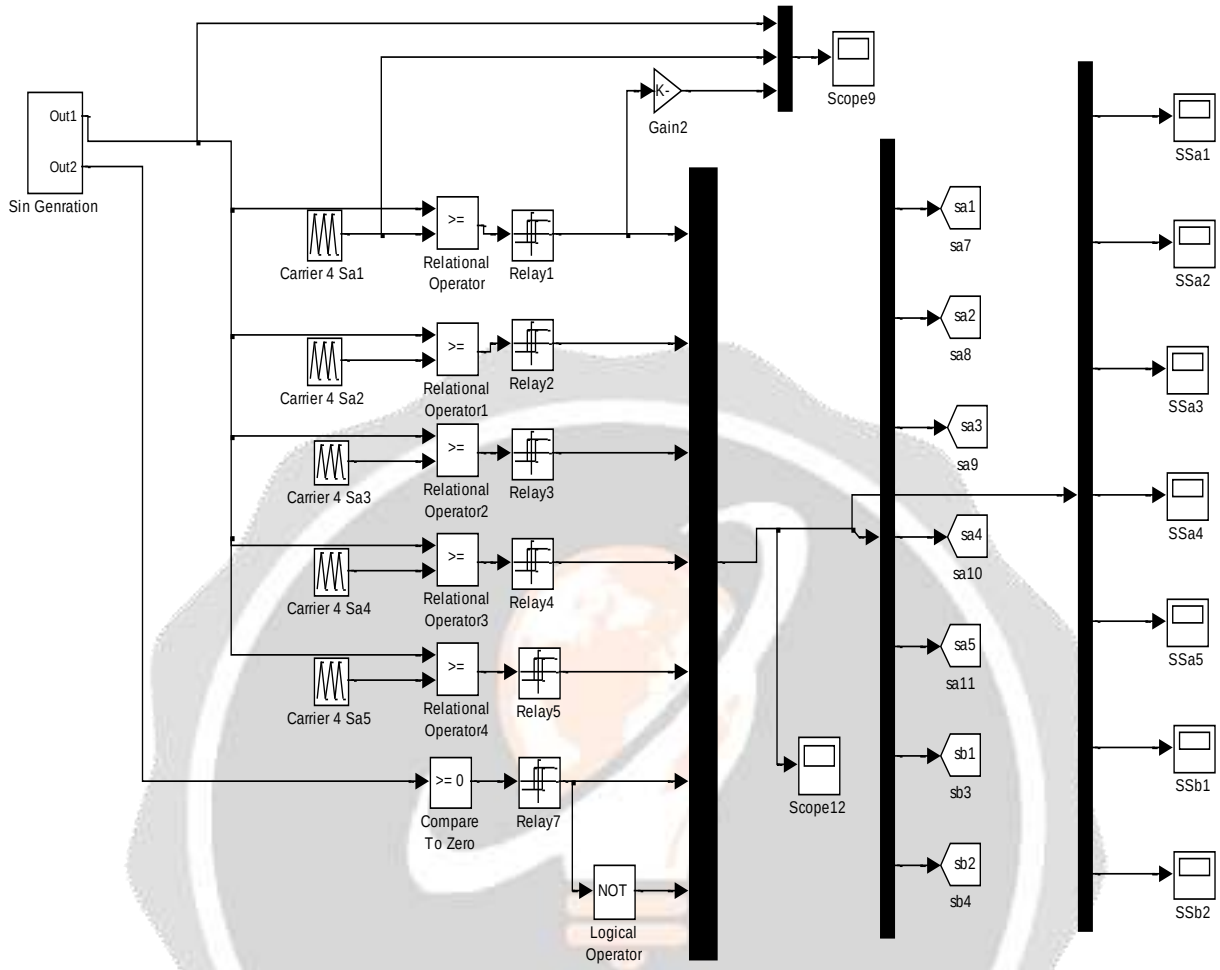


Fig 4.3 (a) SPWM pulse logic block

Fig 4.3 (b) shows switching pulse generation. It is observed that eleven-level is obtain four positive, four negative and one zero level. Amplitude of each level is 60V. Positive addition of all input voltage sources are 240V and negative addition

SIMULATION RESULT OF HARMONIC SPECTRUM OF LINE CURRENT, LINE VOLTAGE AND PHASE VOLTAGE

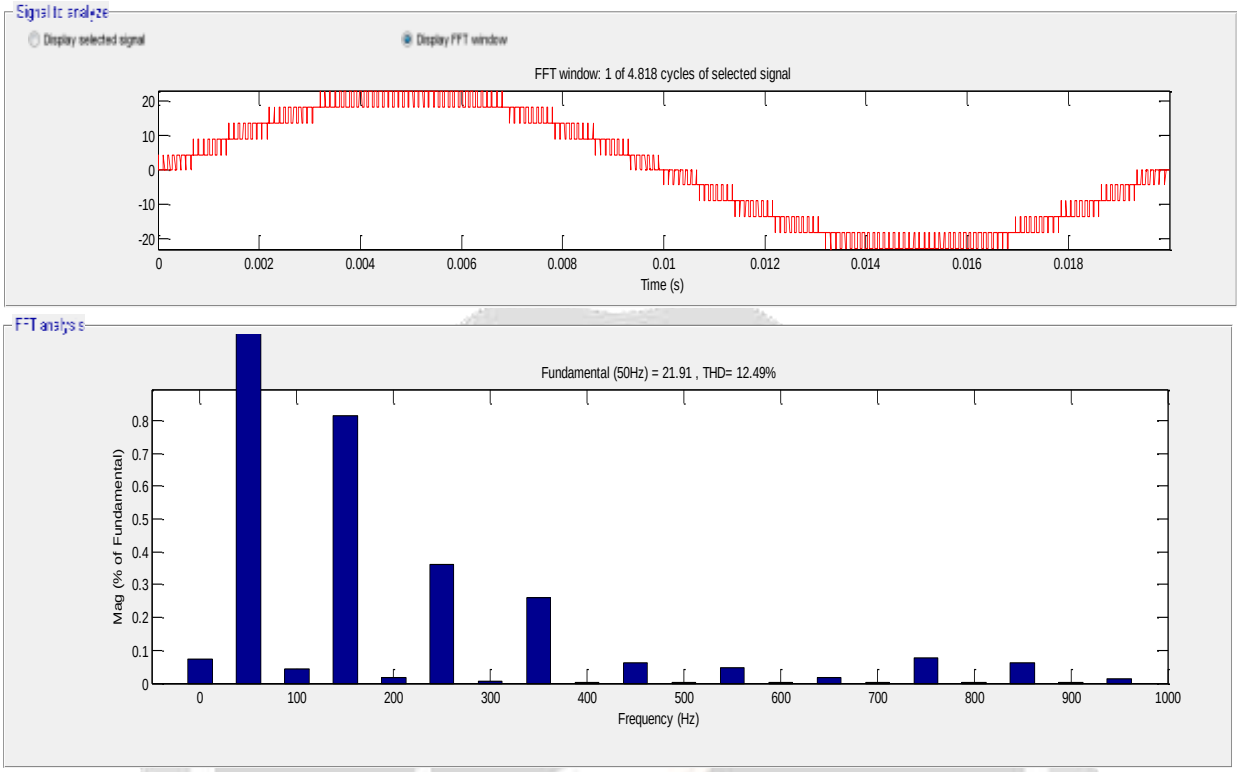
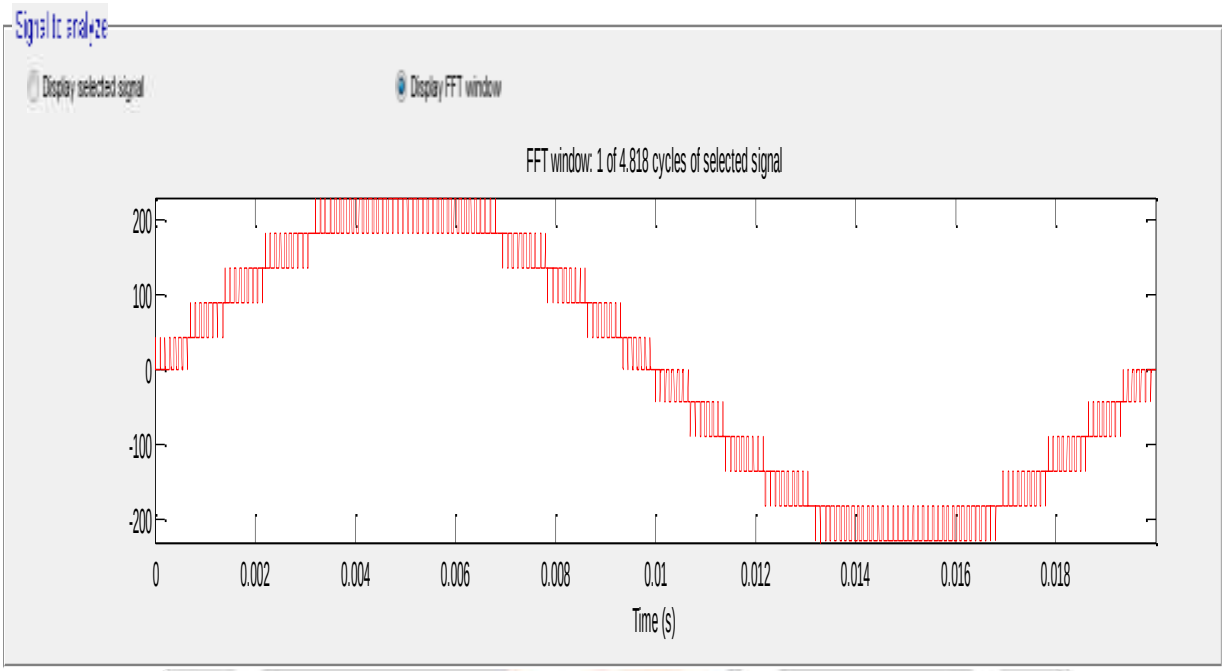


Fig. 5.11 harmonic spectrum line current of three-phase eleven-level inverter


Signal to analyze
Display selected signal
Display FFT window
FFT window: 1 of 4.818 cycles of selected signal
200
100
0
-100
-200
0
0.002
0.004
0.006
0.008
0.01
0.012
0.014
0.016
0.018
Time (s)

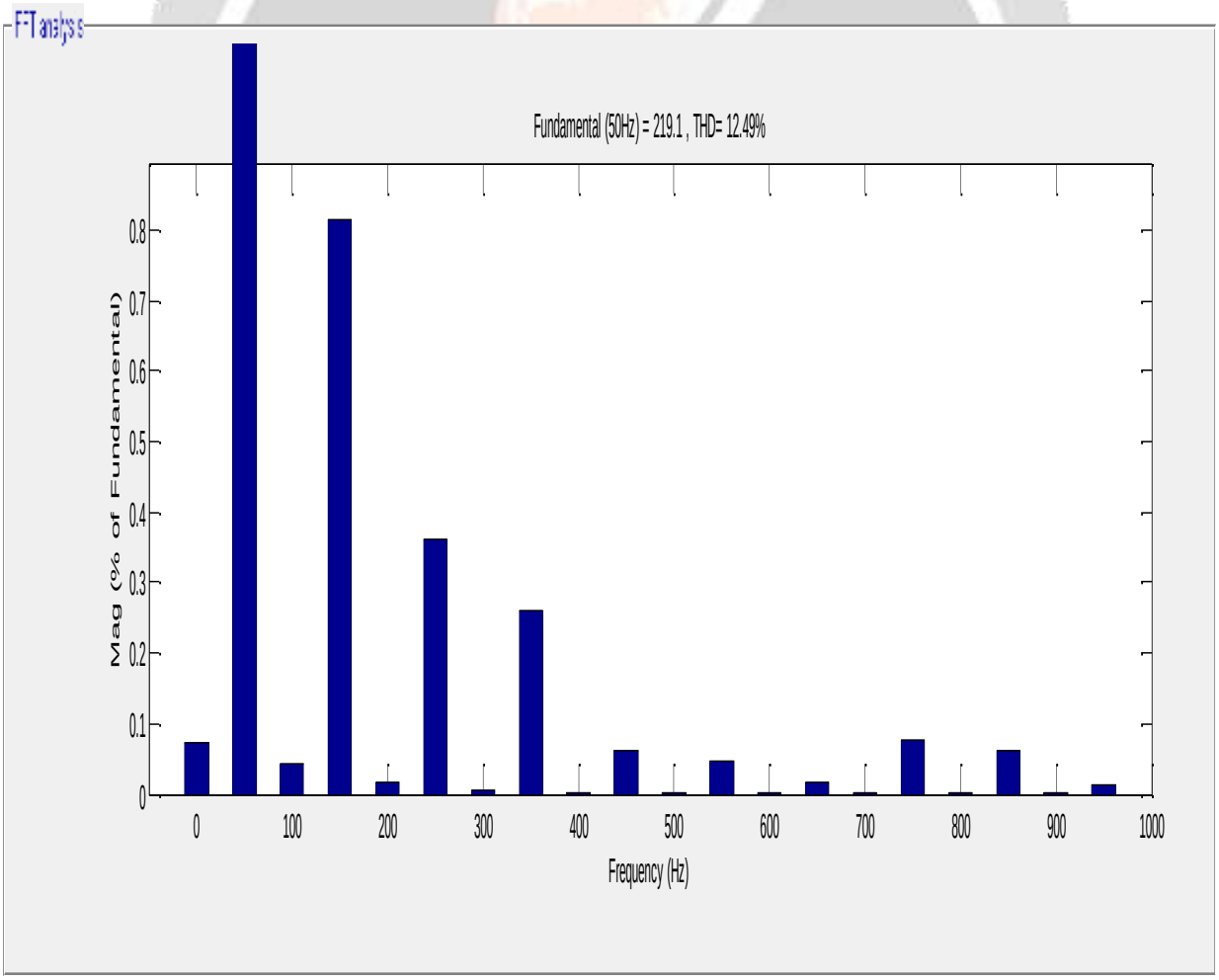

FFT analysis
Fundamental (50Hz) = 219.1 , THD= 12.49%
Mag (% of Fundamental)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0
100
200
300
400
500
600
700
800
900
1000
Frequency (Hz)

Fig. 5.12 harmonic spectrum phase voltage of three phase eleven-level inverter

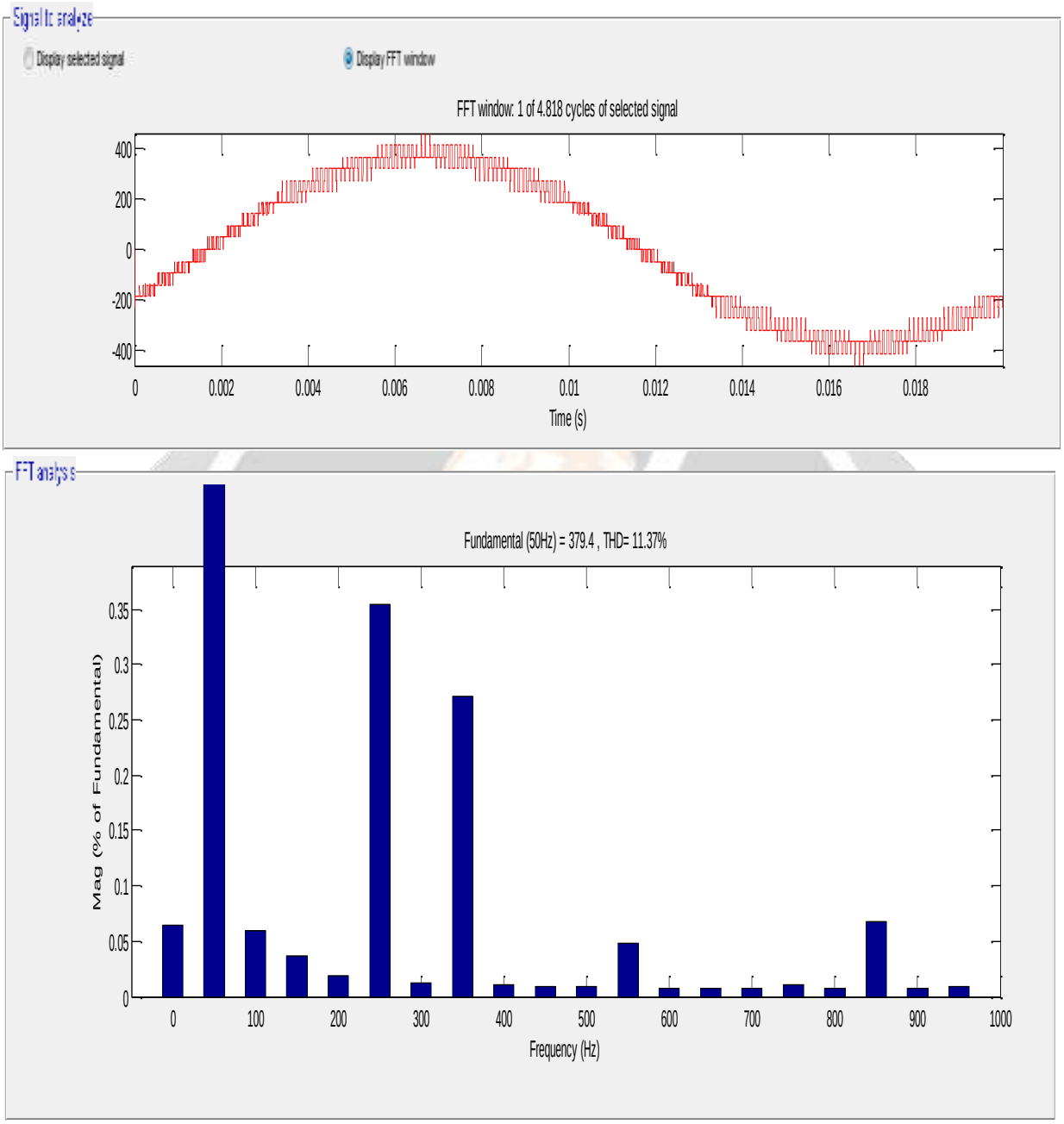


Fig. 5.13 harmonic spectrum line voltage of three phase eleven-level inverter

THD = 14.10%

REFERENCES:

1. Ayoub Kavousi, Behrooz Vahidi, Reza Salehi, Mohammad azem Bakhshizadeh, Naeem Farokhnia and S.Hamid Fathi, "Application of the BeeAlgorithm for Selective Harmonic Elimination Strategy in Multilevel Inverters", IEEE Transactions on power electronics, vol. 27, no. 4, pp1689-1696,2012.

2. Damoun Ahmadi, KeZou, Cong Li, Yi Huang and Jin Wang, "A Universal Selective Harmonic Elimination Method for High-Power Inverters",IEEE Transactions on power electronics, vol. 26, no. 10,pp2743-2752,2011.

3. FaeteFilho, Leon M. Tolbert, Yue Cao and BurakOzpineci, "Real-Time Selective Harmonic Minimization for Multilevel Inverters Connected to Solar Panels Using Artificial Neural Network Angle Generation",IEEE Transactions on industry applications, vol. 47, no. 5, pp2117-2124,2011

4. Hossein Sepahvand, Jingsheng Liao and Mehdi Ferdowsi, "Investigation on Capacitor voltage regulation VoltageRegulation in Cascaded H-Bridge MultilevelConverters With Fundamental Frequency Switching", IEEE Transactions on industrial electronics, vol. 58, no. 11,pp5102-5111,2011.

5. Jason R. Wells, XinGengPatrick L. Chapman Philip T. Kreinand Brett M. Nee, "Modulation-Based Harmonic Elimination", IEEE Transactionson power electronics, vol. 22, no. 1,pp336-340, 2007.

6. J. Napoles, A. J. Watson, J. J. Padilla, J. I. Leon, L. G. Franquelo, P. W. Wheeler and M. A. Aguirre,"Selective Harmonic Mitigation Techniquefor Cascaded H-Bridge Converters with Non-Equal DC Link Voltages", IEEE Transactions on power electronics,pp1-9,2012.

7. John N. Chiasson, Leon M. Tolbert, Keith J. McKenzieand Zhong Du, "A Unified Approach to Solving the Harmonic Elimination Equations inMultilevel Converters",IEEE Transactions on power electronics, vol. 19, no. 2, pp478-500,2004.

   A. Maheswari, S. Mahendran, Dr. I. Gnanambal, "Implementation of Fundamental Frequency Switching