Multilevel Inverter with Three Stage Hybrid Cascading using PWM Control Method

Presilla Vasanthini K.[1], Kala Priyadarshini G.[2], Aadyasha Patel[3]

[1, 2, 3] *Assistant Professor, Electrical & Electronics Engineering, PSVP Engineering College, Tamil Nadu, India*

ABSTRACT

The inverter power circuit is made up of 18 level hybrid cascaded multilevel scheme. The three hybrid inverter stages are the high, medium, and low voltage stages. The high-voltage stage is made of a three phase conventional inverter to reduce dc source cost and losses. The medium- and low voltage stages are made of three-level inverters constructed using cascaded H-bridge units. The aim of this control is to avoid undesirable high switching frequency for high and medium-voltage stages despite the fact that the inverter's dc sources are selected to maximize the inverter levels by eliminating redundant voltage states. Switching algorithms of the high and medium-voltage stages have been developed to assure fundamental switching frequency operation of the high-voltage stages and not more than few times this frequency for the medium-voltage stage. The low-voltage stage is controlled using PWM control to set the order of dominant harmonics as desired. The main and H-bridge cells are fed by isolated dc sources of 9V s, 3V s, and V s. This voltage ratio provides 18-level inverter. In this design, the high voltage stage has only one dc source that operates with reduced current ripple compared to the three dc sources of CHB design. The inverter has been designed with one main dc source to reduce the dc supply cost, and the supply voltage ratio has been selected to maximize the number of symmetrical levels.

Keyword : - *Multilevel Inverter, Hybrid Cascading, PWM technique, Variable Frequency, Harmonics.*

1. INTRODUCTION

The multilevel inverter has gained much attention in recent years due to its advantages in high power with low harmonics applications. The general function of the multilevel inverter is to synthesize a desired high voltage from several levels of dc voltages that can be batteries,fuel cells, etc. Asymmetrical MLI, which results from supplying the CHB cells with different dc voltages, provides higher number of levels for the same circuit topology [6]–[9]. The maximum number of levels is achieved when the cascaded-cell dc voltages form a ratio-3 geometric sequence [10]–[13]. This ratio has been used to construct inverters with large number of levels and, consequently, very small voltage distortion for various applications [12], [13]. Hybrid MLIs created by cascading smaller dissimilar inverter circuits can reduce the number of dc sources required [11]. Hybrid inverters have been implemented in various designs, such as the following: 1) connecting a two-level three-phase inverter in series with three-level stage(s) formed by fullbridge cells [13]; 2) connecting H-bridge three-level stage(s) in series with aneutral-point-clamped three-level stage [12]; 3) cascading two three-level neutral-pointclamped inverter by connecting their outputs to the two sides of an openwinding load [13]; Three Stage hybrid cascaded multilevel inverter can be used as inverse sine PWM technique. This PWM control method for ISPWM technique used for eliminate odd harmonic of the multilevel inverter. The inverter can be used in hybrid electric vehicles (HEV) and electric vehicles (EV). An HEV combines a conventional internal combustion engine, a battery pack, and an electric motor. An EV includes rechargeable batteries and an electric motor. The power inverter that drives the electric motor is a key device of a HEV and EV. To develop the model of a hybrid cascaded multilevel inverter, a simulation is done based on MATLAB simulink platforms. Figure 1 shows the block diagram of a Three stage Hybrid Cascaded Multilevel Inverter with PWM control method.

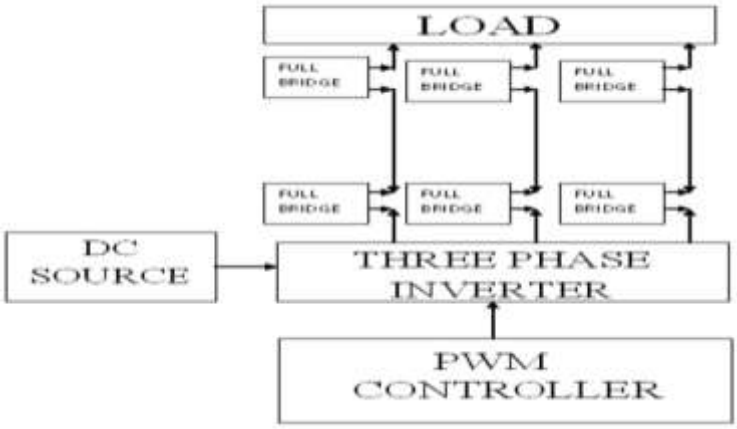

Fig - 1 Block diagram

2. OPERATION PRINCIPLE OF THE HYBRID MULTILEVEL INVERTER

Figure 2 shows a proposed three stage hybrid cascaded multilevel inverter with PWM control method. The bottom is one leg of a standard 3-leg inverter with a DC power source. The top is an H-bridge in series with each standard inverter leg. The H-bridge can use a separate DC power source or a capacitor as the dc power source [7-11].

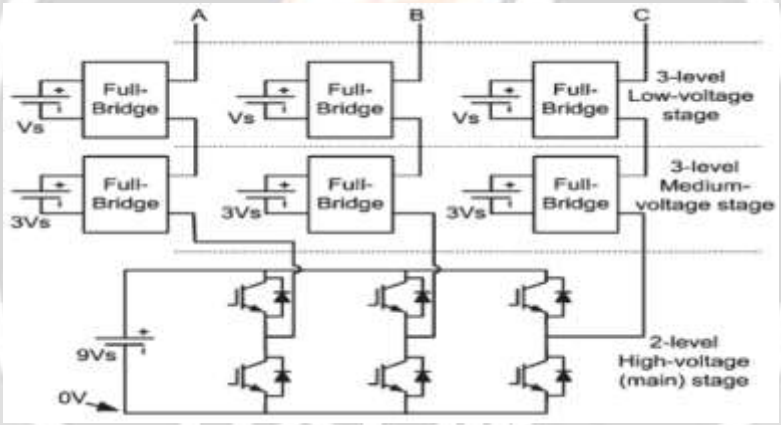

Fig - 2 Circuit Diagram

The output voltage V_1 of this leg (with respect to the ground) is either $+V_{dc}/2$ (S_5 closed) or $-V_{dc}/2$ (S_6 closed). This leg is connected in series with a full H-bridge that in turn is supplied by a capacitor voltage. If the capacitor is kept charged to $V_{dc}/2$, then the output voltage of the H-bridge can take on the values $+V_{dc}/2$ (S_1, S_4 closed), or (S_1,S_2 closed or S_3, S_4 closed), or $-V_{dc}/2$ (S_2, S_3 closed). This H-bridge cell output given to the another one H-bridge cell. This H-bridge charged $V_{dc}/2$ then they output voltage of the H-bridge cell can take one the value $V_{dc}/2$ (S_1,S_2 closed or S_3, S_4 closed), or $-V_{dc}/2$ (S_2, S_3 closed). An example output waveform that this topology can achieve is shown in Figure 3 (a).

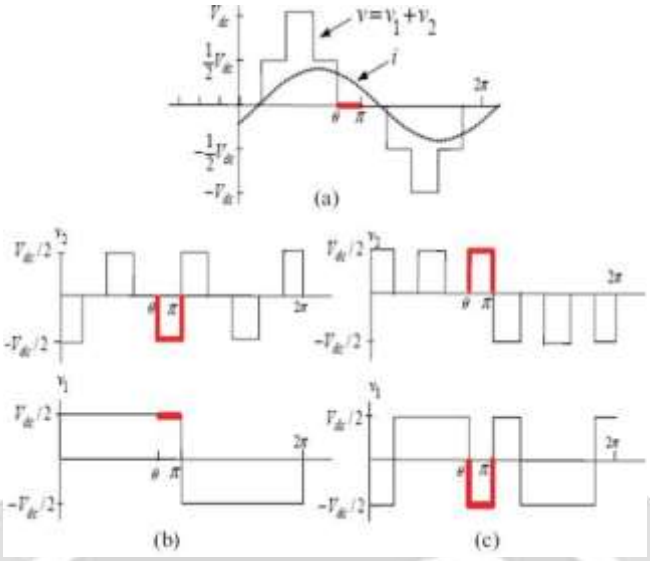

Fig - 3 Capacitor voltage regulation process

When only a dc power source is used in the inverter, that is, the H-bridge uses a capacitor as the dc power source, the capacitor's voltage regulation control details are illustrated in Figure 3. If S_1, S_4 are closed (so that $V_2 = +V_{dc}/2$) along with S_6 closed (so that $V_1 = V_{dc}/2$), then the capacitor is discharging ($i_c = i < 0$ see Fig. 3 (b)) and $V = V_1 + V_2 = 0$. On the other hand, if S_2, S_3 are closed (so that $V_2 = V_{dc}/2$) and S_5 is also closed (so that $V_1 = +V_{dc}/2$), then the capacitor is charging ($i_c = I > 0$ see Figure 3 (c)) and $V = V_1+V_2 = 0$. The case $i < 0$ is accomplished by simply reversing the switch positions of the $i > 0$ case for charge and discharge of the capacitor. Consequently, the method consists of monitoring the output current and the capacitor voltage so that during periods of zero voltage output, either the switches S_1, S_4, and S_6 are closed or the switches S_2, S_3, S_5 are closed depending on whether it is necessary to charge or discharge the capacitor. As Figure 3 illustrates, this method of regulating the capacitor voltage depends on the voltage and current not being in phase. That means one needs positive (or negative) current when the voltage is passing through zero in order to charge or discharge the capacitor. Consequently, the amount of capacitor voltage the scheme can regulate depends on the phase angle difference of output voltage and current. It is noted that the above capacitor voltage regulation method is described using a fundamental frequency modulation scheme because it is easier to illustrate [7].

2.1 Proposed Variable Frequency Inverted Sine PWM Technique (VFISPWM)

The proposed control strategy replaces the conventional fixed frequency carrier waveform [6] by variable frequency inverted sine wave. The inverted sine PWM has a better spectral quality and a higher fundamental voltage compared to the triangular based PWM.But the main drawback is the marginal boost in the magnitude of lower order harmonics and unbalanced switch utilization. This is overcome by employing variable frequency inverted sine carrier signals. In order to balance the number of active switching among the levels is to vary the carrier frequency based on the slope of the modulating wave in each band. The frequency ratio for each band should be set properly for balancing the switching action for all levels. The reference carrier frequency was chosen as 3950Hz as switching losses and THD both are low as shown in Figure 4. With the carrier reference frequency of 3950Hz applied to the band-1, the new frequencies for bands 2 and 3 are assigned proportional to their respective slopes. Figure 5 shows the three bands for different carrier frequency. Figure 6 shows carrier and reference waveform of the ISPWM, whereas, figure 7 shows generation of gating pulses for ISPWM.

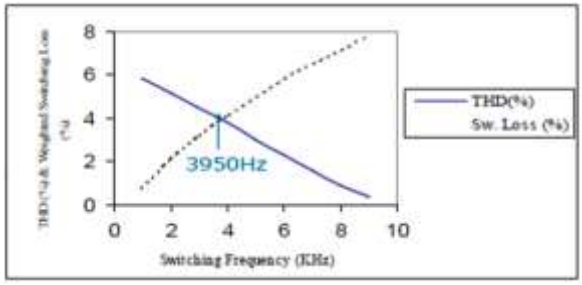

Fig - 4 Inverse PWM technique.

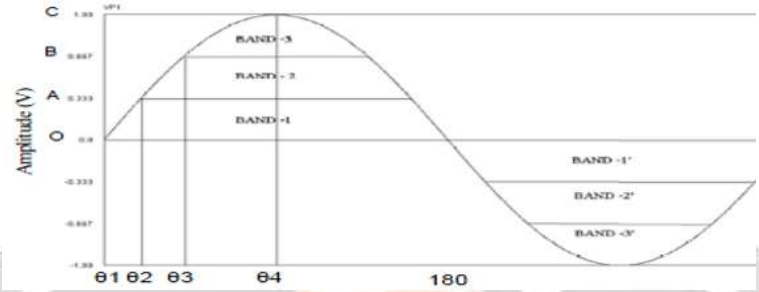

Fig - 5 Three bands for different carrier frequency.

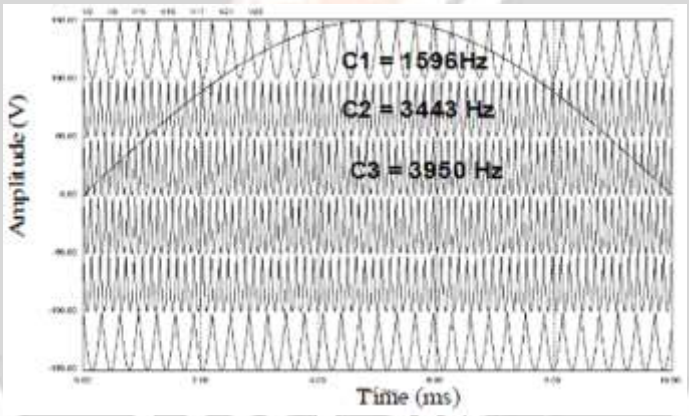

Fig – 6 Carrier and Reference waveform of the ISPWM.

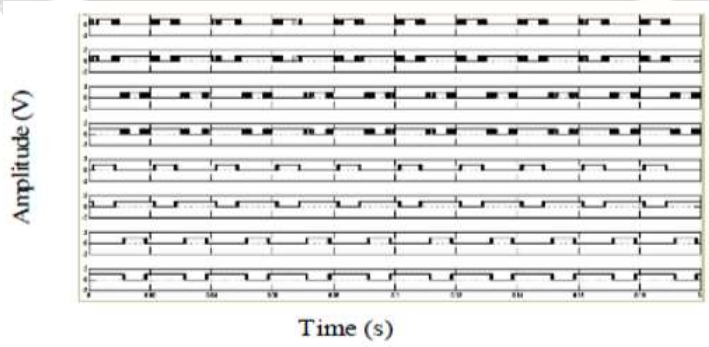

Fig – 7 Generation of gating pulses for ISPWM

2.2 Selective Harmonic Elimination

By placing notches in the output waveform at proper locations, certain harmonics can be eliminated. This allows lower switching frequencies to be used; lower losses, higher efficiency. Figure 8 shows the harmonic elimination process.

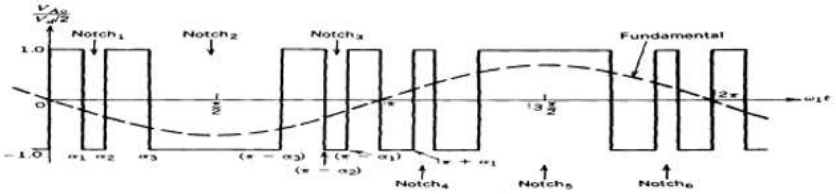

Fig – 8 Harmonic elimination

For a waveform with quarter-cycle symmetry, only the odd harmonics with sine components will appear, i.e. $a_n=0$ and

$$v(t) = \sum_{n=1}^{\infty} b_n \sin n\omega t$$

$$b_n = \frac{4}{\pi}\int_0^{2\pi} v(t)\sin(n\omega t)\, d(\omega t)$$

$$b_n = \frac{4}{n\pi}\left[1 + 2\sum_{K=1}^{K}(-1)^K \cos n\alpha_K\right]$$

Thus we have K variables (i.e. α_1, α_2, α_3, ... α_K) and we need K simultaneous equations to solve for their values.With K α angles, K-1 harmonics can be eliminated. Consider the 5th and 7th harmonics (the 3rd order harmonics can be ignored if the machine has an isolated neutral). Thus K=3 and the equations can be written as:

Fundamental:

$$b_1 = \frac{4}{\pi}(1 - 2\cos\alpha_1 + 2\cos\alpha_2 - 2\cos\alpha_3)$$

5th Harmonic:

$$b_5 = \frac{4}{5\pi}(1 - 2\cos 5\alpha_1 + 2\cos 5\alpha_2 - 2\cos 5\alpha_3) = 0$$

7th Harmonic:

$$b_7 = \frac{4}{7\pi}(1 - 2\cos 7\alpha_1 + 2\cos 7\alpha_2 - 2\cos 7\alpha_3) = 0$$

3. RESULTS

Figure 9 shows the Carrier and reference waveforms. From figure 10, we see the pulses generated by the pulse generator. And figure 11 shows the output waveforms.

Fig – 9 Carrier and reference wave

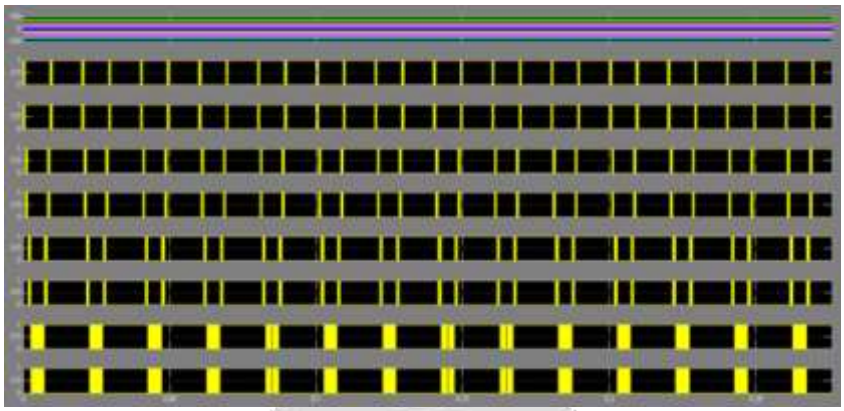

Fig – 10 Pulse generation

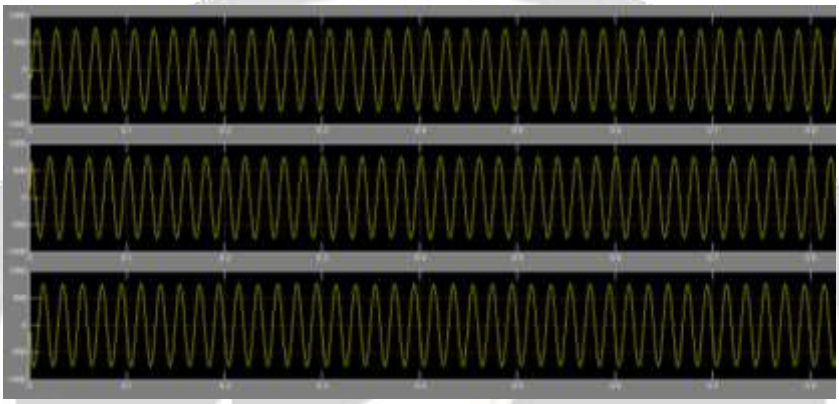

Fig – 11 Output waveform

4. CONCLUSIONS

A simulation model for the three stage hybrid cascaded multilevel inverter is developing in MATLAB and simulation. The inverter output is a 18 level phase voltage this paper presents a men circuit model in MATLAB and simulation details. This system operates in high and medium low voltage stage. In the future design of three stage hybrid cascade multilevel inverter fed induction motor with PWM control method can be implemented.

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