# Novel Approach to Design Ternary D- flip flop using FGMOS

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## ABSTRACT

*In this paper ternary logic is combined with FGMOS (Floating Gate MOS), due to the controllability property of the FGMOS it becomes more compatible with ternary logic as threshold voltage can be adjusted. In this paper, ternary D-flip flop is designed using FGMOS. For this, ternary NAND gates are used, they are designed by using two different methods. Then transistor count is compared for both methods. Using this, number of transistors used per circuit decreases, so the chip area will be lesser and also there will be decrease in power dissipation. This proposed work is designed with the help of tanner tool version 13.0.*

**Keywords**: *MIFGMOS (Multi Input Floating Gate MOS), FGMOS (Floating Gate MOS), Ternary logic, NAND gate, D- flip flop*

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## 1. INTRODUCTION

Ternary logic is now coming into picture due to the advantages it have over that of binary. As we have used binary logic from a very long time, it is known that it has two values 0 and 1; or true and false. But as ternary logic is a new concept to many of us, as it is not in the picture yet. Ternary logic can be defined as having three representational values; true, false and indeterminate value. Ternary logic has various advantages over binary. It uses less memory space to store data and requires lesser address lines to address the data in memory. It requires fewer interconnections which lead to reduction in chip area. By using ternary, efficiency increases. Table I shows the ternary logic. It has been proposed by the researchers that ternary logic can be categorized in two; balanced logic system and the unbalanced logic system. Balanced logic system has –VDD for logic 0, 0V for logic 1 and +VDD for logic 2. Unbalanced logic system has 0V for logic 0, Vdd/2 for logic 1 and Vdd for logic 2.

## 2. FGMOS TRANSISTOR

Floating gate MOS is similar to the conventional MOSFET with a second polysilicon layer on the floating gate. As seen from the fig. 1, floating gate is isolated from any physical contact with the polysilicon layer. Due to this floating gate multiple numbers of inputs can be capacitive coupled to the gate. It is also called as Multi input floating gate MOS. The output of the floating gate is the weighted sum of all the capacitive coupled inputs to the gate. This controls the on and off state of the transistor. Because of this property of MIFGMOS, it is easy to control the threshold voltage Vth [1]

$$\emptyset_F(t) = \emptyset_F(0) + \frac{\sum_{i=1}^{n}\left(C_i V_i(t) - C_i V_i(0)\right)}{\sum_{i=0}^{n} C_i} \quad (1)$$

Where n is the number of inputs and Ø_F (t) is the potential at the floating gate. So transistor turns on when,

$$\frac{V_1C_1+V_2C_2+\cdots+V_nC_n}{C_1+C_2+\cdots+C_n+C_0} > V_{th} \qquad (2)$$

From the equation (2), Vth of the FGMOS can be adjusted. Due to the control on the threshold voltage FGMOS can be used for both analog and digital application. FGMOS are used in memory devices like EPROM, EEPROM, and flash memories.

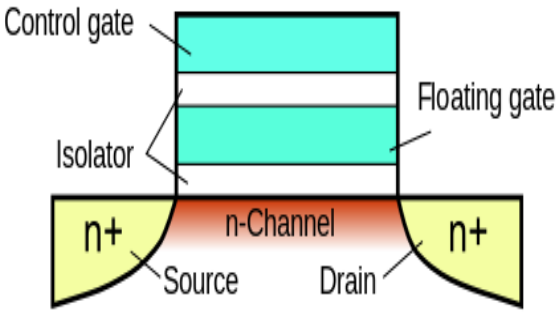


**FIG1(A). MIFGMOS**

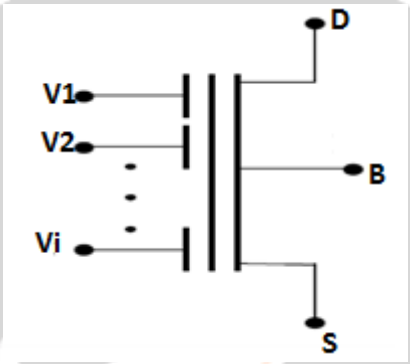


**FIG 1(B). MIFGMOS SYMBOL**

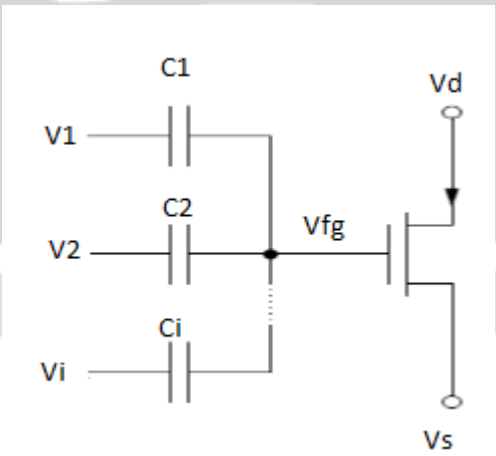


**FIG 2.AN n-INPUT NMOS FG TRANSISTOR**

### 3. TERNARY NAND GATE

For ternary logic NAND gate can be defined as,

$$TNAND = min[\overline{A,B}]$$

The truth table for ternary NAND is given in table 1.

**TABLE 1: TNAND TRUTH TABLE**

| A | B | Out |
|---|---|---|
| 0 | 0 | 2 |
| 0 | 1 | 2 |
| 0 | 2 | 2 |
| 1 | 0 | 2 |
| 1 | 1 | 1 |
| 1 | 2 | 1 |
| 2 | 0 | 2 |
| 2 | 1 | 1 |
| 2 | 2 | 0 |

Ternary NAND gate can be designed by two methods. They are,

1. Using only FGMOS [2]

In this method MOS is replaced by FGMOS in ternary circuits.

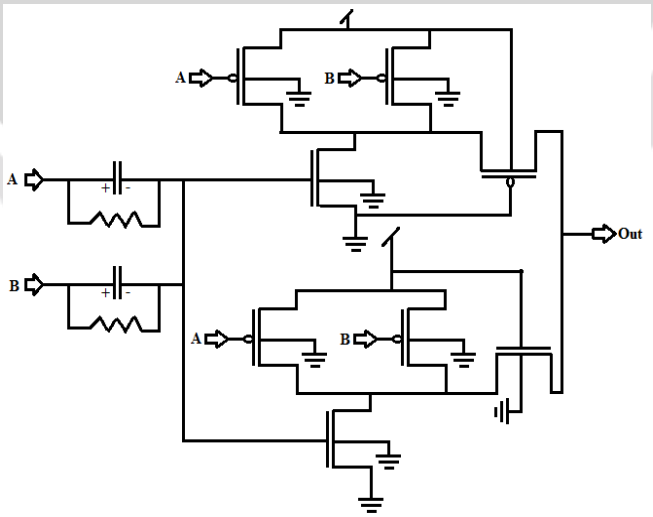


**FIG 3. T-NAND USING ONLY FGMOS**

2. Hybrid method (Using FGMOS and conventional MOS together) [1]

Conventional MOS and FGMOS are used together in hybrid method. Parallel combination of MOS is replaced by FGMOS in CMOS circuit. This will lead to decrease in transistor count.

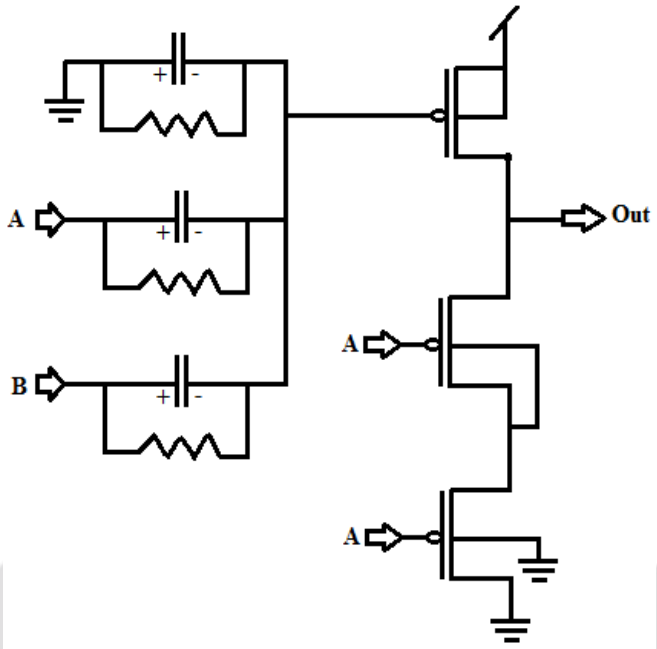


**FIG 4. T-NAND USING HYBRID METHOD**

## 4. D – FLIP FLOP

The basic working of D- flip flop is, output is same as input. Using the hybrid ternary NAND gate, D- flip flop is designed. As, hybrid ternary NAND gate is used to design D- flip flop, transistor count further decreases. It will lead to lesser chip area and decreases in power consumption.

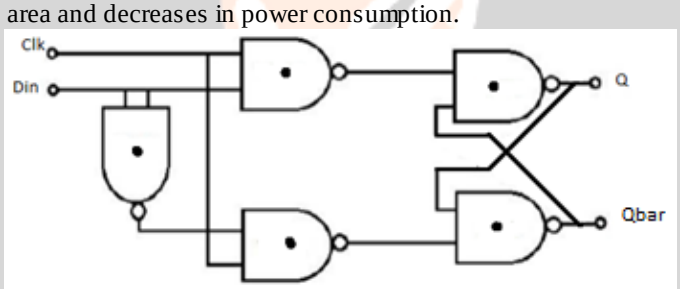


**FIG 5. D-FLIP FLOP**

**TABLE 2: COMPARISION**

| | Transistor count in Simple Approach [3] | Transistor count in Hybrid Approach |
|---|---|---|
| T- NAND | 8 | 3 |
| D- Flip Flop | 40 | 15 |

## 5. SIMULATION RESULT

This is the output waveform of the designed D- flip flop. In this waveform, starting from bottom, first one shows the clock cycle, second is D input, third is Q output wave and the last is the complement of Q output wave (Qbar).

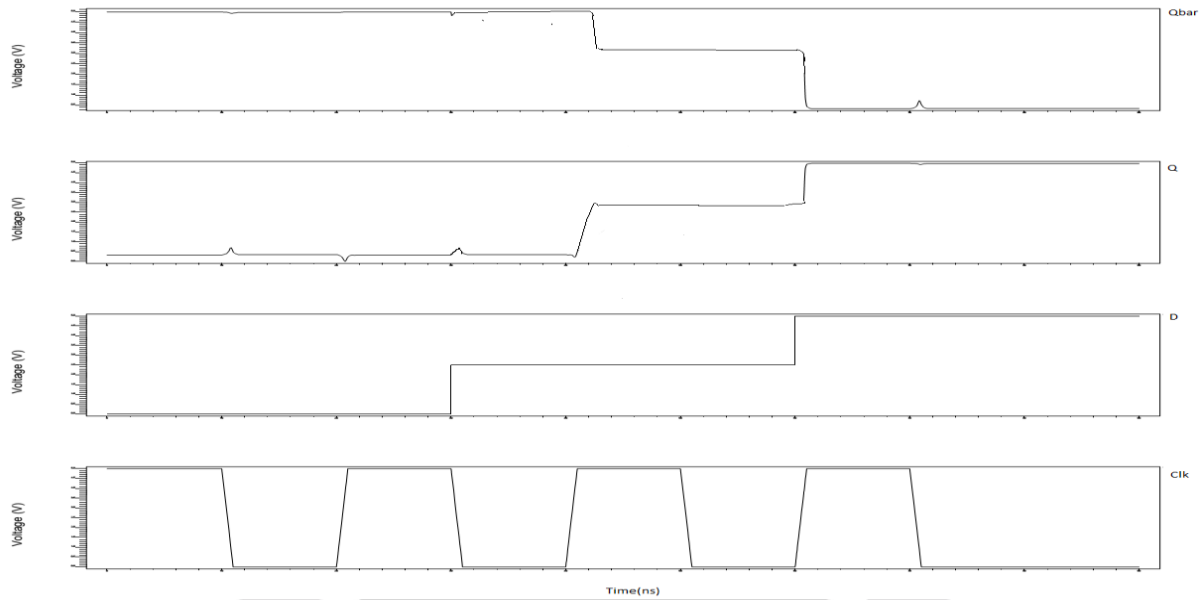


**FIG 6. WAVEFORM OF D-FLIP FLOP**

## 6. CONCLUSION

It can be seen from different paper referred that using FGMOS, transistor count reduces. In this paper two methods are given to design ternary NAND gate. By comparing the two methods, it can be seen that the hybrid approach is effective in reduction of transistor count. This will obviously counts to the reduction in the chip area. Ternary logic is all about three state values and using it with MIFGMOS, because MIFGMOS is the only MOSFET with threshold voltage controlling. So it can amplify the efficiency. From table 2, hybrid approach uses less than half number of transistor as compared to first method.

## 7. REFERENCES

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