PERFORMANCE ANALYSIS OF PULSED LATCH BASED SHIFT REGISTER

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ABSTRACT

The implementation of shift register using pulsed latches instead of flip flops is discussed in this paper. For designing the latch, Static Differential Sense Amplification Shared Pulsed Latch (SSASPL) is used along with Multi-threshold Complementary Metal Oxide Semiconductor (MTCMOS) to avoid the subthreshold leakage. Pulsed latch requires less area and power because it is smaller than the flip flop. But the pulsed latch cannot be used because timing problem occurs between pulsed latches. This is overcome by using multiple non-overlap delayed pulsed clock signals. Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator. In the proposed shift register minimum number of the pulsed clock signals are used by grouping more number of sub shifter registers and using additional short-term storage latches. The AND and NOT gate in the pulser circuit are designed using GDI (Gate Diffusion Input) technique, to reduce the number of transistors used in the design. The design is simulated in Tanner EDA and the results obtained are in such a way that, the area and power consumption are reduced.

Keyword: *Gate Diffusion Input (GDI), MTCMOS (Multi-threshold Complementary Metal Oxide Semiconductor), SSASPL (Static Differential Sense Amplification Shared Pulsed Latch) and Pulsed Latch*
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1. INTRODUCTION

Power consumption is the main objective to design a shift register using pulsed latches. Pulsed latch requires less area and power because it is much smaller than flip flop but the pulsed latch cannot be used because timing problem occurs between pulsed latches. A master-slave flip-flop designed using two latches can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch cannot be used in shift registers due to the timing problem. Area and power consumption of the pulse latch will become almost half of the master slave flip-flop. The pulsed latch is good solution for very less area and less power consumption.

2. ARCHITECTURE OF PROPOSED SHIFT REGISTER

The proposed 16-bit shift register is divided into 4 sub shift registers to reduce the number of delayed pulsed clock signals as shown in Fig-1. A 4-bit sub shift register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals. The proposed shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches.

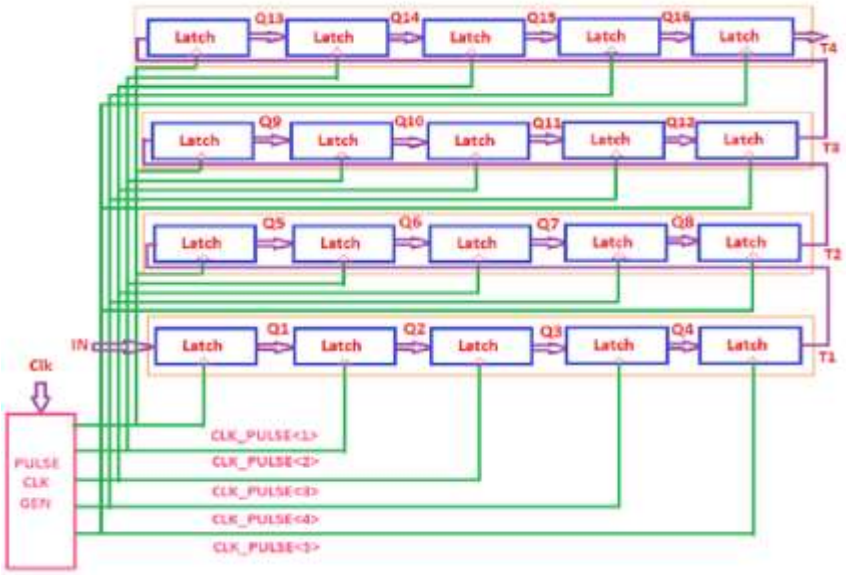

Fig -1: Pulsed latch based shift register

2.1 SSASPL DESIGN

The SSASPL (Static differential sense amplification shared pulse latch) uses the smallest number of transistors (7 transistors) as shown in Fig-2 and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal. The SSASPL updates the data with three N-MOS transistors and it holds the data with four transistors in two cross-coupled inverters. It requires two differential data inputs (D and Db) and a pulsed clock signal. When the pulsed clock signal is high, its data is updated. The node Q or Qb is pulled down to ground according to the input data (D and Db). The pull-down current of the N-MOS transistors must be larger than the pull-up current of the P-MOS transistors in the inverters.

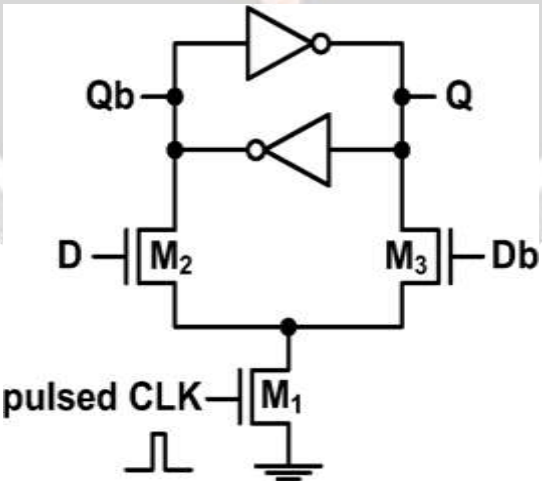

Fig -2: Simple diagram of a Static Differential Sense Amplification Shared Pulsed Latch

SSASPL is one of the smallest pulsed latch as compare to others pulsed latches as shown in table-1. Conventional SSASPL used 9 transistors but in this one inverter is removed and hence only 7 transistors are used.

Table -1: Number of transistors used in various pulsed latch designs

		Total number of transistors	Number of transistors connected to clock
Pulsed latch	**SSASPL**	**7**	**1**
	TGPL	10	4
	HLFF	14	2
	CP3L	26	6
Flip-flop	**PPCFF**	**16**	**8**
	SAFF	18	3
	DMFF	22	5
	CPSA	28	5
	CCFF	28	5
	ACFF	22	4

2.2 PULSED CLOCK GENERATOR

Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator as shown in Fig-3. It consists of a buffer , delay, AND gate and NOT gate. Here the AND gate and NOT gate are designed using GDI technique.

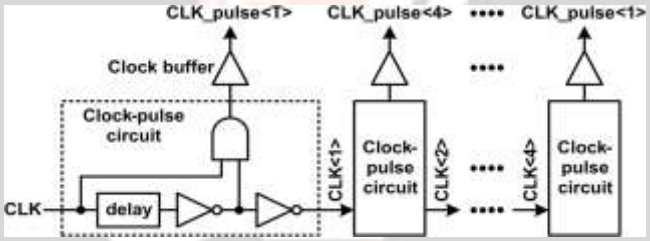

Fig -3: Delayed pulse clock generator

If the pulse clock waveform triggers a latch, the latch is synchronized with the clock similarly to edge-triggered flip-flop because the rising and falling edges of the pulse clock are almost identical in terms of timing. With this approach, the characterization of the setup times of pulsed latch are expressed with respect to the rising edge of the pulse clock, and hold times are expressed with respect to the falling edge of the pulse clock. This means that the representation of timing models of pulsed latches is similar to that of the edge-triggered flip-flop. The pulsed latch requires pulse generators that generate pulse clock waveforms with a source clock. The pulse width is chosen such that it facilitates the transition. Fig-4 shows the waveforms of associated pulse waveform.

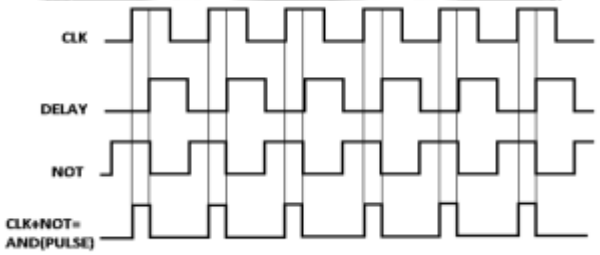

Fig -4: Pulse generator waveform

Fig-5 shows the buffer circuit. Buffer circuit produces an output exactly same as the input. Table-2 shows the truth table of the buffer circuit.

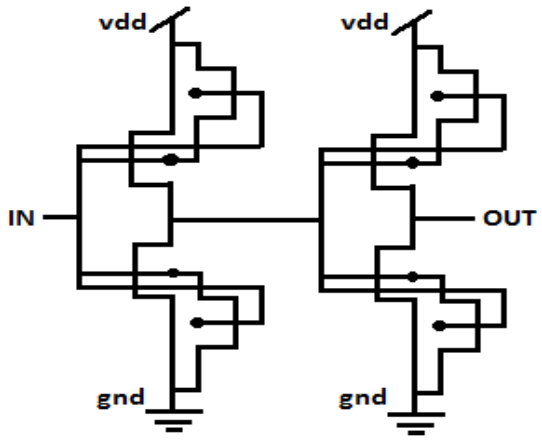

Fig -5: Buffer gate schematic

Table -2: Truth table of Buffer gate

INPUT	OUTPUT
0	0
1	1

Fig-6 shows the delay circuit. Delay circuit sets back the input by some period of time.

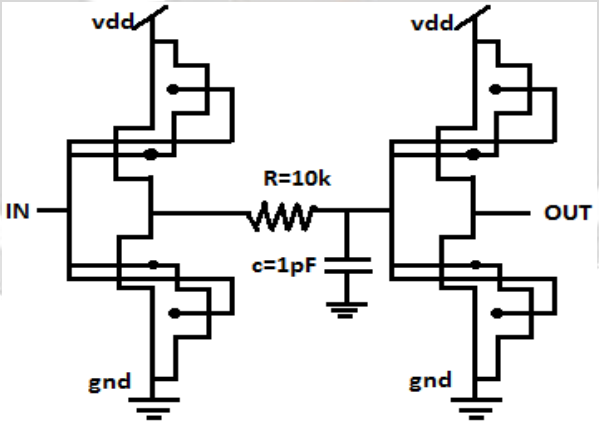

Fig -6: Delay gate schematic

2.3 GDI

GDI (Gate Diffusion Input) is a new technique of low power digital circuit design. The basic GDI cell contains 3 inputs G (common gate input of N-MOS and P-MOS), P (input to the drain/source of P-MOS) , N (input to the source/drain of N-MOS). This technique allows the reduction of power consumption, delay and area of digital circuits, while maintaining low complexity of logic design. The advantage of GDI technique is the 2-transistor implementation of complex logic functions and in-cell swing restoration. Using this technique each AND and NOT

gate can be designed using only 2 transistors alone. The Fig-7 shows the basic cell of GDI. The table-3 shows the comparison of transistor count in GDI and static CMOS.

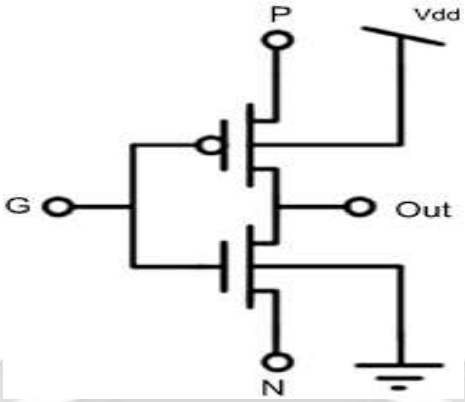

Fig -7: Basic GDI cell

Table -3: Comparison of transistor count in GDI and static CMOS

FUNCTION	GDI	CMOS
INVERTER	2	2
OR	2	6
AND	2	6
MUX	2	12
XOR	4	16
XNOR	4	16
NAND	4	4
NOR	4	4

The AND gate circuit designed using GDI technique is shown in Fig-8 and its truth table is shown in table-4.

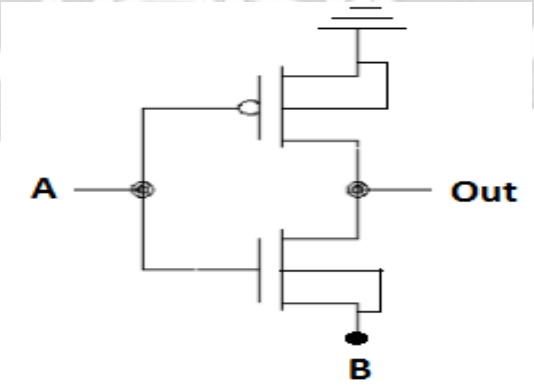

Fig -8: AND gate schematic using GDI technique

Table -4: Truth table of AND gate

A	B	OUTPUT
0	0	0
0	1	0
1	0	0
1	1	1

The NOT gate circuit designed using GDI technique is shown in Fig-9 and its truth table is shown in table-5.

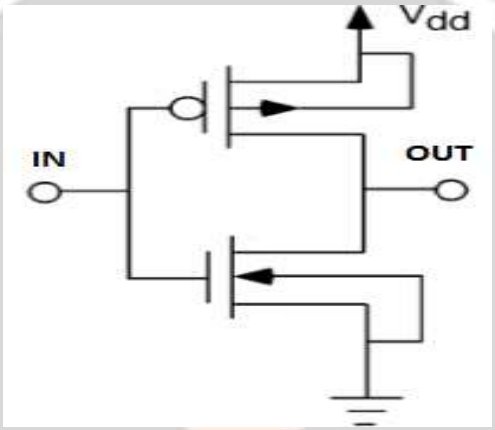

Fig -9: NOT gate schematic using GDI technique

Table -5: Truth table of NOT gate

INPUT	OUTPUT
0	1
1	0

2.4 MTCMOS TECHNIQUE

The MTCMOS is used as a power gating technique, to reduce the power consumption in a circuit. The P-MOS sleep transistor is used to switch V_{dd} supply and hence is called a "header switch". The N-MOS sleep transistor controls V_{ss} supply and hence is called a "footer switch". The circuit diagram of MTCMOS technique is shown in Fig-10. Low V_{th} devices switch faster, and are therefore useful on critical delay paths to minimize clock periods. The penalty is that low V_{th} devices have substantially higher static leakage power. High V_{th} devices are used on non-critical paths to reduce static leakage power without incurring a delay penalty. Typical high V_{th} devices reduce static leakage by 10 times compared with low V_{th} devices.

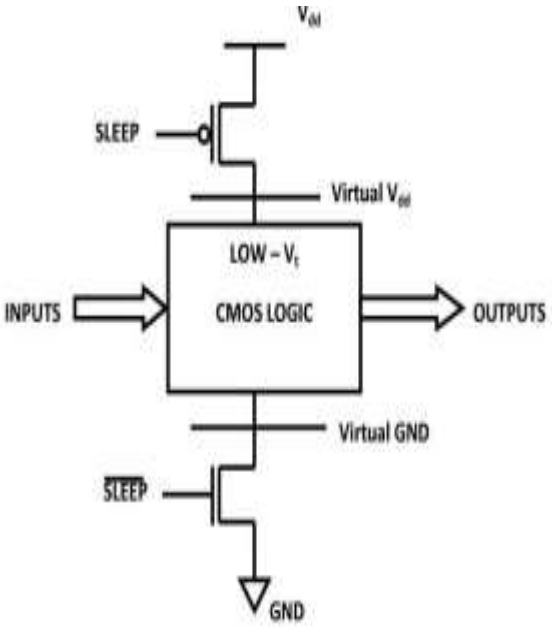

Fig -10: Multi-threshold Complementary Metal Oxide Semiconductor

The most common implementation of MTCMOS for reducing power makes use of sleep transistors. Logic is supplied by a virtual power rail. Low V_{th} devices are used in the logic where fast switching speed is important. High V_{th} devices connecting the power rails and virtual power rails are turned on in active mode, off in sleep mode. High V_{th} devices are used as sleep transistors to reduce static leakage power. The design of the power switch which turns on and off the power supply to the logic gates is essential to low-voltage, high-speed circuit techniques such as MTCMOS. The speed, area, and power of a logic circuit are influenced by the characteristics of the power switch. In a "coarse-grained" approach, high V_{th} sleep transistors gate the power to entire logic blocks.

The sleep signal is de-asserted during active mode, causing the transistor to turn on and provide virtual power (ground) to the low V_{th} logic. The sleep signal is asserted during sleep mode, causing the transistor to turn off and disconnect power (ground) from the low V_{th} logic. The drawbacks of this approach are that logic blocks must be partitioned to determine when a block may be safely turned off (on),sleep transistors are large and must be carefully sized to supply the current required by the circuit block an always active (never in sleep mode) power management circuit must be added.

3. RESULTS AND DISCUSSIONS

The comparison between the flip flop based shift register design, pulsed latch based shift register design without using MTCMOS and GDI techniques and pulsed latch based shift register design using MTCMOS and GDI technique is provided in Table-6. The number of transistors used in pulsed latch based shift register design using MTCMOS and GDI technique is nearly half of those used in flip flop based shift register design, the average power consumption and the delay value is also considerably reduced.

The reduction in the number of transistors used is due to usage of SSASPL and GDI techniques for latch and logic gates design respectively.

Table -6: Comparison of various parameters between the different shift register design

Parameters	Flip flop based shift register design	Pulsed latch based shift register design without using MTCMOS and GDI techniques	Pulsed latch based shift register design using MTCMOS and GDI techniques
Number of transistors	464	270	232
Average power consumed	147.8µW	95.24µW	18.42Mw
Delay	0.262µs	0.112µs	0.033µs

4. CONCLUSIONS

In the pulsed latch based shift register designed using MTCMOS and GDI techniques the number of transistors used is reduced by 232, the average power consumption is reduced by 87.53% and the delay is reduced by 87.43% when compared to conventional flip flop based shift register design. When compared pulsed latch based shift register designed without using MTCMOS and GDI techniques the number of transistors used is reduced by 38, the average power consumption is reduced by 80.66% and the delay is reduced by 70.68%.

5. REFERENCES

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