PERFORMANCE IMPROVEMENT TECHNIQUE IN DIVIDE-BY-2/3 COUNTER USING STATIC FLIP-FLOP

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ABSTRACT

In modern low power VLSI Circuits, the power consumption is a very important and critical task for their applications. Optimization of the power at the logic level is one of the most important tasks to minimize the power. Hence, the power consumption and performance has been analyzed for counter design. Here, the number of transistors used has been reduced. In the previous design, an AND gate is used in the counter design, that produces the delay in the Flip-flop. In the proposed design, to increase the performance of the counter, the AND gate is replaced by switching transistors to reduce the delay and also shows better power consumption, less number of transistors are used and it is simulated using Tanner EDA.

Keywords: *Static FlipFlop Divide-By-2/3 Counter*

I INTRODUCTION

In a digital design basic storage elements are Flip- flops (FFs) .In particular, digital designs now a day often adopt intensive pipelining techniques and employ many FF modules such as register file, shift register. Various techniques are used in previous designs such as LFSR Dynamic logic, Transmission gate logic, Circuit shared static logic, Pass Transistor logic,C^2 MOS logic. Two types of MOS transistor PMOS and NMOS are invented and used for designing integrated circuits. Both types have very high static power consumption. This problem is solved if and only logic designed in such a way that it consumes no power in the static state. After decades, Frank Wanlass introduced a new logic designed using two complementary p-type and n-type MOSFETs. Two main advantages of CMOS technology are high noise immunity and very low static power consumption. The last several decades have seen the innovation of new CMOS technologies with excellent features. Innovations of new technologies are very important for the downsizing of CMOS integrated circuits.

A simple and correct technique for the timing analysis of gates that involve pass-transistor logic was introduced. In High speed and low power circuit design, more popular design are based on Pass transistor logic (PTL) and especially Complementary Pass-Transistor logic (CPL). There are many drawbacks in all these methods, in order to overcome this we are going to implement flip flop using divide- by-2/3 counter. Divide-by-2/3 counter operates with a pair of division ratios. It includes a switching circuit to switch from a higher division to lower division. It suffers from the disadvantage of large load capacitance. In the proposed design, to overcome this, a new technique has been designed.

Static Flip-Flops:

Static logic is one which does not require a clock. The output will be there as soon as the inputs are probed (without considering the propagation delay on the gate).The static input latch provides first and second intermediate complementary outputs on first and second intermediate output terminals respectively. A storage element responsive to static input signals which generates complementary static output signals and incorporates scan test logic. Static flip-flop is used for high speed and low power application.

True Single Phase Clock Latch:

The true single phase clock is a common dynamic flip-flop which performs the flip-flop operation with little power and at high speeds. As a true single phase clocking flip-flop design has a small area and low power consumption. The most modern synchronous circuit uses only a single phase clock i.e., they transmit all clock signals on one wire. The dynamic logic circuits have both minimum and maximum clock periods. The time between clock edges can widely vary from one edge to the next and back again. Such digital devices work just as well with the clock generator that dynamically changes its frequency. Prescalar is typically used at a very high frequency to extend the upper frequency range of frequency counters, phase locked loop (PLL) synthesizers, and other counting circuits. When used in conjunction with a PLL, a prescalar introduces a normally undesired change in the relationship between the frequency step size and phase detector comparison frequency. A counter is a device which includes a predefined state based on the clock pulse applications. Generally, counters are designed by flip-flop arrangement which can be the synchronous mode or asynchronous mode of operation basis.

II SURVEY BACKGROUND

Peiyi Zhao, Jason McNeely, Weidong Kuang, Nan Wang, and Zhong Feng Wang[3] suggested that power consumption is a major bottleneck of system performance. In Sequential Elements design, a power is consumed by the clock system which is made of the clock distribution network and flip-flop. They proposed novel clocked pair shared flip-flop which reduces the number of local clocked transistors by approximately 40%.

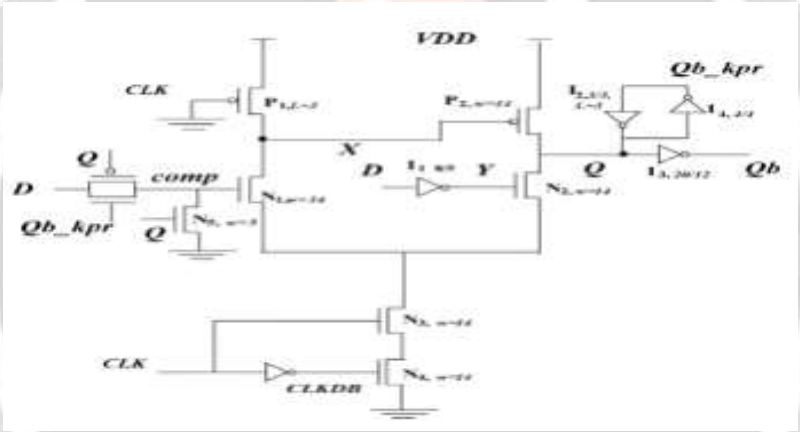


Figure 1. CMOS True-Single-Phase-Clock Dividers

Z.Deng and A.M.Niknejad [4]suggested that a true-single-phase-clock (TSPC) divider synthesis technique that is based on the general TSPC logic family. According to this united technique, various types of TSPC dividers are compared in terms of the speed–power trade-off. The newly proposed RE-2 type has shown a better balance between speed and power performance than other types. The measurement results of a prototype design in a 65 nm LP CMOS technology show that the maximal input frequencies can be 19 GHz and 16GHz for a divide-by-2 divider and a divide-by-2/3 prescaler respectively, and the power consumption is less than 0.5 mW.

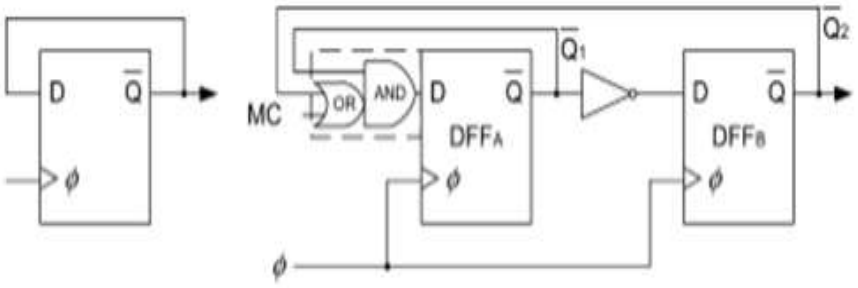


Figure 2. Divide-By-2/3 Prescaler

Xiao Peng Yu, Manh Anh Do, Wei Meng Lim, Kiat Seng Yeo, and Jian-Guo Ma [7] suggested that the power consumption and operating frequency of the extended true single-phase clock (E-TSPC)-based frequency divider is investigated. In this research short-circuit power and the switching power are calculated and simulated. They proposed low-power divide-by-2/3 prescaler using CMOS technology and implemented and 25% reduction of power consumption is achieved.

III-EXISTING METHOD

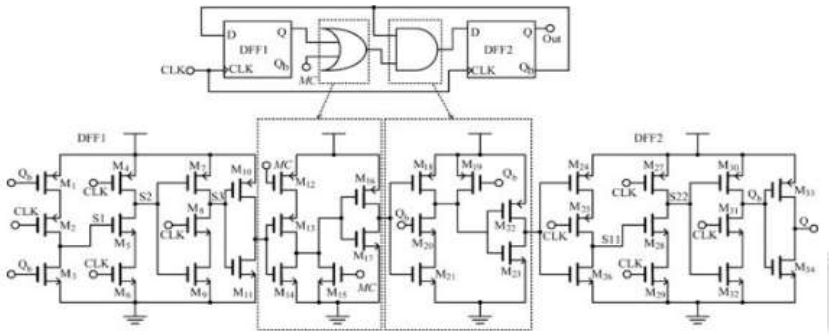


Figure 3: Basic CMOS Circuit

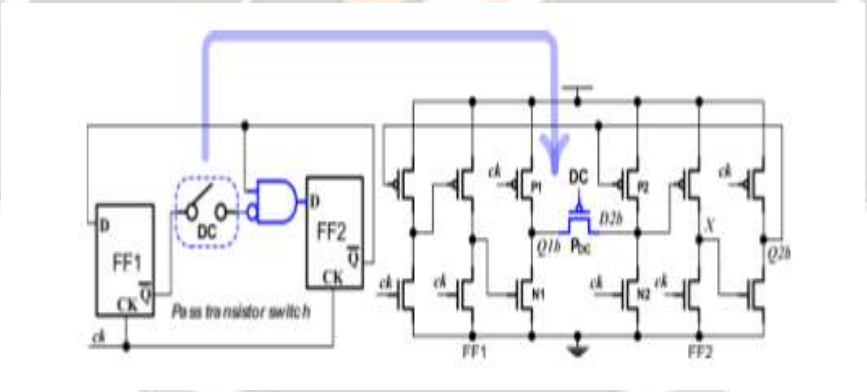


Figure 4: Switch Based Circuit

The two FFs, the AND gate and the OR gate are common in previous designs. Here A switch is doing the OR operation for the divide control. There is a negation bubble at one of the AND gate's input. The complemented output is fed to FF2. When the switch is open, the input from FF1 is disconnected and FF2 alone divides the clock frequency by 2. The divide control signal controls the function of PMOS transistor, when a Dc input logical 1 mean the PMOS transistor in an off state and if DC input logical 0 mean transistor in ON state in this condition the output of FF1 is connected with the output node of the 1st stage inverter of FF2. When the clock signal in a rising edge, then the output of the inverters is pre-discharged to zero. So that in the meantime D-Latch holds the output. When the clock signals in a falling edge, then inverters enter the evaluation phase and the D-latch becomes a pseudo-NMOS inverter to admit the evaluation result from the preceding inverter.

IV-PROPOSED DESIGN

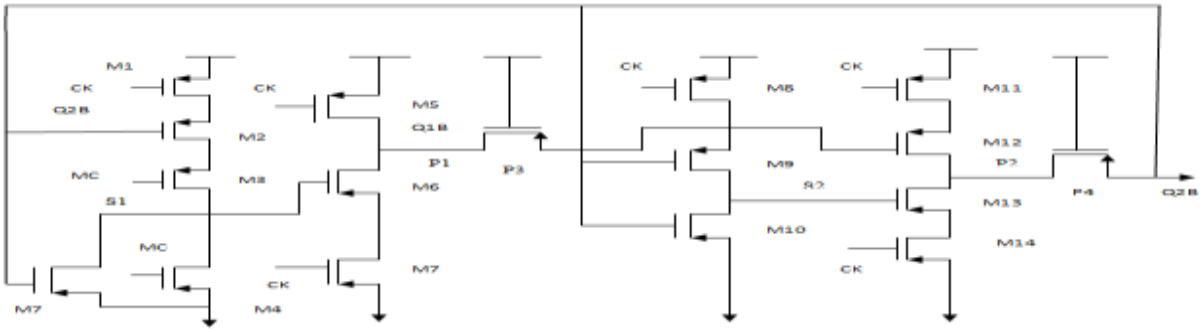


Figure 5: Reduced Stage Prescaler Circuit

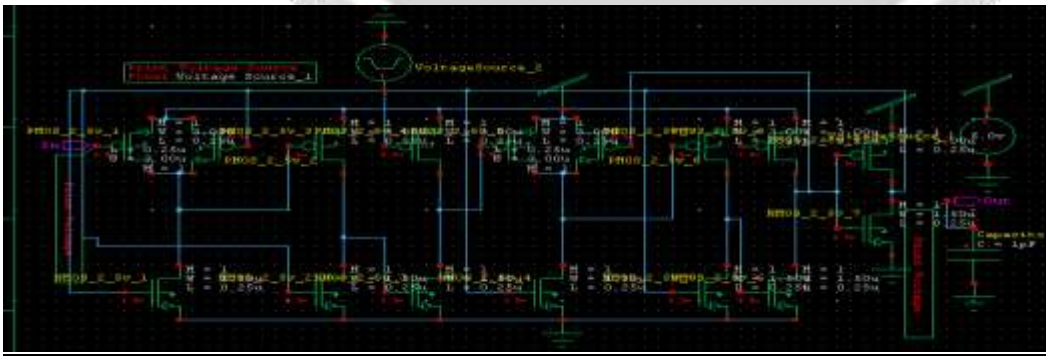
When the modulus control signal MC is low, the proposed pre scalar is set to be in the divide-by-3 mode. At times t1, when CK turns from high to low, the first stage of DFF2 samples the input data and charges the node S2. When the clock CK turns high at time t2, the node P2 evaluates the data, the voltage at node P2 is discharged through the transistors M14 and M11, then the DFF2 output Q2B toggles from low to high, and the DFF1 output Q1B also turns from low to high. At timing t3, when the negative cycle of the clock arrives, the node P2 should be charged with high While the output Q1B of the flip-flop DFF1 is high at this time, the transistor M12 is turned off by Q1B. The precharge operation of the second stage of DFF2 is stopped, the voltage at node P2 keeps low until the next falling edge of the clock. At times t4, the voltage at node Q1B turns, thus the node of P2 is charged to high again at times t5.When the rising edge of the clock CK comes at times t6, the output Q2B turn low, and a divide-by-3 operation is completed. The key points of the divide-by-3 operation are that the control signal Q1B should turn off the transistor M12 to prevent the node P2 being charged too high before the negative cycle of the clock signal. In this design the of total number stages gets reduced in prescaler so that the switching power in the divide-by-3 mode is also reduced. The inverter between the flip-flop DFF1 and DFF2 of the conventional TSPC 2/3 prescaler is eliminated. The load capacitance of DF1 is essentially reduced compared with the conventional TPSC divide-by-3 circuit.

V-SIMULATION RESULTS

EXISTING METHOD 1

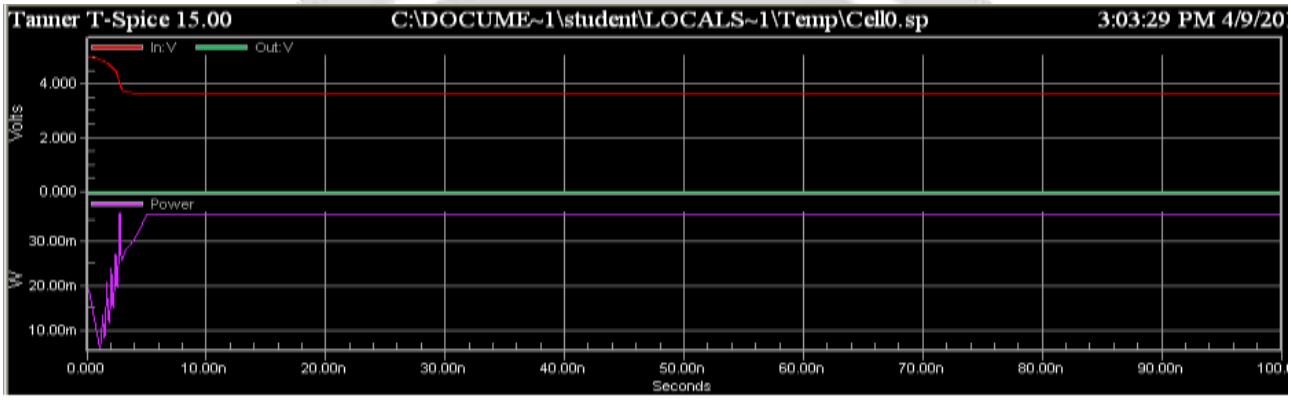
A 13.5-mW 5-GHz frequency synthesizer with dynamic-logic frequency divider

SCHEMATIC:



SIMULATION RESULT IN SECONDS

SIMULATION RESULT IN NANO SECONDS



Supply voltage 5v
Obtained voltage 4.5v

POWER CONSUMPTION RESULTS:

VVoltageSource_1 from time 0 to 1e-007
Average power consumed -> 2.589387e
Max power 3.997390e-002 at time 2.77498e-009
Min power 4.771656e-003 at time 1.0399e-009

TIME RESULTS:

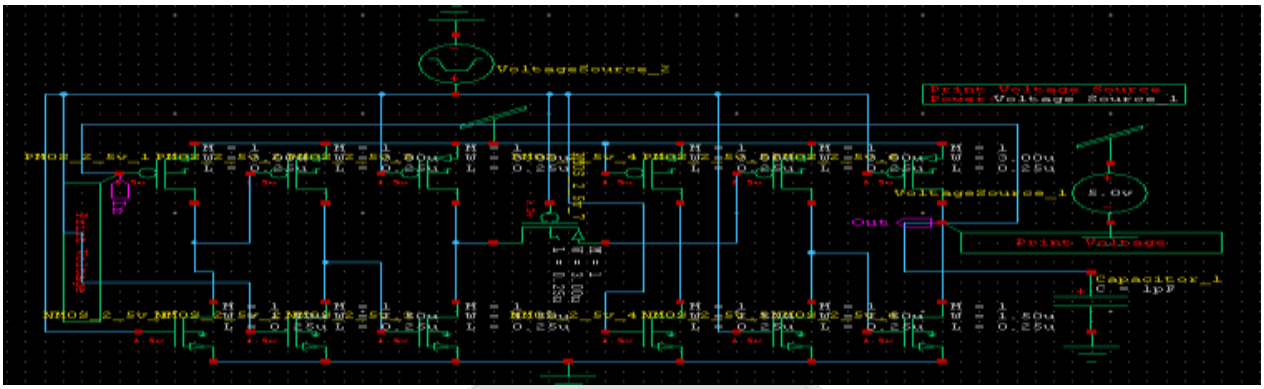
Parsing	0.02 seconds
Setup	0.01 seconds
DC operating point	0.11 seconds
Transient Analysis	0.14 seconds
Overhead	0.42 seconds

Total	0.70 seconds

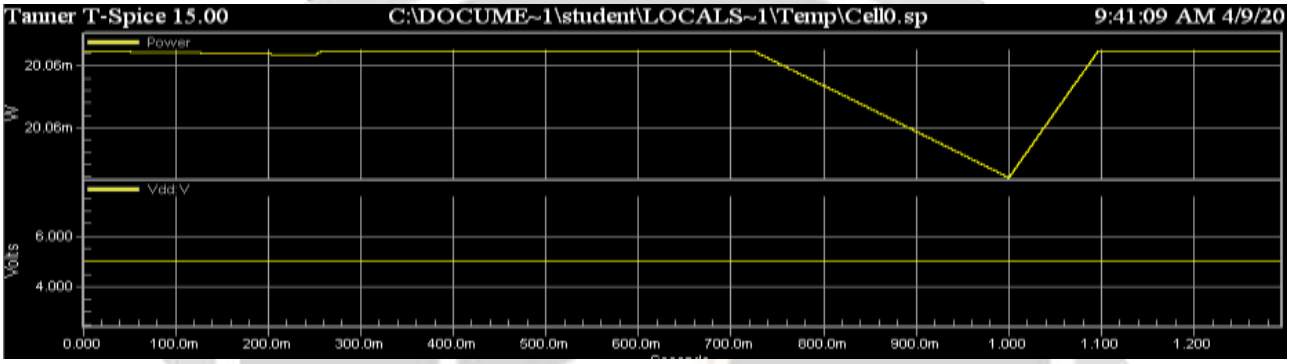
EXISTING METHOD 2

Low Voltage and Low Power Divide-By-2/3 Counter Design Using Pass Transistor Logic Circuit Technique

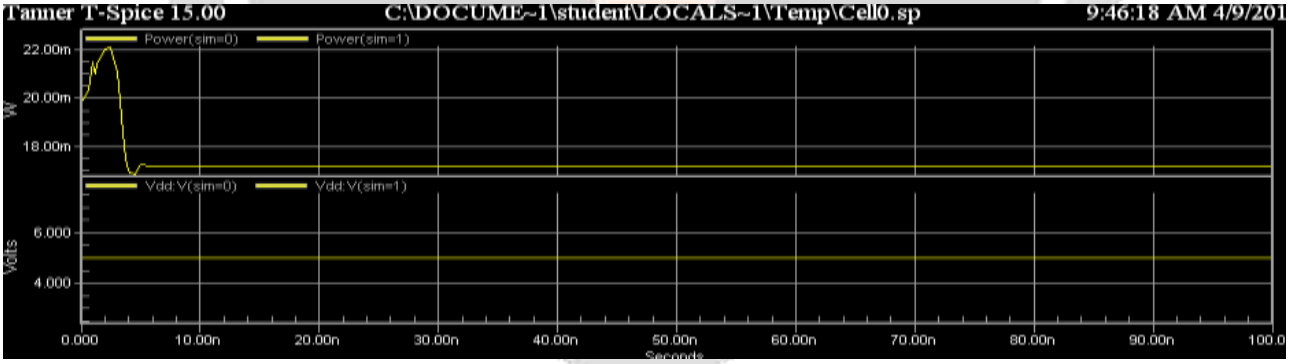
SCHEMATIC



SIMULATION RESULT IN SECONDS



SIMULATION RESULT IN NANO SECONDS



Supply voltage 5v
Voltage obtained 4.8v

POWER CONSUMPTION RESULTS:
VVoltageSource_1 from time 0 to 1e-007
Average power consumed->1.734997e
Max power 2.200186e-002 at time 2.49458e-009
Min power 1.673205e-002 at time 4.57862e-009

TIME RESULTS

Parsing	0.00 seconds
Setup	0.02 seconds

DC operating point	0.05 seconds
Transient Analysis	0.14 seconds
Overhead	0.43 seconds
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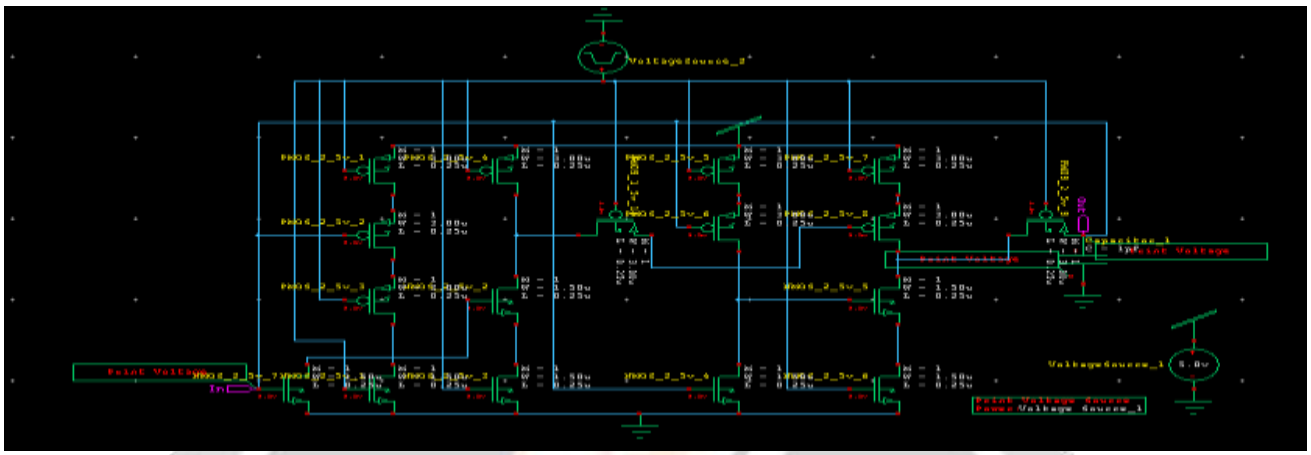
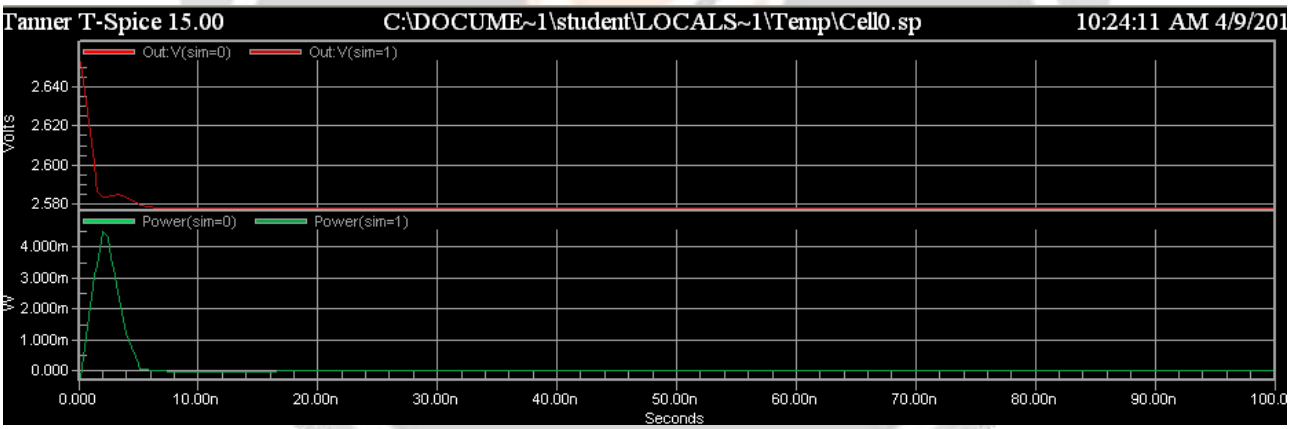
Total	0.64 seconds

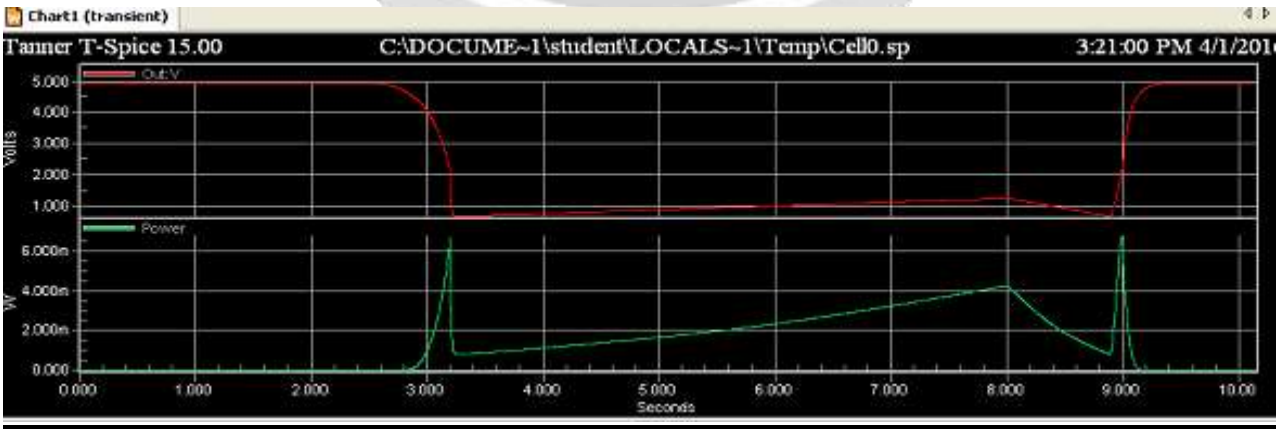
PROPOSED METHOD



SIMULATION_RESULT (SECONDS)



SIMULATION_RESULT IN NANO SECONDS



Supply voltage 5v
Obtained voltage 4.9v

POWER CONSUMPTION RESULTS:

VVoltageSource_1 from time 0 to 1e-007
Average power consumed->1.018356e-004W
Max power 4.359328e-003 at time 1.99051e-009
Min power 2.632879e-009 at time 0

TIME RESULTS:

Parsing	0.00 seconds
Setup	0.01 seconds
DC operating point	0.11 seconds
Transient Analysis	0.09 seconds
Overhead	0.28 seconds

Total	0.39 seconds

COMPARISON TABLE FOR RESULTS

PARAMETERS	EXISTING METHOD 1	EXISTING METHOD 2	PROPOSED METHOD
NO OF NMOS TRANSISTORS	9	8	7
NO OF PMOS TRANSISTORS	9	9	8
AVERAGE POWER CONSUMPTION(using Tanner EDA)	2.589387e	1.734997e	1.018356e
TIME CONSUMED	0.70s	0.64s	0.45s
SCALING(5V)	4.3V	4.6V	4.9V

CONCLUSION

Thus our project accomplishes the goal of high speed and low power consumption by implementing effective counter designs using Flip-flops. The reduction in the number of transistors in the circuit leads to reduced area and thus power consumption and switching delays also reduces. This kind of design has been implemented using Tanner EDA, which makes it a powerful tool in circuit design. The simulation results demonstrate the high speed and low power properties of this proposed pre-scalar.

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