.

Performance Analysis of different MUX for FPGA

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ABSTRACT

A Field-Programmable Gate Array is an FPD featuring a general structure that permits very high logic capacity. FPGAs offer higher ratio of flip-flops to logic resources than do CPLDs. The main problem is power dissipation than speed and area.

In this paper, the primary and important issue within the low power MOSFET circuit is power dissipation. The methods we use for reducing power and energy dissipation in conventional CMOS circuit comprise reducing the power supply voltages and the nodes, capacitances or switch activities with efficient charge recovery logic. This paper also determine with multiplexer to improve the ability and design a 2:1, 4:1 and 8:1 multiplexer with CMOS transistor. All the results of this paper are simulated on SYMICA tool realized in 22nm and 32nm technology.

Keyword: - *CMOS, LUT, 2:1Multiplexer, 4:1Multiplexer, 8:1 Multiplexer*

1. INTRODUCTION

Due to the restricted power supplied by the batteries, the circuitry cover in this device must be designed to consume less power. Also power dissipation requires exclusive and noise preserve machinery, batteries and power conservation circuits. Multiplexer is significant component digital design [1]. Look up table are used in performing combinational logic circuits in a static random access memory(SRAM) based field programmable gate arrays(FPGA)[2].The electronic device circuit is typically accustomed to mix two digital signal on to single line, by placing them at completely different times. it can be referred to as time division multiplexing it may be used as PLD [3].Multiplexer mainly use to increase the amount of data that can be sent over the network within certain amount of time and bandwidth[4].

2. LITRATURE SURVEY

A logic style is the way how a logic function is resultant from a set of transistors. It disturbs the speed, size, and power consumption, wiring density of a circuit[2013].The authors have suggested a 4:1 MUX using PFAL and ECRL adiabatic logic design technique and compared with the Conventional CMOS Multiplexer. The basic methods

that we used for reducing energy or power dissipation in conventional CMOS circuits include varying the rise time and full time, on reducing frequency and minimize then switching activities with capable charge recovery logic[2014].The repeated decrease in feature size of CMOS circuits and corresponding increase in chip density and in operation frequency have made power consumption a significant concern in VLSI design[2012].The low power consumption is the primary critical problem within the system SOC design completely different techniques and technologies for low power design in high speed[2013].The choice technique for reducing power dissipation is by the implementation of the adiabatic logic[2013].

3. PROCESS FLOW

3.1) 2:1 MUX implementation:

A two-to-one-line multiplexer connects one of two 1-bit sources to a common destination. The circuit has two data input lines, one output line, and one selection line S. When S = 0, the upper AND gate is enabled and I0 has a path to the output. When S = 1, the lower AND gate is enabled and I1 has a path to the output. The multiplexer acts like an electronic switch that selects one of two sources.

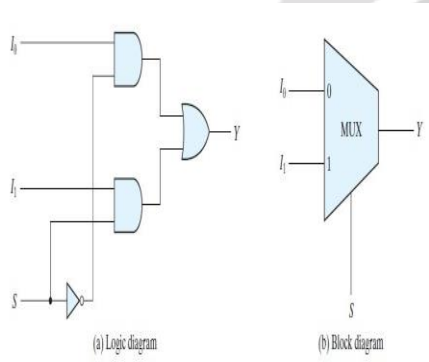


Figure 3.1.1) Logic diagram of 2:1 MUX

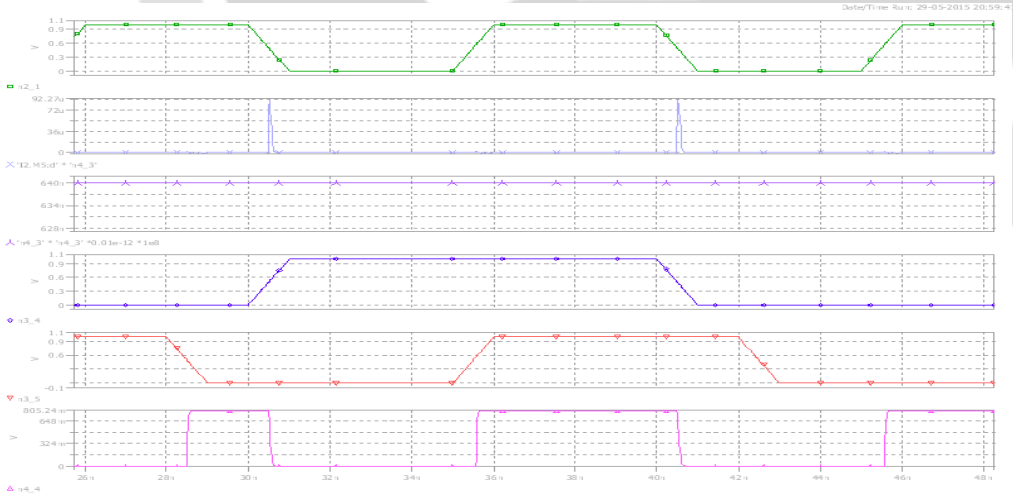
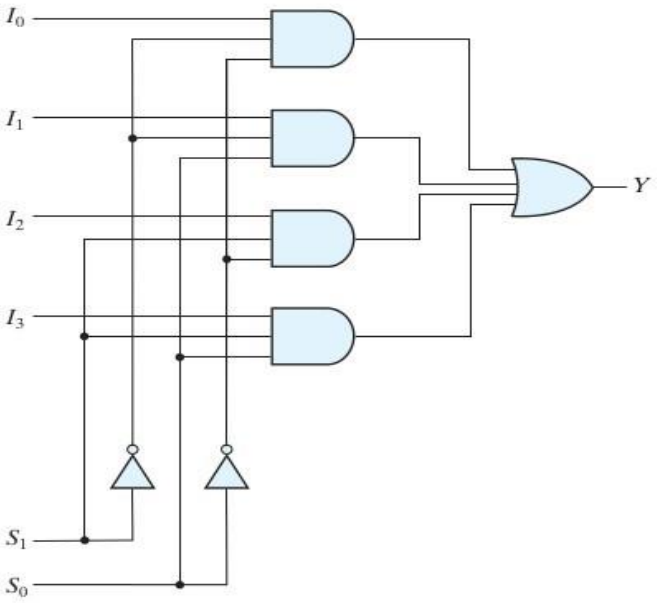


Figure 3.1.2) Waveformof 2:1MUX at 1V

3.2) 4:1 MUX implementation:

The 4:1 Mux is made by using four 3-input AND gate and one 4-input OR gate. The select lines are constructed with the help of inverters. These gates have been constructed on 22nm length. When the enable input is in the inactive state, the outputs are disabled, and when it is in the active state, the circuit functions as a normal multiplexer.



(a) Logic diagram

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

(b) Function table

Figure 3.2.1) Logic diagram of 4:1 MUX

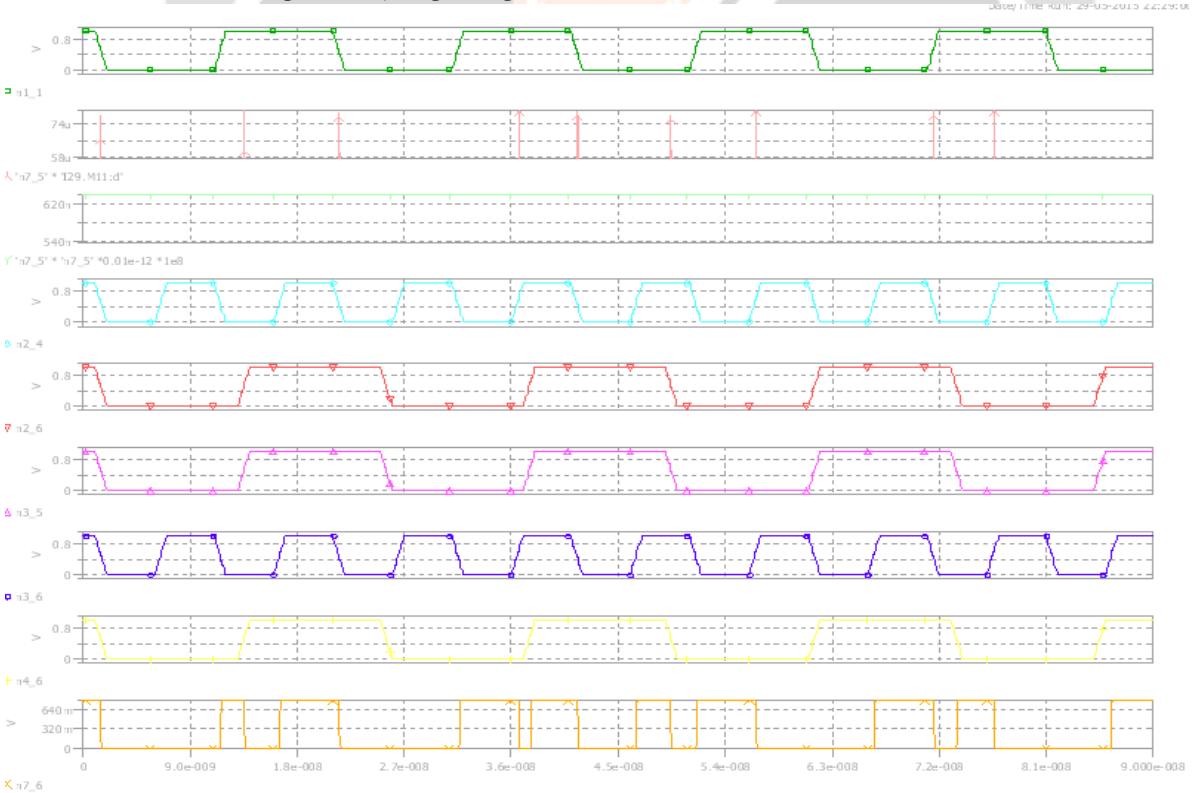


Figure 3.2.2) Waveform of 4:1 MUX at 1V

3) 8:1 MUX implementation:

The 8:1 Mux is made from eight 3-input AND gates.The output of these gates is given to ORgate.Further the output of the OR gate is given to the 4-input OR gate.

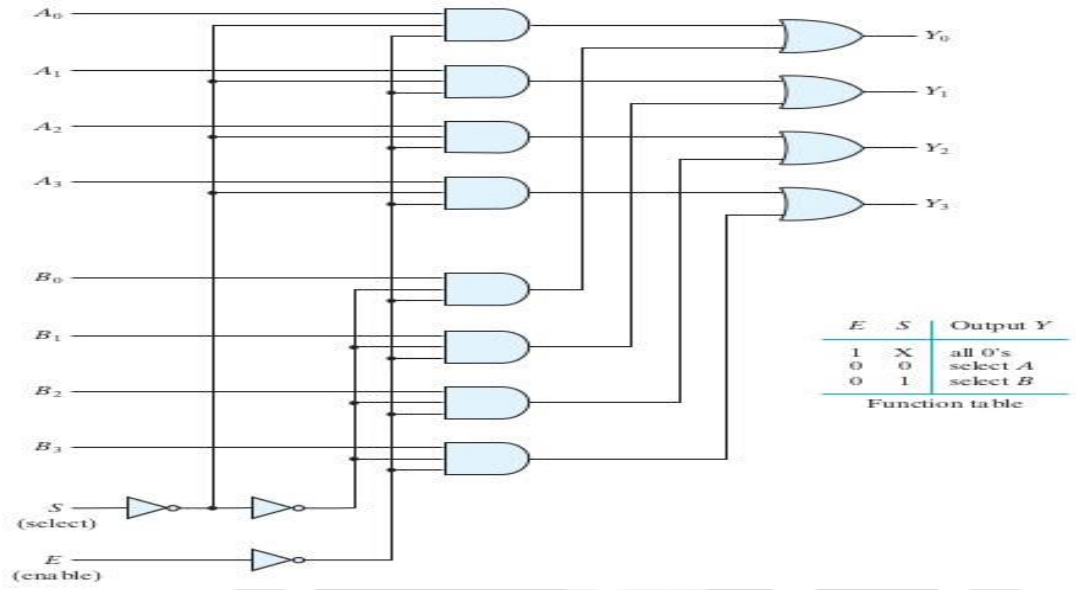


Figure 3.3.1) Logic diagram of 8:1 MUX

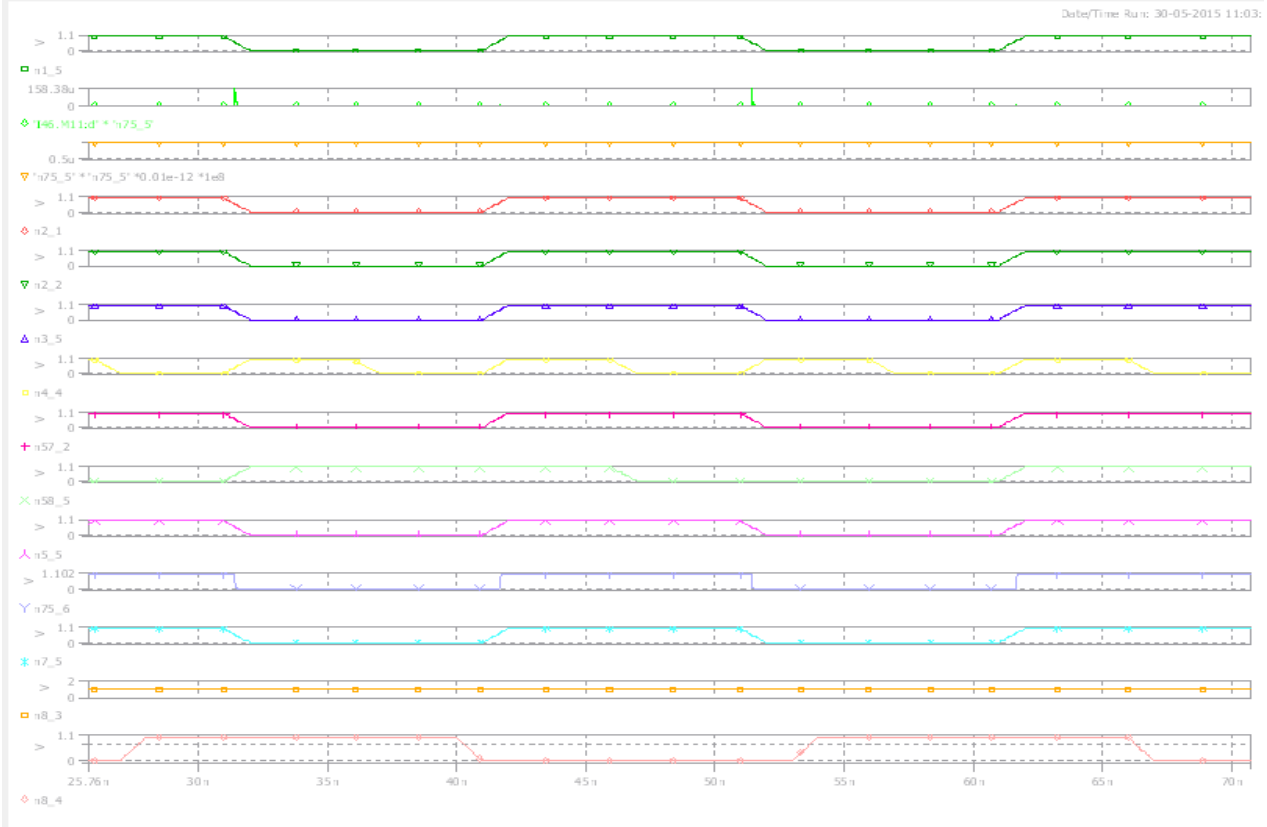


Figure 3.3.2) Waveform of 8:1MUX at 1V

4. CALCULATED RESULTS

4.1 Calculation of Total power:
The tool is flexible, in that it can be used to estimate power in a wide variety of FPGA architectures. It is fast, in that estimates can be obtained without the time-consuming computation of programs such as SymicaDE, or the reliance on simulations.
The total power is sum of Static power And Dynamic power.
Total Power = Static Power + Dynamic power.

4.1.1. Dynamic power:
Dynamic power is a result of signal transitions between logic-0 and logic-1.The dynamic power consumption is generally modeled as below: voltage swing and clock frequency of the resource i, respectively. The total dynamic power consumed by a device is the summation of the dynamic power of each resource.
$\mathbf{P_{(Dynamic)} = \sum V_{dd}^2 .C .F_{clk}}$
Where C, V_{dd} and F_{clk} represent capacitance, the voltage swing, and clock frequency of the resource i, respectively.
The total dynamic power consumed by a device is the summation of the dynamic power of each resource.

4.1.2. Static Power:
Static power is the product of Drain current and V_{dd}
$\mathbf{P_{(Static)} = V_{dd}.I_d}$

5. Results

5.1) Result for 32nm:

Parameter	2:1 MUX			4:1MUX			8:1 MUX		
Voltage (V)	1	0.9	0.8	1	0.9	0.8	1	0.9	0.8
Static Power	176.99 uW	130.5 uW	91.28 uW	159.47 uW	117.15 uW	80.59 uW	157.39 uW	177.92 uW	80 uW
Dynamic Power	175 pW	810 nW	639.9nW	1.01 uW	810 nW	640 nW	1.15 uW	810 nW	630 nW
Total Power	176.99 uW	131.3 uW	91.91 uW	160.48 uW	117.96 uW	81.23 uW	158.54 uW	178.7 uW	80.63 uW

5.2) Result for 22nm:

Parameter	2:1 MUX			4:1MUX			8:1 MUX		
Voltage (V)	1	0.9	0.8	1	0.9	0.8	1	0.9	0.8
Static Power	143.18 uW	105 uW	72.99 uW	130.54uW	96.05 uW	64.34 uW	127 uW	97.15 uW	66 uW
Dynamic Power	0.99 uW	815.8nW	640 nW	1.01 uW	815.6 nW	637.38 nW	0.99 uW	815 nW	640 nW
Total Power	144.17 uW	105.8 uW	73.63 uW	131.55 uW	96.86uW	64.97 uW	127.9 uW	97.96 uW	66.64 uW

6. CONCLUSIONS

In this work performance of different MUX is discussed. We propose and discussed basic Static and dynamic power and studied by simulation of 2:1, 4:1and 8:1mux.The comparison of the power dissipation of above mux is carried by varying the $V_{dd.}$ Different mux designs are simulated and compared and compared proposed multiplexer in terms of power consumption and drain voltage at frequency of 100 MHz. The minimum power dissipation in 4:1 mux at 32nm is 64.97uW is obtained at Vdd=0.8V and minimum power dissipation in8:1 mux at 22nm is 80.63 uW is obtained at Vdd=0.8 at 22nm.

7. REFERENCES

[1] Richa Singh and Rajesh Mehra, "Power efficient design of Multiplexer". International Journal of Advances in Engineering & Technology, Mar. 2013.

[2] Gurpreet Kaur, Narinder Sharma, "Design and analysis of 4:1 multiplexer using an efficient reversible logic in 180nm," International Journal of Computer Techniques (IJCT), Vol.1 Issue. 2 Dec – 2014.

[3] Haider A.F. Almurib and T. Nandha Kumar "A Memristor-Based LUT for FPGAs," Proceedings of the 9th IEEE International Conference on Nano/Micro Engineered and Molecular Systems: April 13-16, 2014, Hawaii, SA.

[4] Aron and Shelly Garg, "Power Efficient Mux Based Decoder," Proceedings of the 9th IEEE International Conference on Nano/Micro Engineered and Molecular Systems. International Conference on Computing, Communication and Automation .pp. 145-170 (2015 IEEE 1010).

[5] Abhishek Dixit **"**Power Optimization of 8:1 MUX," International Journal of Computer Applications, 0975 – 8887.Volume 99– No.5, pp.75-79 August 2014.

[6] Said Hamdioui, Mottaqiallah Taouil, and Nor Zaidi Haran, "Testing Open Defects in Memristor-Based Memories". Volume 90– No.5, pp.175-279 August 2014.

[7] Xu, X. Dong and Y. Xie "Design Implications of Memristor-Based RRAM Cross-Point Structures" 1 C. were supported in part by NSF grants 0702617, 0903432, 0905365, and SRC grants, pp.507-510 April, 2014.

[8] P. S. Nair , S. Koppa , and E. B. John "Topology selection of FPGA look-up tables for low leakage operation ,"P. S. Nair, S. Koppa, and E. B. John in European Conference on Circuit Theory and Design, pp.73-76, Aug 2009.

[9] Sandeep S. Nair, Santosh Koppa, Eugene B. John "A comparative analysis of coarse-grain and fine-grain power gating for FPGA lookup tables,"52nd IEEE International Midwest Symposium on Circuits and Systems, pp.507-510, 2009.

[10] Mostafizur Rahman, Mingyu Li, Jiajun Shi, Santosh Khasanvis, and C. Andras Moritz, "A New Tunnel-FET based RAM Concept for Ultra-Low Power Applications," in Proceedings of 2014 IEEE/ACM International Symposium on Nano scale Architectures (NANOARCH) - pp.150-208, Paris, France. 2014.

[11] International Technology Roadmap for Semiconductors, (SIA), 2013 edition of ITRS, http://public.itrs.net.

[12] B.H. Calhoun, A. Wang, and A. Chandrakasan, "Modeling and sizing for minimum energy operation in subthreshold circuits," IEEE J. Solid-State Circuits, vol. 40, no. 9, Sep 2014.

[13] K. K. W. Poon, S. J. E. Wilton, and A. Yan. A detailed power model for field-programmable gate arrays. ACM Trans. Des. Autom. Electron.
System, 10(2):279–302, 2014.

[14] L. Shang, A. S. Kaviani, and K. Bathala. Dynamic power consumption in Virtex-II FPGA family. In FPGA '02: Proceedings of the 2014 ACM/SIGDA tenth international symposium on Field-programmable gate arrays, pages 157–164, 2014.