Review on VHDL based design of convolutional encoder using vedic mathematics and viterbi decoder using parallel processing

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ABSTRACT

Convolution encoder and viterbi decoder are widely used in many communication system due to the excellent error control performance.The convolutional encoder encodes the message and then the encoded bits are generated. The bits which are encoded are again sent to the Viterbi decoder and then decoded output is obtained. Convolution encoder using vedic mathematics which leads to improve delay and faster speed. There are sixteen sutras in Vedic multiplication in which "Urdhva Tiryakbhyam" has been used here because it is most efficient one in terms of speed. Viterbi decoder using parallel processing improves processing speed because trace back and decoder can simultaneously work.

Keywords :- *Convolutional Encoder, Vedic Mathematics, Viterbi Decoder, VHDL.*

1. INTRODUCTION

Convolutional encoding is one of the forward error correction scheme. Error correction technique plays a very important role in communication systems. The error correction technique improves the capacity by adding redundant information for the source data transmission. It provides an alternative approach to block codes for transmission over a noisy channel. Convolutional codes are characterized by code rate and memory of the encoder (n,k,K). The code rate is typically given as n/k, where n is the input data rate and k is output symbol rate.The memory is called the "constraint length" 'K' where the output is a function of the previous K-1 inputs. Convolutional codes were introduced in 1965 by Peter Elias. Convolutional codes are used extensively in numerous application in order to achieve reliable data transfer, including digital video, radio, mobile communication and satellite communication. Convolution encoding is a process of adding redundancy to the information sequence which is going to be transmitted over the channel. Redundancy means introducing some extra symbols to the information sequence so that the output bit pattern generated makes the transmitted data more immune to the noise in the channel. A convolution encoder processes the information serially.

Viterbi decoder is a basic and important block in any Code Division Multiple Access (CDMA). Viterbi decoder uses the Viterbi algorithm for decoding a data which is encoded using a Convolutional Encoder. It performs basically two operations, they are Synchronization and Quantization. Analog signals are quantized and converted into digital signals in the quantization block. The synchronization block detects the frame boundaries of code words and symbol boundaries. The Viterbi decoder receives successive code symbols, in which the boundaries of the symbols and the frames have been identified. The Viterbi decoding algorithm has been classified into hard decision decoding and soft decision decoding. If the received signal is converted into two levels, either zero or one, it is called hard decision. If the input signal is quantized and processed for more than two levels, it is called soft decision. The soft decision decoding is expensive and require large amount of memory than hard decision decoding. The Viterbi Algorithm was developed by Andrew J. Viterbi. Viterbi decoder is used in digital Cellular Phones, satellite Communications, digital Video Broad Casting, digital wireless Transmitters and receivers.

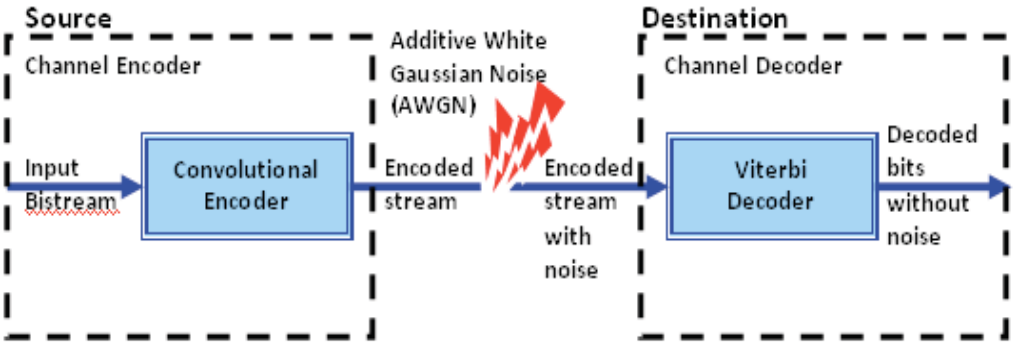

Figure 1. Convolutional encoder and Viterbi decoder [5]

Convolution encoding and viterbi decoding are the most popular because of their powerful coding-gain performance. Convolutional encoder and viterbi decoder is extensively used in a wide variety of devices to reduce transmitted power,decrease the degrading effects of noise in the channel

The multipliers used in convolution encoder are based on vedic mathematics.The word 'Vedic' is derived from the word 'veda' which means the store-house of all knowledge.There are 16 Sutras in Vedic multiplication in which "Urdhva Tiryakbhyam"has been noticed to be the most efficient one in terms of speed. A large number of high speed Vedic multipliers have been proposed with Urdhva Tiryakbhyam sutra. Vedic multiplier is one of the fastest and low power multiplier. This sutra is based on "Vertically and Crosswise"technique. It makes almost all the numeric computations faster and easier. The advantage of multiplier based on this sutra over the others is that with the increase in number of bits, area and delay increase at a smaller rate in comparison to others

2. RELATED WORK

Bineeta Soreng [1] presents the improvement of implementation in terms of area compared to the implementation done in [3]. The Convolution Encoder and Viterbi Decoder have been implemented in Altera DE board. The device taken for the implementation is EP4SGX70HF35C2 of Stratix IV family and design has been simulated using ModelSim 6.6d. It shows area improvement in terms of hardware utilized. The silicon validation is done by programming the FPGA with VHDL code of the proposed structure implementation. There are many techniques and algorithms available for transmission and reception of digital data over noisy channel but Convolution Encoder and Viterbi Decoder are most efficient. It gives improved coding gain and enhanced performance.

Ms.G.S. Suganya [2] presents the realization of an efficient logic design of a crypto system. This design has been simulated in MODELSIM altera 6.6d and synthesized using XILINX-ISE 12.4i. The type of crypto system considered in this paper is convolutional encoder and adaptive Viterbi decoder (AVD) using field programmable gate array (FPGA) technology.The cost for the convolutional encoder and Viterbi decoder are expensive for a specified design because of the patent issue. Therefore, to realize an adaptive Convolutional encoder and Viterbi decoder on a field programmable gate array (FPGA) board is very demanding. In this paper, we concern with designing and implementing a convolutional encoder and Viterbi decoder which are the essential block in digital communication systems using FPGA technology. Convolutional codes offer an alternative to block codes for transmission over a noisy channel. Convolutional coding can be applied to a continuous input stream (which cannot be done with block codes), as well as blocks of data. In crypto system the Convolutional encoder encodes the message and then the encoded bits are generated.The bits which are encoded are again sent to the Viterbi Decoder and then the decoded output is obtained.

V.Kavinilavu [3] presents viterbi decoder uses the Viterbi algorithm for decoding a bit stream that has been encoded using Forward error correction based on a Convolutional code. The maximum likelihood detection of a digital stream is possible by Viterbi algorithm. This is realized using Verilog HDL. It is simulated and synthesized using Modelsim PE 10.0e and Xilinx 12.4i. The Convolutional encoder and Viterbi decoder are implemented using Verilog HDL and the code has been developed under full-custom design. This implementation is complicated when using Verilog HDL compared to VHDL[5]. The Convolutional encoder encodes the given input sequence by modulo-2 adders. The given

input sequence has been encoded by using convolutional encoder and it is transmitted through the channel. Finally, the transmitted sequence is decoded by the Viterbi decoder and the estimated original sequence is produced.

Lei -ou Wang [4] presents a practical method to design a parallel processing Viterbi decoder. It means trace back and decoder can simultaneously work in order to improve the processing speed. The core unit of this design is the TB (Trace Back) and DECODER, which include two function modules. The one is TB that read the information of the survivor paths in the MEMORY. The other is DECODER that computes the output results. These two modules work simultaneously but in different MEMORY address. In this way, the Viterbi decoder is more efficient than a normal one because the DECODER do not need to wait TB. In this way, we can save processing time and memory space. In this design, many units such as ACS, TB and DECODER need parallel processing ability to decrease the computation timing delay, so choosing FPGA for the implementation device is more advisable. From the experimental results, it is clear that the input signal to the convolution encoder is identical to the output signal from the Viterbi decode. So this parallel design of TB and DECODER module meet requirements.

Yin Sweet Wong [5] presents the realization of convolutional encoder and adaptive Viterbi decoder (AVD) using field programmable gate array (FPGA) technology. This paper presents a 4-state, radix-2, hard decision AVD which has the ability to decode adaptively through different trace back length(TL). The performance of the implemented AVD is analyzed by using ISE 9.2 and MATLAB simulations. The AVD is targeted to a Xilinx XCV300PQ240-4 FPGA device for hardware realization. The synthesis results show that the reconfiguration parameter TL of 4 and 15 of AVD implementation has significant difference (>20% improvement) in FPGA device utilization. The results also show that the use of reconfiguration leads to a 28% area occupancy of slice usage improvement over a TL of 15 model compared to a TL of 4 model. All communication channels are subject to the additive white gaussian noise (AWGN) around the environment. Forward error correction (FEC) techniques are used in the transmitter to encode the data stream and receiver to detect and correct bits in errors, hence minimize the bit error rate (BER) to improve the performance. The purposed architecture enforces a simple but highly efficient Viterbi arithmetic unit which helps the device utilization The proposed architecture is focused on the area parameter and decreases it as small as possible. The module of this architecture is described with VHDL language and synthesized on Virtex series of FPGA devices. All the synthesis and placement and routing are done with ISE foundation from Xilinx and the whole simulation processes are carried out on Modelsim software.

Anuradha Kulkarni [6] presents the implementation of convolutional encoder and viterbi decoder using system on programming chip. It uses variable constraint length of 7,8 and 9 bits for ½ and 1/3 code rates.The reduced bit error rate with increasing constraint length shows an increase in efficiency and better utilization of resources as bandwidth and power.In this paper, the convolutional encoder and viterbi decoder are tested for different constraint length of 7,8 and 9 bits.

Hema. S [7] presents a field-programmable gate array implementation of Viterbi Decoder with a constraint length of 11 and a code rate of 1/3. It shows that the larger the constraint length used in a convolutional encoding process, the more powerful the code produced. The convolutional encoder and viterbi decoder implemented using VHDL.It is simulated and synthesized using Xillinx technology. a Viterbi algorithm based on the strongly connected trellis decoding of binary convolutional codes has been presented. The use of error-correcting codes has proven to be an effective way to overcome data corruption in digital communication channels.

Yogita Bansal [8] presents the compressor based vedic multiplier with Urdhva Tiryakbhyam sutra is seen as a promising technique in terms of speed and area. This sutra has been noticed to be the most efficient one in terms of speed. A large number of high speed vedic multipliers have been proposed with Urdhva Tiryakbhyam sutra. Few of them are presented in this paper.

Honey Durga Tiwari [9] presents Vedic mathematical formulae and their application to various branches of mathematics. The algorithms based on conventional mathematics can be simplified and even optimized by the use of Vedic Sutras. In this paper new multiplier and square architecture is proposed based on algorithm of ancient Indian Vedic Mathematics, for low power and high speed applications.The design implementation on ALTERA Cyclone –II FPGA shows that the proposed Vedic multiplier and square are faster than array multiplier and Booth multiplier. A new reduced-bit multiplication algorithm based on a formula of ancient Indian Vedic mathematics has been proposed. Both the Vedic multiplication formulae, Urdhva tiryakbhyam and Nikhilam, have been investigated in detail.Urdhva tiryakbhyam, being general mathematical formula, is equally applicable to all cases of multiplication. A multiplier

architecture based on this Sutra has been developed and is seen to be similar to the popular array multiplier where an array of adders is required to arrive at the final product. Due to its structure, it suffers from a high carry propagation delay in case of multiplication of large numbers. This problem has been solved by introducing Nikhilam Sutra which reduces the multiplication of two large numbers to the multiplication of two small numbers. The FPGA implementation result shows that the delay and the area required in proposed design is far less than the conventional booth and array multiplier.

3. CONCLUSION

Convolution encoder using vedic multiplier improves delay and provide faster speed than the normal convolution encoder. Here, the efficiency of Urdhva Tiryakbhyam vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of partial products and eliminates unwanted multiplication steps. This algorithm follows a fast multiplication process and achieves a significantly less computational complexity over its conventional counterparts. Viterbi decoder using parallel processing improves processing speed than normal viterbi decoder because the decoder do not need to wait trace back. It means trace back and decoder can simultaneously work.

4. REFERENCES

[1]. Bineeta Soreng, Saurabh kumar, Efficient Implementation of Convolution Encoder and Viterbi Decoder, 978-1-4673-4922-2113/$31.00 ©20 13 IEEE / 2013 International Conference on Circuits, Power and Computing Technologies [ICCPCT-2013]

[2]. Ms.G.S. Suganya, Ms. G.kavya, RTL Design and VLSI Implementation of an efficient Convolutional Encoder and Adaptive Viterbi Decoder, 978-1-4673-4866-9/13/$31.00 ©2013 IEEE / International conference on Communication and Signal Processing, April 3-5, 2013, India..

[3]. V.Kavinilavu, S. Salivahanan,"Implementation of Convolutional Encoder and Viterbi Decoder using Verilog HDL," 978-1-4244-8679-3/11/$26.00 ©2011 IEEE.

[4]. Lei -ou Wang , Zhe-ying Li, "Design and Implementation of a Parallel Processing Viterbi Decoder Using FPGA," 978-1-4244-6936-9/10/$26.00 ©2010 IEEE.

[5]. Yin Sweet Wong, "Implementation of Convolutional Encoder and Viterbi Decoder using VHDL", 978-1-4244-5187-6/09/$26.00 ©2009 IEEE/ Proceedings of 2009 Student Conference on Research and Development (SCOReD 2009), 16-18 Nov. 2009, UPM Serdang, Malaysia.

[6]. Anuradha Kulkarni, Dyaneshwar Mantri, Neeli R Prasad, Ramjee Prasad," Convolutional Encoder and Viterbi Decoder using SOPC For Variable Constraint Length," 978-1-4673-4529-3/12/2012 IEEE.

[7]. Hema. S, Suresh BABU. V and Ramesh P, "FPGA Implementation of Viterbi Decoder," Proceedings of thc 6th WSEAS Int. Conf. on Electronics, Hardware, Wireless and Optical Communications, Corfu Island, Grecce,Feb.2007.pp.162-167

[8]. Yogita Bansal, Charu Madhu, PardeepKaur," High speed vedic multiplier designs-A review", Proceedings of 2014 RAECS UIET Panjab University Chandigarh, 06 – 08 March, 2011

[9]. Honey Durga Tiwari, Ganzorig Gankhuyag , Chan Mo Kim, Yong Beom Cho, "Multiplier design based on ancient Indian Vedic Mathematics," 978-1-4244-2599-0/08 2008 IEEE.

[10]. A.J. Viterbi, "Error bounds for convolutional codes and an asymptotically optimum decoding algorithm," ieee transactions on information theory, vol. it-13,april, 1967, pp. 260-269.