ANALYSIS AND DESIGN OF HIGH PERFORMANCE LOW POWER 8*8 VEDIC MULTIPLIER

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ABSTRACT

Multiplier plays an vital role in high performance of the system. Multiplication is the basic operation and the speed is limited by the adders used in the architecture. In this paper we have improved the processor speed there by reducing the delay. The speed of the processor is increased by one of the mathematical approach, Vedic mathematics. On the whole in Vedic mathematics Urdhva Triyakbhyam Sutra is used. Addition to this carry skip techniques is realized. An 8 bit multiplier is realized using 4 bit multiplier and thereby reducing the number of logic gates and delays. Simulation is carried out by using Xilinx software. Multipliers are mainly concentrated on speed, area and memory required.

Keyword*: Vedic Multiplier, Urdhva Triyakbhyam Sutra, Delay, Carry skip technique, Xilinx ….*

1 Introduction

Mathematics, resulting from the Veda, provides one line, physical and fast methods along with quick cross checking systems. Multiplication is the important operation performed in processors. Integrating Vedic mathematics for the multiplier design will enhance the speed of the multiplication operation. Multipliers are significant constituent in today's image signal and other digital signal processing applications. Scientific progression has brought to design multiplier which makes propose with high speed, low power consumption, less area in single multiplier thus making them appropriate for various high speed, low power and compacted VLSI implementation. Multiplication is the core component in DSP application. Multiplication is the dominating factor in many applications. A Vedic process is very quick and requires less hardware. For composite applications need of quicker multiplier chip is required. The Vedic multiplier brings alter in good quality organization for a processor than any other system.

1. Vedic Multiplication

Vedic method of mathematics is primarily based on sixteen sutras. It was reconstructed by Swami Bharathi Krishna in 20th century. Vedic Mathematics converts a monotonous theme into a playful and enjoyable one .Vedic Mathematics with its unique skin tone has the inbuilt probable to solve the psychological problem in Mathematics. It can be pertinent to various division of engineering with some algorithms. Here we used vertical and cross wise technique.

1.2 **Urdhva Triyakbhyam Sutra (Vertical and Cross wise technique)**

Among the sixteen sutras we use two sutras for multiplication purpose. One is Urdhva Triyakbhyam i.e., vertical and cross wise technique and other is nikilam sutra i.e., all from 9 and the last from 10.Thse sutras provide efficient time for calculation and partial sums are obtained in a single step.

Urdhva Triyakbhyam is explained by multiplication of two decimal numbers.

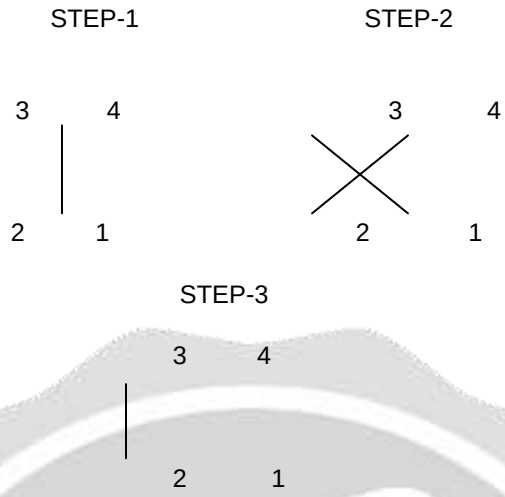

Fig1: Multiplication Of Two Decimal Numbers

Similarly for two bit binary numbers vertical and cross wise technique is employed.

1.2 Tabulation

The sixteen sutras are explained as follows:

S.NO	SUTRAS	MEANINGS
1.	Ekadhikina Purvena	By one more than the previous one
2.	Nikhilam Navatashcaramam	All from 9 and the last from 10
3.	Urdhva-Tiryagbyham	Vertically and crosswise
4.	Paraavartya Yojayet	Transpose and adjust
5.	Shunyam Saamyasamuccaye	When the sum is the same that sum is zero.
6.	Shunyamanyat	If one is in ratio, the other is zero
7.	Sankalana-vyavakalanabhyam	By addition and by subtraction
8.	Puranapuranabyham	By the completion or non-completion
9.	Chalana-Kalanabyham	Differences and Similarities
10.	Yaavadunam	Whatever the extent of its deficiency
11.	Vyashtisamanstih	Part and Whole
12.	Shesanyankena Charamena	The remainders by the last digit
13.	Sopaantyadvayamantyam	The ultimate and twice the penultimate

14.	Ekanyunena Purvena	By one less than the previous one
15.	Gunitasamuchyah	The product of the sum is equal to the sum of the
16.	Gunakasamuchyah	The factors of the sum is equal to the sum of the

2. Algorithm for 4-Bit Urdhva Triyakbhyam

Multiplicant A3 A2 A1 A0

Multiplier B3 B2 B1 B0

Product S T U V W X Y Z

P7 P6 P5 P4 P3 P2 P1 P0

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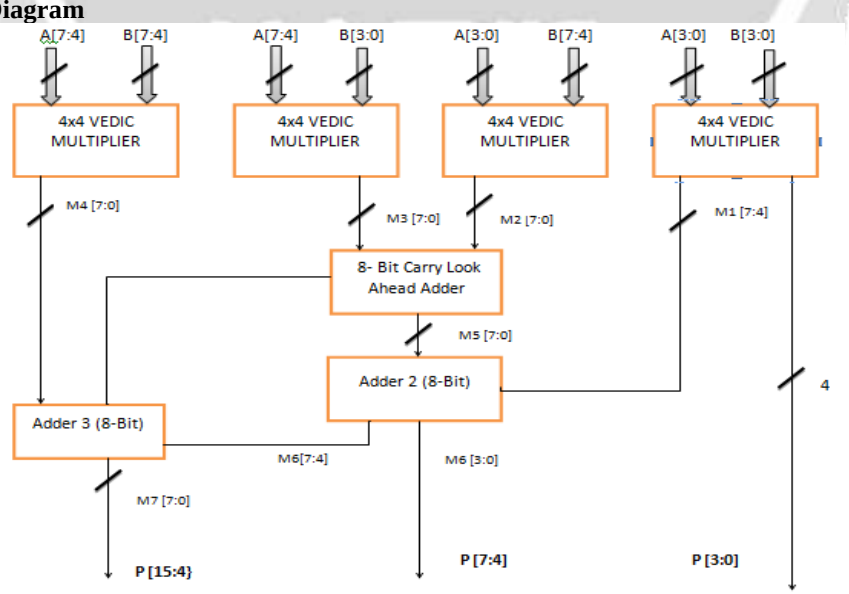
3. Proposed Vedic Multiplier Architecture

In the proposed 8×8 Vedic multiplier architecture utilizes 4×4 multiplier block. In this method partial product generation and addition are done concurrently. This is well suited for binary multiplication and in turn reduces delay there by increasing the speed of the multiplier. Computational speed of multiplication is increased compared to normal multiplication.

3.1 Block Diagram



.Fig2: Block Diagram Of 8*8 Vedic Multiplier

3.2 Architecture

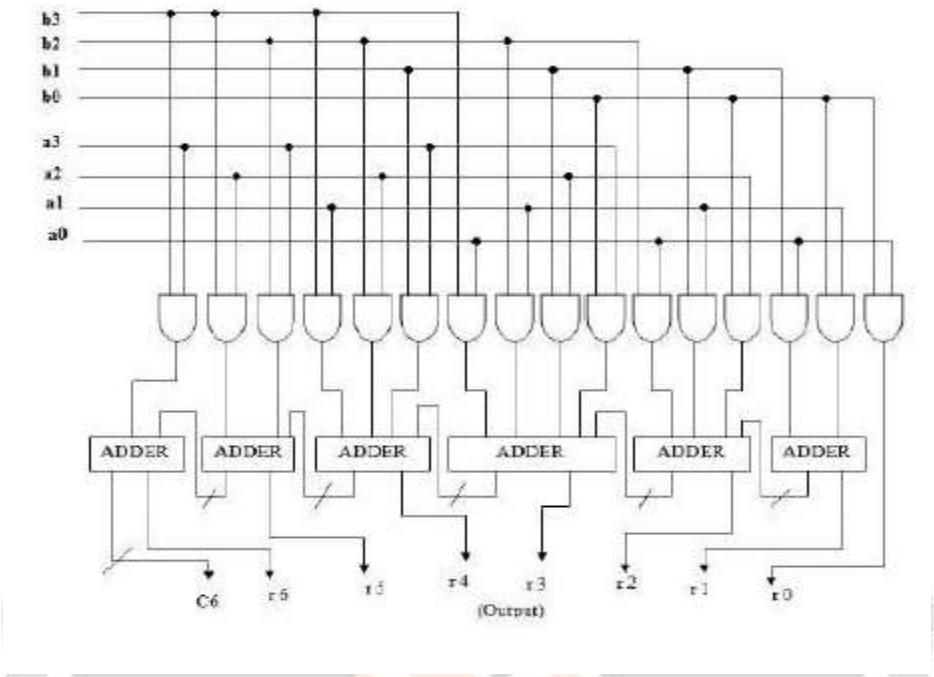


Fig3: Hardware Architecture of 4*4 Vedic Multiplier

Modified equation for proposed multiplier architecture:

PC0=X0Y0
PC1=X1Y0+XOY1
PC2=X2Y0+X1Y1+X0Y2+X0X1Y0Y1
PC3=X3Y0+X2Y1+X1Y2+X0Y3+carry from PC2
PC4=X3Y1+X2Y2+X1Y3+carry from PC2+ carry from PC3
PC5=X3Y2+X2Y3+carry from PC4+carry from PC3
PC6=X3Y3+X1Y1X2Y2+carry from PC4
PC7=carry from PC6

This modified equation, to reduce the delay and waiting of carry off from previous step.

3.3. Speed

Vedic multiplier is more rapidly than array and booth multiplier. Time delay is very much compact in Vedic multiplier compared to further multipliers. Vedic multiplier has numerous compensation over normal multipliers such as gate delays, number of logic level used etc., Thus Vedic multiplier shows soaring speed amid other predictable multipliers.

3.4. Power delay in gates

The power delay is the outline of value interrelated with the energy competence of logic relations. It is the product of power utilization times the input output interruption. The power burning up is reduced by using ECRAL(Efficient charge recovery adiabatic logic.

4. STIMULAION AND RESULT ANALYSIS

4.1 Implementation

In this project,8×8 bit Vedic multiplier using vertical and cross wise technique i.e.,"Urdhva Triyakbhyam" is implemented in VHDL code (Very High Speed Integrated Circuit Hardware Description language).

4.2 Comparison

The 8-bit multiplier is compared with different design in terms of total delay, logic delay and propagation delay. This can be given in the tabulation provides obvious reduction in delay. The logic delay is about 5.9ns and total delay of 15.9ns. The number of logic levels is 13. Thus the proposed design gives good performance than other popular multiplier architecture and developed the high speed intricate multiplier with reduced interruption.

Utilities	8-Bit Vedic Multiplier	4- Bit Vedic Multiplier	Array Multiplier	Booth Multiplier
Logic levels	10	13	15	18
Logic delay	5.02	7.89	8.9	10.6
Memory	15000	1509864	151988	152773
Number of 4 input LUTs	35	504	690	867

5. RESULT

5.1 RTL Schematics

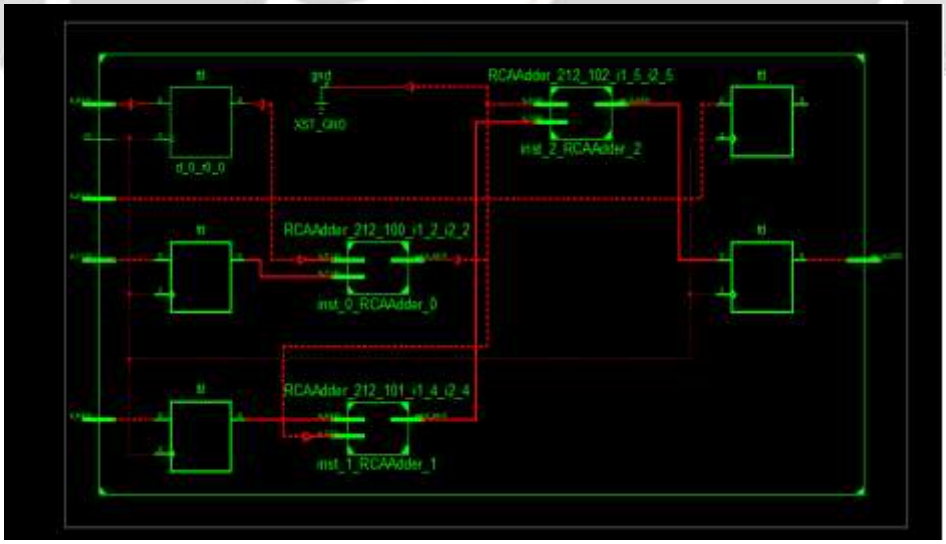


FIG 4: RTL Schematic of 8*8 Vedic Multiplier

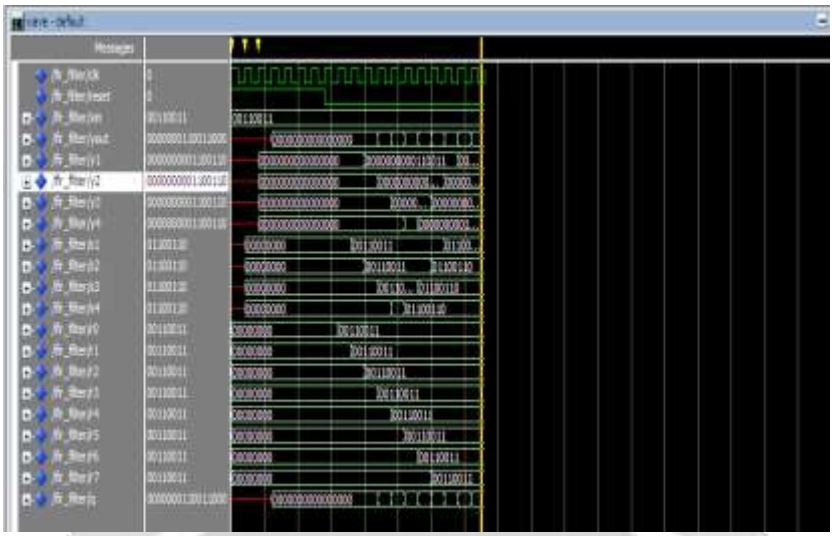


FIG 5: Output of Normal 8*8 Multiplier

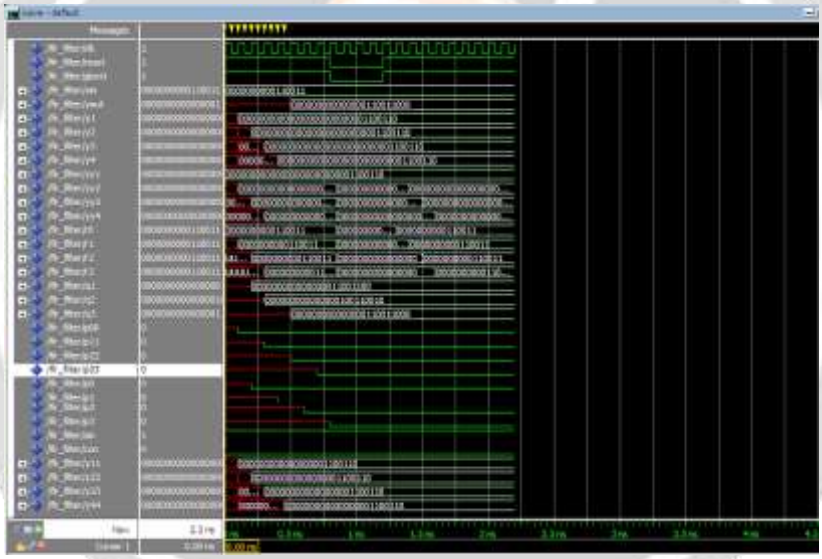


FIG 6: Output of 8*8 Vedic Multiplier

5.2. Advantages

The advantages of Vedic multiplier are

- ✓ Amplify the rate of the system
- ✓ To gain good competence of the system.
- ✓ Diminish the instance interruption as well as path delay.

6. CONCLUSION

Vedic formulas are based on the rudiments. This fascinating pasture presents some successful algorithms which can be practical to propose of Digital filters. The prospective of this turf can be used resourcefully to resolve the actual globe tribulations. The Vedic multiplier is potential to decrease area, raise speed, shrink power utilization and to reduce complication of digital FIR and IIR filters. It is probable to hold out do research work on uses of Vedic mathematical algorithms over conventional methods. FIR and IIR filters uses operations like multiplication and addition. Array and booth multiplier consumes more power and delay will be larger. Thus vedic mathematics increase the speed which determines the efficiency of the system.

6.1 Future Work

Vedic mathematics has been developed over 2500 years ago. This gives the clue of symmetric computation in multiplication. It deals with various topics of mathematics such as geometry, calculus, trigonometry, arithmetic calculations. All these methods are very efficient compared with manual calculation are concerned. If this method are implemented in hardware will drastically reduce the computational speed. This process is not been implemented in DSP and ADSP processors which employs larger number of multiplication in FFT'S

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