ANALYSIS AND DESIGN OF HYBRID ACTIVE MULTI-LEVEL INVERTER TOPOLOGY FED INDUCTION MOTOR DRIVE

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ABSTRACT

This paper proposes a new five-level hybrid topology combining features of neutral point clamped and flying capacitor Multi-level inverters. The proposed topology provides a tradeoff between different component counts to achieve a good loss distribution, avoid direct series connection of semiconductor devices, keep the balanced operation of dc-link capacitors while keeping the number of costly components such as capacitors and switches low. The Pulse width modulation strategy for this hybrid topology has designed using modified SVPWM technique. The features of the proposed topology are investigated and compared to other available topologies. Simulation results are provided to verify the performance of the converter for medium voltage applications. Performance of the proposed technique under different operating conditions is investigated in the MATLAB/Simulink environment with R-L load initially and extended with Induction motor load. The operation of the proposed topology is studied for Line, Phase voltages and THD.

Keyword: - *Neutral point clamped Inverter, Flying capacitor Inverter, CSVPWM, THD.*

1. INTRODUCTION

Multilevel converters are a very attractive solution for medium-voltage high-power conversion applications; such as motor drives, microgrids, and distributed generation systems. The main features of these topologies, as compared with the two-level voltage-source converters (VSC), are their capabilities to reduce:

1) Harmonic distortion of the ac-side waveforms;

2) *dv/dt* switching stresses;

3) Switching losses; and

4) Minimize or even eliminate the interface transformer [1].

Many multilevel topologies have been developed, among them, the neutral-point clamped (NPC), flying capacitor (FC), and the cascaded H-bridge (CHB), are the most studied and well-established multilevel topologies, which are so-called classic multilevel topologies [1]–[5]. Although the classic multilevel converters have been commercialized by major manufacturers, they have some drawbacks, which limit their applications. For instance, an NPC structure with higher number of levels is less attractive and this is because the number of clamping diodes increases substantially with the voltage level. For FC structure, the number of FCs increases with the voltage level. The CHB topology needs a large number of isolated dc sources and an expensive and bulky phase-shifting transformer.

Numbers of variants and new multilevel converters have been proposed in literatures [6]–[15]; however, most of them are variations to the three classic multilevel topologies or hybrids between them, which are so-called advanced multilevel topologies. Among the recent topologies, the following topologies have found practical application, which are commercialized by manufacturers; the five-level H-bridge NPC (5L-HNPC) [6]–[9], the three-level active NPC (3L-ANPC) [10]–[11], the five-level active NPC (5L-ANPC) [12]–[15], and the four-level nested neutral-point

clamped (NNPC) converter [16]. A 5L-HNPC is the H-bridge connection of two classic 3L-NPC phase legs, which makes a five-level converter. This topology like an H-bridge topology requires isolated dc sources with the phase-shifting transformer, which increases the cost and complexity of the converter.

A 3L-ANPC is an improved three-level NPC, which can control the loss distribution among the switches of the converter. This topology has higher number of the devices as compared to three-level NPC with the same number of output voltage levels. This increases the cost and complexity of the overall converter. A 5L-ANPC is a combination of a 3L-ANPC and 3L-FC. The main drawback of the 5 L-ANPC converters is that the voltage rating of the switches in one phase of the converter is different.

The voltage rate of the outer switches is half of the dc-bus voltage and the voltage rate of the inner switches are 1/4 of the dc-bus voltage. The hybrid converter, as shown in Fig. 1, is a recent multilevel converter topology with interesting properties such as [16]:

1) It can operate for a wide range of 2.4–7.2 Kv without device in series;

2) It has fewer parts, in compare to same rate previous multilevel converters;

3) All the switches have the same voltage stress and equal to one third of the input voltage;

4) It does not need any complex transformer;

5) The hybrid converter mitigates some drawbacks of the existing topologies, however still the voltage rate that this converter can operate without connecting power semiconductor devices in series is limited to 7.2 kV.

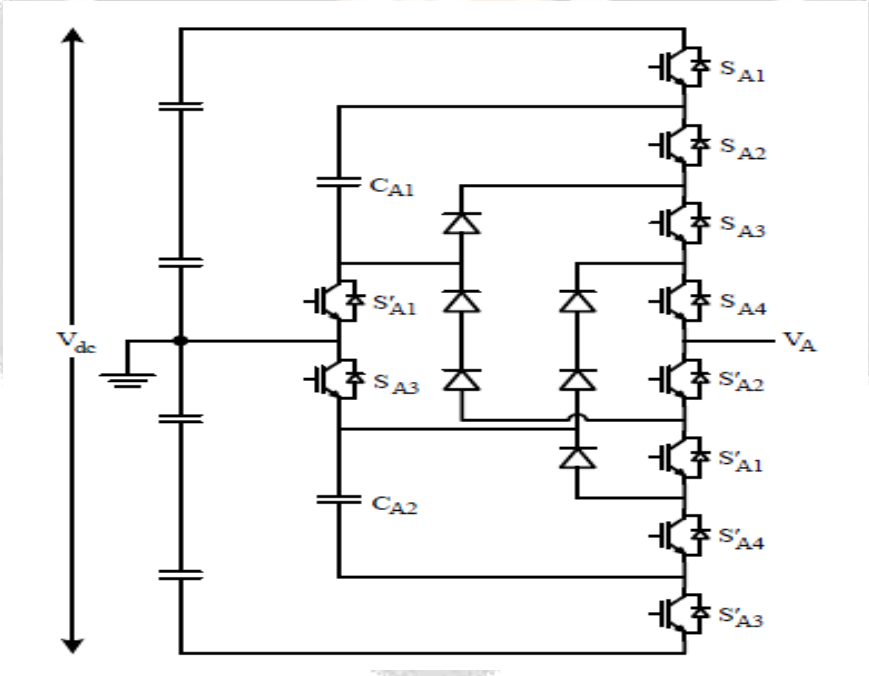

Fig-1: Single Leg of Proposed ANPC converter.

One of the main common issues for the multilevel converter is to control the capacitor voltages at their nominal values to operate the converter properly. For example, for a diode clamped converter the dc-link capacitor voltages should be balanced at nominal values and for a FC converter the voltages of the FCs should be regulated. Different strategies can be applied to control the voltage of capacitors in multilevel converters. One approach is to use auxiliary converter to perform the voltage balancing, which increases the cost and complexity of the overall converter particularly at high-voltage/power levels [17].

Various modulation strategies have been developed and studied for multilevel converter topologies. Since the multilevel converters are intended to be used in high-power applications; there are two major challenges in the selection of modulation strategies; high power quality and minimum switching frequency. Moreover, depends on the converter topology, there may exist some redundant switching states for each voltage level. Theses redundancies

increase the number of calculations in the cost function in order to select the best switching state [5], [16]. By the increase in the number of levels, the computational burden for the real-time implementation will increase and sometimes the real-time system cannot handle this task properly, which deteriorate the performance of the converter.

Another modulation scheme that is the most popular modulation scheme in industrial applications is sinusoidal PWM Fig. 2. Block diagram of the proposed SPWM approach for phase *x*. This modulation scheme is based on the multicarrier PWM strategy. The performances of the different SPWM strategies are studied analytically in to show which SPWM strategy has the better harmonic performance. Moreover, the comprehensive comparison of the SPWM and SVM modulation schemes has been studied in [17].

The main focus of this paper is to propose a new approach using multicarrier SPWM strategy to generate multilevel output voltage, while regulating the voltage of capacitors. This approach employs the deviation of the capacitor voltages from their nominal values and based on the converter output current select the best switching state from the available redundant switching states to charge or discharge the capacitors, and finally, regulate the voltages of capacitors. This approach, unlike the SVM strategy, does not need any cost function and is very intuitive and simple to implement, however, it is very effective. In this procedure, first, the modulating signal for phase *x* (*x* = *a*, *b*, *c*) is compared to carriers (*n*-1 carriers for an *n*-level converter), and then, the desired output levels are determined. Based on the desired output level, the corresponding switching state that generates this voltage level can be applied to the power switches. Moreover, there are some redundant switching states for some levels that come from the topology of the converter.

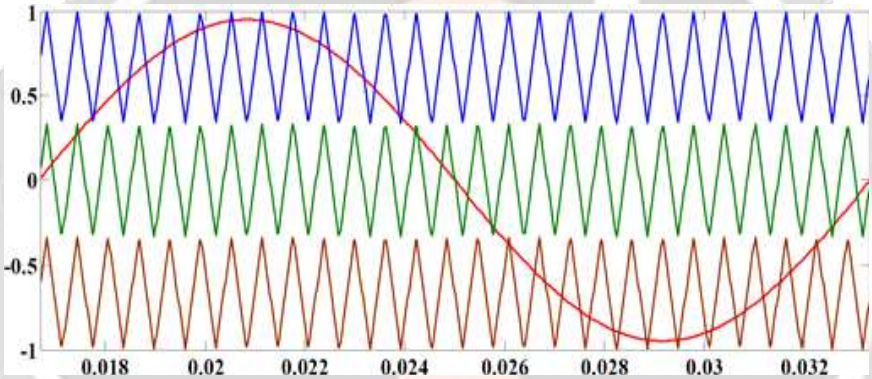

Fig-2: Level-shifted multicarrier modulation for the NNPC inverter.

One of the main advantage of the proposed strategy is that, unlike the SVM strategy, this strategy can be applied for each phase of the converter separately, as a result when the converter is employed to be in different configurations such as the back-to-back structure, cascades H-bridge structure, and modular multilevel structure, the proposed modulation scheme can be implemented easily to generate the output multilevel voltage and also regulate the capacitor voltages. In this paper, this strategy is developed for an NNPC converter. Fig. 4. Desired output levels based on modulating signal.

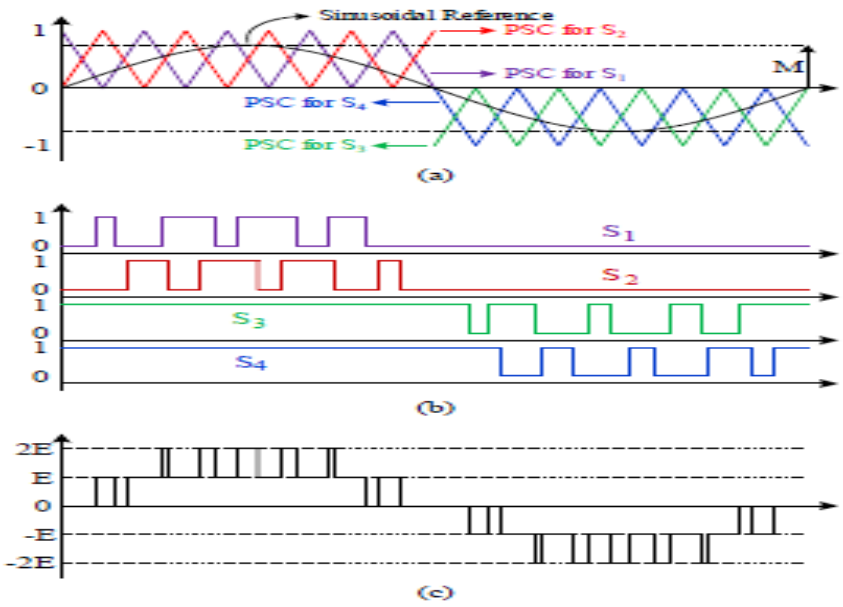

Fig-3: A phase shifted PWM

Hybrid topologies are viable solutions where higher number of levels is required. Combining the advantages of CHB, FC, and NPC, hybrid inverters can provide loss and voltage balancing while keeping the number of components low. Examples of hybrid topologies combining FC and NPC can be found in [10]–[12], some of which has already found industrial applications.

The 5-level FC-ANPC is an example of hybrid topologies that made its way to the industry. The ACS2000 family of medium voltage drives, commercialized by ABB, uses this topology with both active and passive front end configurations. The main advantage of this topology is the use of a single flying capacitor to generate the output five levels. Compared to other topologies that provide a common dc-link, FC-ANPC has provided an acceptable tradeoff between the cost, performance, and reliability for 5-level applications. The disadvantages of FC-ANPC are high number of switches, series connection of high voltage switches, and poor loss distribution [13].

This paper proposes a new 5-level hybrid topology based on FC and NPC inverters. The goal of the proposed topology is to overcome the shortcomings of the traditional FC-ANPC. Thus, comparatively, the proposed topology provides better loss distribution, avoids direct series connection of high voltage switches, and eliminates 2 switches per phase leg. These advantages come at the cost of an additional capacitor and 6 diodes. Nevertheless, the lifetime of each capacitor is expected to prolong due to the half cycle operation and lower rms current.

2. PROPOSED HYBRID ACTIVE NEUTRAL POINT CLAMPED FLYING CAPACITOR MULTILEVEL INVERTER

The proposed topology includes a dc-link that is common among the three phases. The dc-link provides three voltage levels +2E, 0, and -2E for the phase legs. Since all the phases have similar configuration, only one phase leg of the proposed topology has been shown in Fig. 1. All the components shown in the figure have equal operating voltage E i.e. one fourth of the dc-link voltage Vdc. The flying capacitors CA1 and CA2 are controlled to stay charged at the target voltage E. The available states of one phase leg are shown in table I. To generate level 2E, all the top arm switches SA1, SA2, SA3, SA4 should turn on. For level E, two choices are available i.e. either through dc-link's positive point (EP) or through dc-link's neutral point (E0). This redundancy can be used to balance the voltage of CA1. Level 0 is generated through clamping the dc link's neutral point to the output (00). Negative states can be generated similarly due to the symmetry of the topology.

The operation of this topology is in essence similar to topologies such as stacked multi cell (SMC) converter [14], [15], [7], where the positive and negative stacks operate independently. Hence, the positive stack capacitor CA1 is used and balanced during the positive cycle and rest during the negative cycle, whereas the negative stack capacitor CA2 is used and balanced during the negative cycle and rest during the positive cycle. So, the flying capacitors will see the switching frequency rather than line frequency and therefore the capacitor size is not too large.

Similar to the three-level NPC inverter, if the three phases of the load are balanced, the neutral point voltage will be constant in theory. However, the voltage might slightly drift away due to the imbalance in the elements' leakage current. In addition, although small, there is always some imbalance among the phases. A constant voltage drifts, even though small, can cause higher voltage across part of the devices which can be lethal. Nevertheless, this drift can be compensated by injecting a small common mode to the three phases. An important feature of the proposed topology is the even distribution of transitions among switching devices. Therefore, switching loss which is the major limiting factor of inverter's thermal performance is distributed among the switches. As the main result, the tradeoff between switching frequency and current derating is improved. This provides the opportunity to either increase the rated current and power of the inverter or increase the switching frequency resulting in lower capacitor size and improved voltage waveform quality.

3. MODULATION TECHNIQUES APPLIED TO PROPOSED TOPOLOGY

Various modulation techniques may be adapted for the proposed topology. Carrier-based modulation with sinusoidal or modified reference as well as non-carrier-based techniques such as space vector modulation and selective harmonic elimination may be used to generate the gate signals. The choice of a modulation technique is mostly a tradeoff among the requirements of the application, complexity of the software, and cost of the control hardware.

Table-I: Switching states of the proposed converter

Level	State	S_1	S_2	S_3	S_4	C_1	C_2
+2E	+2E	1	1	1	1	N.A.	N.A.
+E	+EP	1	0	1	1	i>0 Charge i<0 Discharge	N.A.
	+E0	0	1	1	1	i>0 Discharge i<0 Charge	N.A.
0	0	0	0	1	1	N.A.	N.A.
-E	-E0	0	0	1	0	N.A.	i>0 Charge i<0 Discharge
	-EN	0	0	0	1	N.A.	i>0 Discharge i<0 Charge
-2E	-2E	0	0	0	0	N.A.	N.A.

3.1 Carrier-Based Modulation

Carrier set's arrangement and reference waveform's shape are the main sources of varieties in carrier-based modulation techniques for multilevel inverters. As for carrier set's arrangement, level shifted carriers LSC and phase shifted carriers PSC are the two main categories that are respectively suitable for diode-clamped and multi-cell structures. Two members in the LSC family, alternative phase opposition disposition APOD and phase disposition PD are known to generate the best results for singe-phase and three phase applications, respectively. PSC in its original form has been shown to generate a PWM waveform that matches with APOD. Also a modified version of PSC with dynamic phase shift has been shown to match with PD [16].

The reference for single-phase applications is usually a simple sinusoidal waveform. For three-phase applications, a variety of reference waveforms are available due to the possibility of common mode injection in three-phase structure. This flexibility has been used to serve different purposes such as increased dc link utilization, lower THD, lower Loss, and neutral point voltage control.

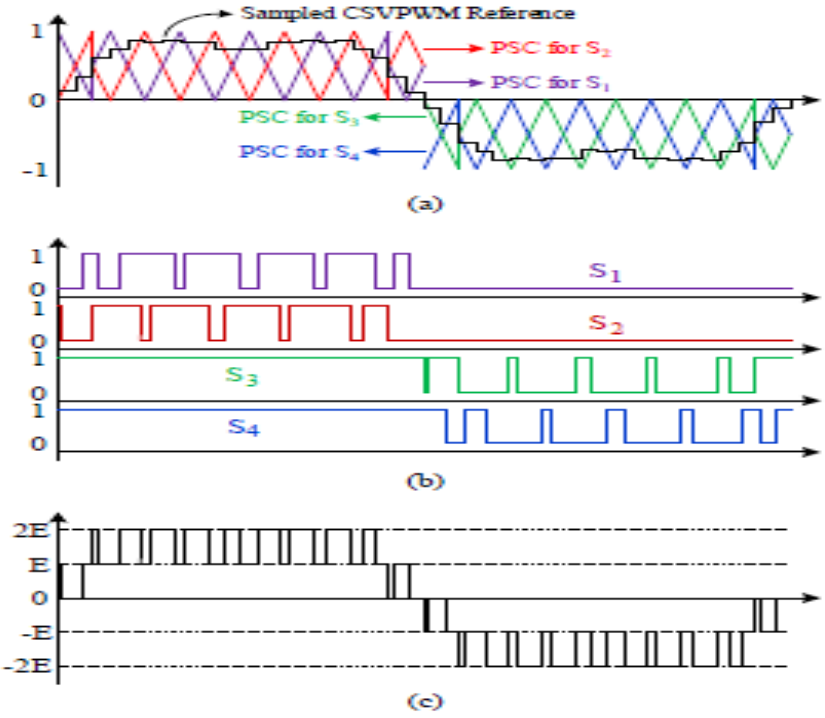

Fig-4: Carrier-based modulation using modified PSC with sampled CSVPWM reference for three phase application. (a) Reference and carriers arrangement. (b) Gate signals. (c) Output waveform.

For the proposed inverter, a hybrid modulation technique is required due to the hybrid structure of the topology. Figure 3 illustrates the modulation technique for single-phase case. It is intuitive to separate the operation to positive and negative cycles, since each cycle is generated with a 3-level FC stack. The gate signals for each FC is then generated using PSC to provide natural voltage balancing for the flying capacitors. The generated output PWM waveform matches the APOD scheme.
For three-phase case, similar approach may be adopted except that, to generate a PD scheme equivalent, the positive cycle carriers should have $\pi/2$ phase shift compared to the negative cycle carriers. Also, the carriers incorporate a dynamic phase shift which for sampled reference waveforms always adds up by $\pi/2$ at the carrier band transitions.

For the reference waveform, centered space vector PWM (CSVPWM) sampled at half PD carrier period can provide similar output performance as SVM. Figure 4 illustrates the modulation technique using sampled CSVPWM along with modified PSC for the proposed inverter.

Table-II: Simulation Parameters

Converter parameters	Values
Converter rating	0.5MVA
FCs	2200µF
Input DC Voltage	600V
Output Frequency	60Hz
Output Inductance	5mH
Output Load	7.5Ω

4. RESULTS AND ANALYSIS

To verify the operation of the proposed topology and the performance of the modulation techniques provided in section III, a model is developed and simulated with MATLAB software.

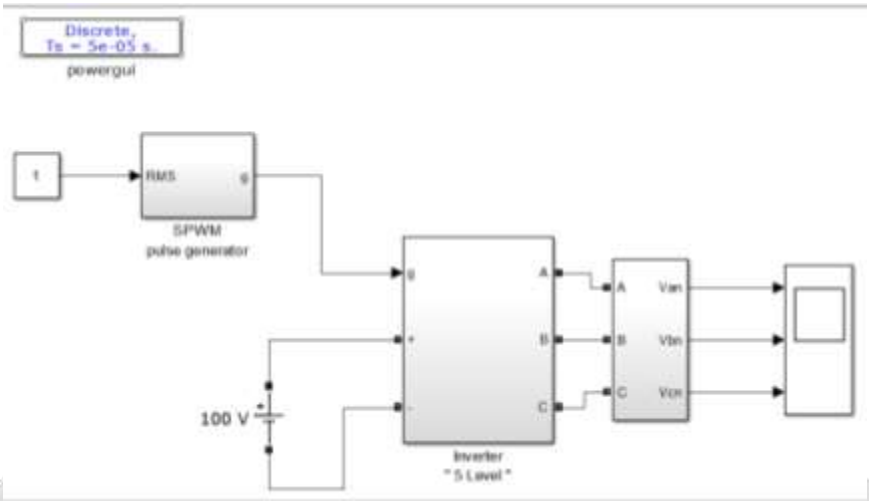

Fig-5: Proposed circuit using MATLAB design

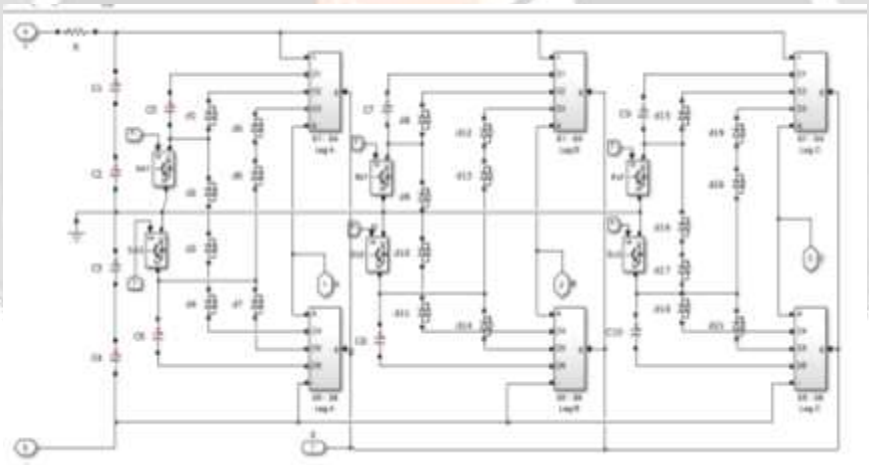

Fig.6: The proposed hybrid active MLI topology

4.1 SPWM control of the proposed topology

The Proposed systemPWM control has used basic SPWM technique to observe the output density and THD of output. Fig-7 to Fig-11 represents the outputs corresponding to SPWM technique.

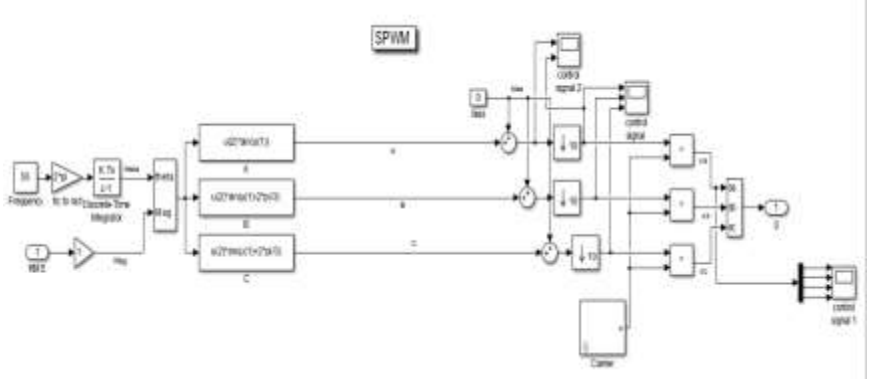

Fig-7: SPWM control of the proposed topology

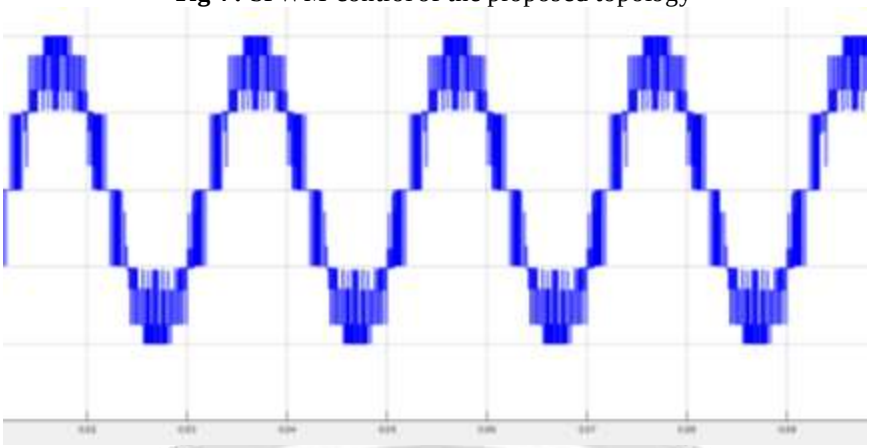

Fig-8: Phase voltage of a single Leg waveform

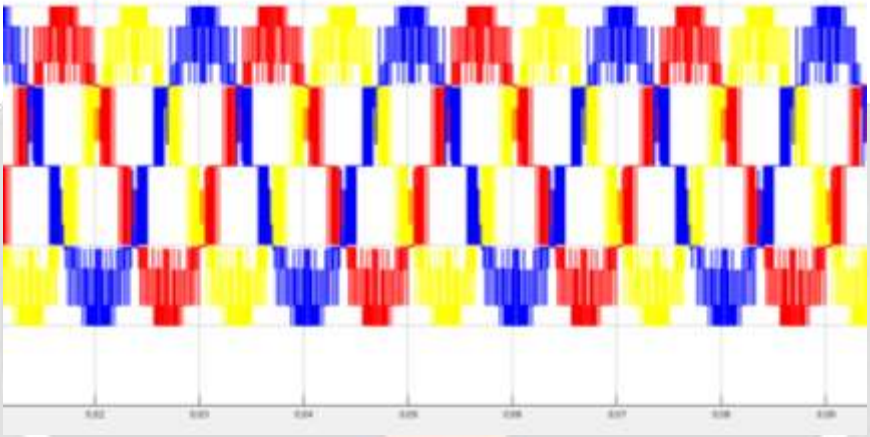

Fig-9: The three phase voltage waveform of the proposed topology with SPWM

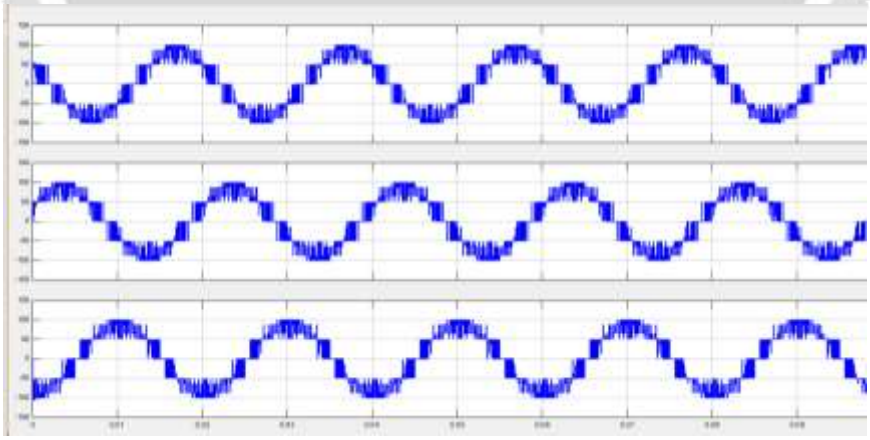

Fig-10: The line voltage waveform of the proposed controller using R-L load.

4.2 Third Harmonic Based SVPWM Control

The proposed system reference sine wave has formed of third harmonic to remove the third harmonic from output of the inverter which is going fed to any application. The Proposed system PWM control has used third harmonic SPWM technique to observe the output density and THD of output. Fig-7 to Fig-11 to 13 represents the outputs corresponding to third harmonic SPWM technique

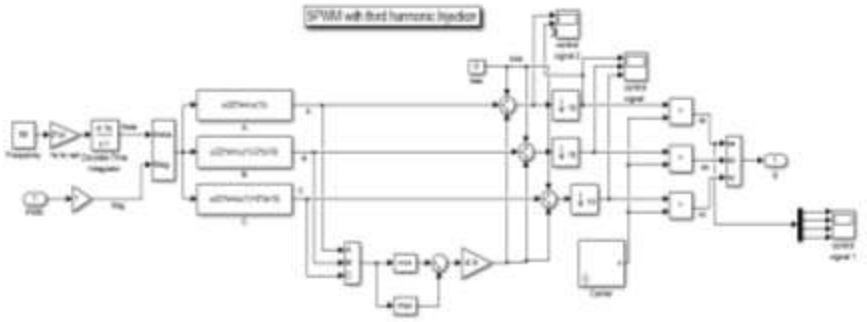

Fig-11: The Third harmonic CSVPWM applied to proposed control

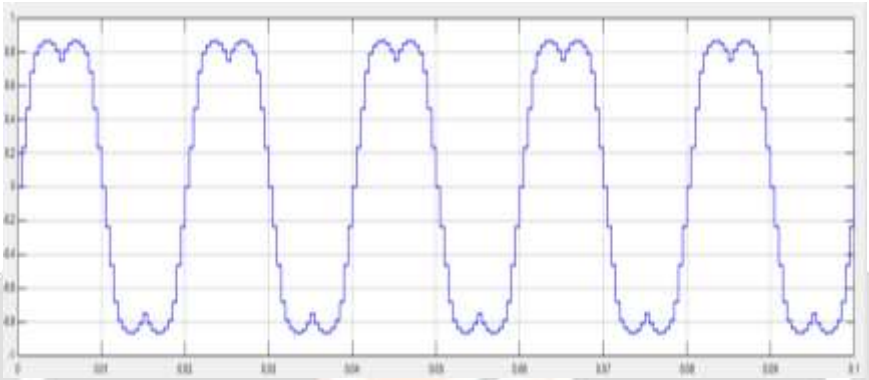

Fig-12: The reference Sine when using CSVPWM control

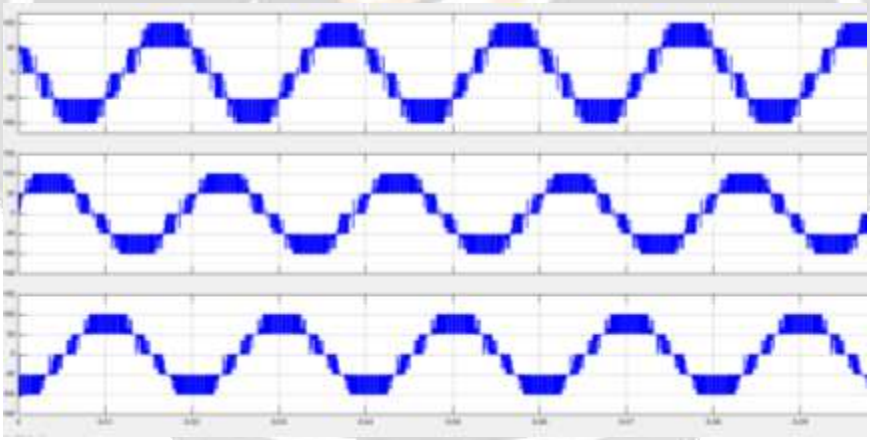

Fig-13: The Output phase voltage for CSVPWM

4.3 When fed to INDUCTION Motor

The proposed system also tested by feeding it to INDUCTION Motor as a Drive. The speed, torque and stator currents are given from fig-14 to 17.

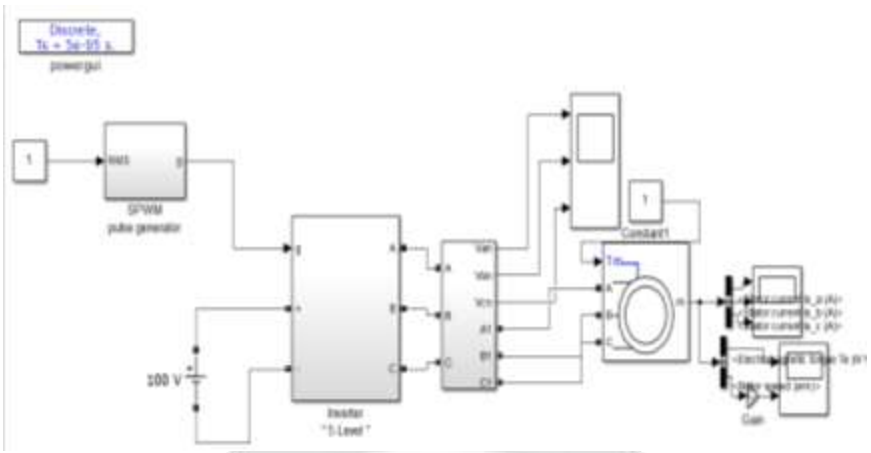

Fig-14: The proposed Topology fed to Induction motor

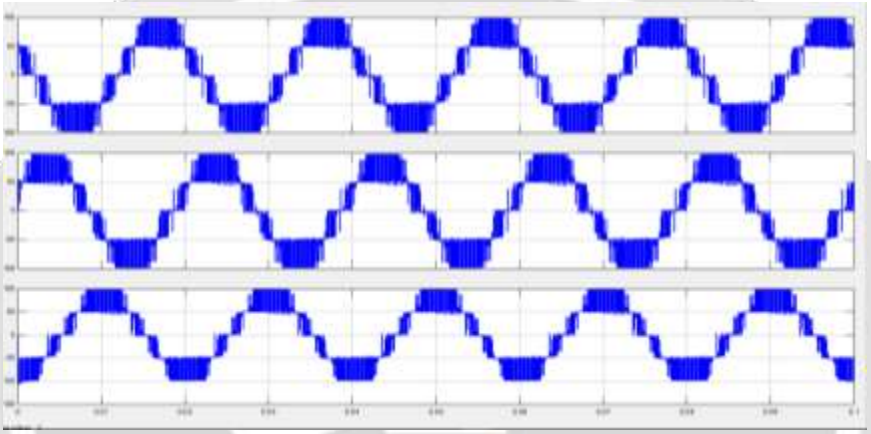

Fig-15: The Phase voltages of the proposed converter fed to IM

Fig-16: The stator currents of the Induction motor

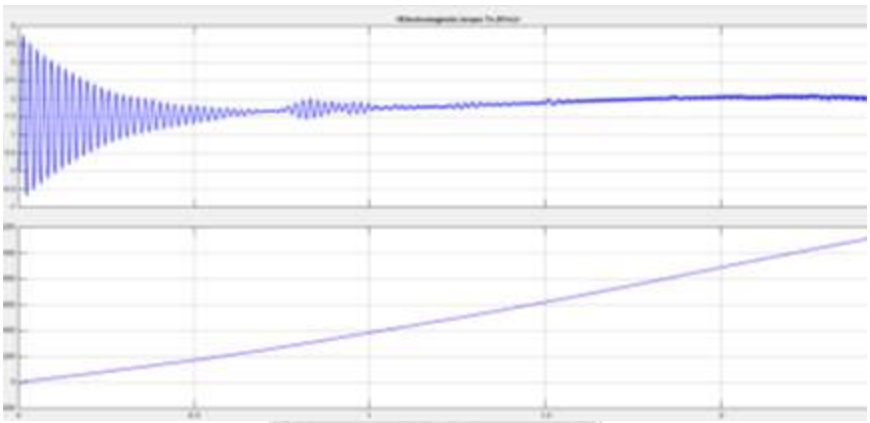

Fig-17: The torque and speed of Induction Motor

5 CONCLUSION

A new hybrid 5-level inverter topology and modulation technique is proposed. Compared to 5-level ANPC as the most similar topology, this new topology requires two less switches at the cost of an additional capacitor and six diodes. However, since the capacitors still see the switching frequency and their size remain the same, it is expected to reduce the inverter's total cost. Also, unlike 5-level ANPC, all switches must withstand the same voltage which eliminates the need for series connection of switches and associated simultaneous turn on and off problem. Good loss distribution among switches can increase the inverters rated power or provide higher switching frequency and smaller capacitor size.

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