ANALYSIS AND DESIGN OF SYMMETRICAL MULTI-LEVEL INVERTER FOR MEDIUM VOLTAGE HIGH POWER APPLICATIONS

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ABSTRACT

This paper presents optimal design of three-phase multilevel inverter for distributed power generation system using low frequency modulation and sinusoidal pulse width modulation as well. It is a modular type and it can be extended for extra number of output voltage levels by adding additional modular stages. The impact of the proposed topology is its proficiency to maximize the number of voltage levels using a reduced number of isolated dc voltage sources and electronic switches. Moreover, this paper proposes a significant factor which is developed to define the number of the required components per pole voltage level. A detailed comparison based on is provided. The Simulation have obtained using MATLAB software for analysis.

Keyword: - *Low frequency modulation, multi-level inverter, multi-level inverter comparison factor, sinusoidal pulse-width modulation (SPWM), symmetrical DC power sources, three-phase.*

1. INTRODUCTION

Multilevel inverters (MLIs) are finding increased attention in industries as a choice of electronic power conversion for medium voltage and high-power applications, because improving the output waveform of the inverter reduces its respective harmonic content and, hence, the size of the filter used and the level of electromagnetic interference (EMI) generated by switching operation. Various multilevel inverter (MLI) structures are reported in the literature, and the cascaded MLI (CMLI) appears to be superior to other inverter topologies in application at high power rating due to its modular nature of modulation, control and protection requirements of each full bridge inverter (FBI). CMLI synthesizes a medium voltage output based on a series connection of power cells that use standard low-voltage component configurations. Most of the modulation methods developed for MLI is based on multiple-carrier arrangements with pulse width modulation (PWM). The carriers can be arranged with vertical shifts (phase disposition, phase opposition disposition, and alternative phase opposition disposition (APOD) PWM), or with horizontal displacements (phase-shifted carrier (PSC) PWM). Space-vector modulation (SVM) is also extended for the MLI operation, offers good harmonic performance. A few publications are available in the area of hybrid modulation to improve the performance of the MLI. In space-vector-based hybrid PWM technique is reported to reduce current ripple. This paper addresses the issue to reduce the switching loss of multilevel sinusoidal-modulation (MSPWM) schemes with low computational overhead. Also, it covers the methodology for equal power dissipation among the power devices, and the power modules. Architecture for Complex Programmable Logic Device (CPLD) implementation with only logical elements is presented adopting sequential switching hybrid-modulation (SSHM) algorithm with PWM circulation. Although only the five-level case is presented here, the proposed method can be equally applied to any number of voltage levels, any number of phases, and switching transitions.

Multi-level inverters have obtained great attention as a single stage inverter. Although, they need high number of components, but due to their advantages such as generating output voltage with extremely low distortion factor , low dv/dt, small output filter size, low electromagnetic interface, and low total harmonic distortion , still have great attention [1]–[6]. Practically, all of these advantages appear strongly as the number of dc-power sources increased as in the case of renewable energy systems. The general concept of is to utilize isolated dc sources or a bank of series capacitors to produce ac voltage waveforms with higher amplitude and near sinusoidal waveform. There are three conventional types of named as neutral point diode clamped [7], flying capacitor [8], and cascaded H-Bridge [9]. Almost all of them are suffering from increased components number per level, and complex control architecture [9].

Among the different topologies for, they can be classified into two main categories:
1) Single dc-source inverter such as, and inverters;
2) multi-dc sources inverters such as inverter.

While, multi-dc sources inverter is divided into symmetrical and nonsymmetrical topologies. Principally, nonsymmetrical topologies produce more voltage levels compared to symmetrical topologies. Almost all of these topologies can be extended for more voltage levels by increasing the number of the primary configuration (basic cell). Many topologies were presented in the last decade focusing on minimizing the basic multilevel topologies drawbacks. The author in [1] presented a topology named multilevel dc link. It consists of a group of basic cells connected in series configuration. Each cell produces or 0 voltage across the connected cells, there is an H-bridge to change the polarity of the synthesized voltage. The required number of active switches for output voltage levels is for the inverters. However, this topology requires increased number of components compared to the conventional topologies, and high voltage stresses. However, in [2], the authors presented a topology named transistor-clamped H-bridge. The primary cell can produce five-levels per pole in the output voltage. However, it suffers also from the increased components counts, requirements of electrolytic capacitors, complex control methodology.

On the other hand, in [5], the authors presented three-phase asymmetrical multi-level cascade inverter. The output voltage levels synthesized by series connected cells like in [1]. For two cells configuration, it produces four levels per pole 0, E 2E, 5E. However, instead of using H-bridge to getting the opposite voltage polarities as in [1], it uses simply the phase shift relationship between the three legs, by subtracts each leg's voltage with the neighboring one to produce the line voltage, the same subtraction idea was presented in [4].

While, the authors in [15] presented a new single dc-link power supply topology, the presented topology generates seventeen voltage levels 0 , E/16, E/8, 5E/16, E/4, 5E/16, 6E/16, 7E/16,E/2, 9E/16, 10E/16, 12E/16, 15E/16, 14E/16, 15E/16 AND E on the output voltage by using three level flying capacitor inverter and cascades H-bridge. However, this topology utilizes a single dc-power supply. It uses increased number of electrolytic capacitors as floating dc-power supplies. The authors in [6] presented a double sub-module circuit. The presented cell generates a three output voltage levels across its terminals using eight switches and two capacitors. It improved the voltage balancing over capacitors at low switching frequencies; however extra components compared with the equivalent half bridge modules required. Some topologies such as in [7] were presented for large scale application. They basically use a dc-ac inverter stage to convert the dc output voltage from the PV modules to the required ac-voltages. That in turns transformed into three ac isolated voltages using a medium frequency transformer having three secondary windings. This configuration suffers from many limitations like increasing components counts, high cost, noise, low efficiency, and big installation size.
In [4]–[7], new sub-families of the were produced. They mainly consist of a high voltage main stage linked with low voltage auxiliary stages. The main stage commonly utilizes a conventional voltage source inverter or -three level inverter. It has high voltage single dc-power supply and auxiliary cascaded cells either are a full H-bridge or half H-bridge cells. Almost these topologies are suitable in medium voltage applications. It has low components counts as isolated dc-power supplies and switches. Nevertheless, it seems to have a high conduction loss since a zero voltage state in the pole requires switches (for half H-bridge) or (for full H-bridge) be in ON-state.
Obviously, from the above survey, there are many different topologies for MLI. Some of them use single dc-power supply and others use many dc-power supply s. In addition, some of them use many electrolytic capacitors as floating power supplies and some of them not. Almost all of addressed topologies suffering from increased number of components counts and usage of electrolytic capacitors as floating power sources which add more complicated problems in the control system. On the other hand, introducing new topology that can solve the stated challenges and proposing new factor for distinguishing different topologies are highly recommended.

This thesis is tackling to reduce the components count compared with the conventional and the addressed MLI topologies in the literature with keeping the same pole voltage levels number. This leads to reduced inverter size, minimized switching losses, low conduction losses, and simple control architecture.

In addition, a comparison strategy based on components per level factor has been proposed in this thesis. This factor is used to define the required components to produce one voltage level across the output pole. Therefore, it acts as a comparison tool that is describing how the different topologies of fully utilize their components. This factor is defined in (1). If this factor has a high value, this indicates that a large number of components counts are required to produce one pole voltage level and vice versa. Therefore, the research target is to decrease this factor.

$$F_{\frac{C}{L}} = \frac{N_C + N_D + N_{SW} + N_{PS} + N_{\text{taf}} + N_X}{N_{\text{Pole}}}. \quad (1)$$

2. MULTI-LEVEL INVERTER TOPOLOGIES

There are three well-known types of multilevel inverters the neutral point clamped (NPC) multilevel inverter, the flying capacitor (FC) multilevel inverter, and the cascaded H-bridge (CHB) multilevel inverter. The NPC multilevel inverter, also called diode-clamped, can be considered the first generation of multilevel inverter which was a three-level inverter. The three-level case of the NPC multilevel inverters has been widely applied in different industries. Unlike the NPC type, the FC multilevel inverter offers some redundant switching states that can be used to regulate the capacitors voltage. However, the control scheme becomes complicated. Moreover, the number of capacitors increases by increasing the number of voltage levels.

In the symmetric topology, the values of all of the dc voltage sources are equal. This characteristic gives the topology good modularity. However, the number of the switching devices rapidly increases by increasing the number of output voltage level. In order to increase the number of output voltage level, the values of the dc voltage sources are selected to be different, these topologies are called asymmetric. The CHB multilevel inverters have been industrially employed in several applications fields such as pump, fans, compressors, etc.

Table: I Existing Topologies Comparison

Presented in		N_{Pole}	N_{PS}	N_{SW}	N_D	N_C	N_{taf}	$F_{C/L}$
[11]		3	3	18	0	0	0	7.0
[12]		5	3	15	12	6	0	7.2
[13]		3	6	12	0	0	0	6.0
[14]		3	1	9	12	2	0	8.0
[15]		17	1	48	0	12	0	3.6
[16]		3	1	24	0	6	0	10.3
[17]		3	1	28	0	0	3	10.7
[18]	(a) four-level	4	3	18	0	4	0	6.3
	(b) five-level	5	3	24	0	4	0	6.2
	(c) six-level.	6	5	30	0	6	0	6.8
[19]		12	1	144	0	35	3	15.2
[20]		5	3	36	0	9	0	9.6
[21]	(a) the half-bridge based cell	3	1	12	0	6	0	6.3
	(b) the full-bridge based cell	5	1	24	0	6	0	6.2
	(c) the clamp-double	3	1	15	6	6	0	9.3
	(d) the three-level *FC*	3	1	12	0	6	0	6.3
	(e) the three-level *NPC*	3	1	12	6	6	0	8.3
	(f) the five-level cross-connected *SM.*	9	1	36	0	12	0	5.4
[22]	(a)Mixed commutation cells	4	1	18	0	6	0	6.3
	(b)Asymmetrical commutation cells	4	1	18	0	6	0	6.3
	(c) Cross connected commutation cells	5	1	24	0	6	0	6.2
	(d) Clamped double commutation cells	4	1	15	6	6	0	7.0
	(e) T-connected *NPC* using *RB* switch	3	1	12	0	6	0	6.3
	(f) Alternative Active *3-L NPC*	3	1	18	0	6	0	8.3
[24]	Hybrid *MLIs* topologies	6	7	30	0	0	0	6.2
[25]		7	8	36	6	0	0	7.1
[26]		6	13	30	0	0	0	7.2
[27]		3	4	12	0	0	0	5.3
[28]		3	6	12	0	0	0	6.0
[29]		4	3	11	20	0	0	8.5
[30]		5	3	18	24	6	0	10.2
[31]		5	6	24	0	0	0	6.0
[32]		5	6	24	0	0	0	6.0

In addition, they have recently been proposed for other applications like photovoltaic power-conversion system and wind power conversion.

The general three topologies of MLI are

2.1 Half-Bridge NPC Topology

This topology consists of a neutral point clamped (NPC) leg composed of eight transistors in series. The additional voltage levels are provided either by clamping the series of the dc-link capacitors with diodes or by employing flying capacitors

2.2 Cascaded Full-Bridge Topology

Another possibility to provide a multilevel output voltage is to connect in series multiple full-bridge structures. This solution needs several independent dc sources, i.e., multiple PV strings or transformers with multiple second arise and rectifiers. This requirement limits the adoption of this topology. A different approach, employing a transformer, allowed connecting in series various full-bridge structures using a single dc supply. The cascaded full-bridge allows multiple PWM strategies, i.e., carrier-based modulations or space-vector approaches. In the field of carrier-based PWM, unipolar and hybrid modulations can be applied.

3. HYBRID MULTI-LEVEL TOPOLOGY

Multilevel converters are nowadays widely adopted; the basic idea is that the dc-link voltage can be split between different capacitors, which can provide intermediate voltage levels between the reference potential and the dc-link voltage. The CHB multilevel inverters have been industrially employed in several applications fields such as pump, fans, compressors, etc. In addition, they have recently been proposed for other applications like photovoltaic power-conversion systemand wind power conversion. The topologies discussed previously are the conventional topologies. Many other multilevel inverter topologies have been introduced in recent years. One of the topologies is the modular multilevel inverter. This topology is simpler than the cascaded four-switch H-bridge-based inverter and has several advantages, such as modular extension to any number of levels and redundancy. However, the topology does not consider reduction in the number of components used. Other multilevel inverter topologies have been introduced. The multilevel inverter presented is based on symmetric topology and uses series/parallel connection of the dc voltage sources. This topology uses lower number of switches in comparison with the symmetric CHB multilevel inverter. The topologies presented, consider reduction in the components. These topologies are basically based on asymmetric topologies; hence, the used dc voltage sources have different values.

4. PROPOSED SYMMETRICAL TOPOLOGY

A new modular three-phase with reduced components count is proposed and studied in this paper. The suggested three phase symmetrical inverter is shown in Fig. 4.1 (a) Each arm consists of series connection of basic cells with a series connected switch, for example arm A is consists of one cell connected in series with switch Q_1.

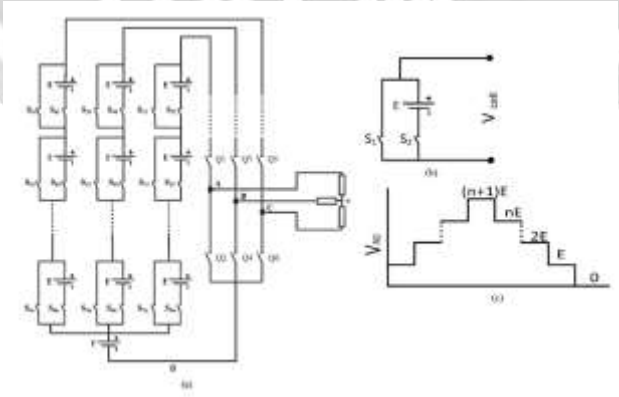

Fig-1: (a) generalized power circuit of the suggested three-phase symmetrical MLI. (b) Basic cell. (c) Pole voltage waveform for -cell.

Adding the common dc voltage source in to each arm forms the pole, creating the pole voltages. Adding the common dc voltage source in to each arm forms the pole, creating the pole voltages. In order to obtain the zero state pole voltage another switch Q2. is added to the pole, similarly Q4 and Q6 for pole. Fig. 4.1(b) shows the primary

basic cell, where each cell consists of two switches S1 and S2 and single dc voltage source. The two switches operate in a complementary fashion. Therefore, each cell can produce two voltage levels 0 and E. when S1 in ON-STATE, zero voltage is produced across the cell terminals, and when S2 in ON-STATE, E volt is applied across the cell terminals. Furthermore, using only one cell per each pole and applying suitable control signals to the S1, S2, Q1 and Q2 three voltage levels per pole (i.e.,0, E, 2E) are produced. The output pole voltage for cells connected in series configuration is shown in Fig. 4.1 (c).

TABLE II
DIFFERENT SWITCHING STATES AND THE CORRESPONDING OUTPUT VOLTAGES

Switching states	Switch				Basic-unit Output voltage	Pole voltage (V_{AO})
	S_1	S_2	Q_1	Q_2		
1	ON	OFF	ON	OFF	0	E
2	OFF	ON	ON	OFF	E	$2E$
3	OFF	OFF	OFF	ON	-	0

Table II summarizes the different switching states and the corresponding output voltages for both the basic cell and the pole voltage $_{VA}$ of the proposed topology. The proposed topology is a modular type therefore it can be extended to any levels. Equations (2)–(5) provide the relations of the proposed topology as

$$N_{\text{Pole}} = N_{\text{Cell}} + 2 \quad (2)$$

$$M_{\text{Level}} = 2N_{\text{Cell}} + 3 \quad (3)$$

$$N_{SW} = 3(2N_{\text{Cell}} + 2) \quad (4)$$

$$N_{PS} = 3N_{\text{Cell}} + 1. \quad (5)$$

Then for the example of N_{cell} = 1, N_{pole} =5, [based on (2)] which is the pole voltage levels and M_{level} =5 [based on (5)] which is the output line-to-line voltage levels. Note that the number of output phase voltage levels will be derived to be seven levels in low frequency modulation and nine levels for high frequency modulation.

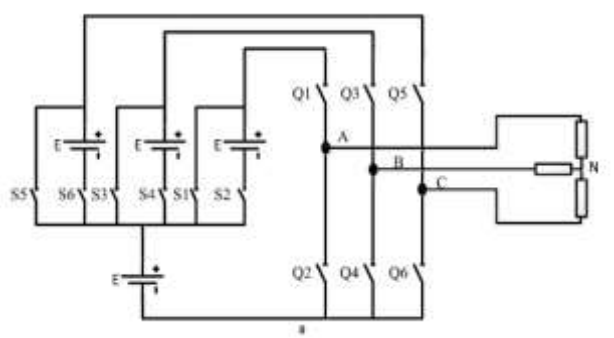

Fig-2: proposed MLI

5. MODULATION TECHNIQUES FOR THE PROPOSED MLI

The MLI modulation techniques are classified into two main groups according to the switching frequency used to drive inverter switches:

1) Low frequency modulation technique,

2) pulse- width modulation techniques that cover conventional techniques, sinusoidal pulse width modulation , space vector pulse width modulation , sub-harmonic pulse-width modulation , and switching frequency optimal pulse-width modulation [54]. In this paper, two modulation techniques are investigated to achieve sinusoidal output voltages waveforms as described in the following.

5.1. Low Frequency Modulation Technique

The low frequency modulation is considered as the basic modulation technique due to its lower switching frequency than the other modulation methods. It causes the switching loses reduced dramatically [55]. In order to investigate the performance of the proposed, a three levels per pole by using single basic cell in each pole is used as shown in Fig. 4.2. It is simulated via PSIM and MATLAB/SIMULINK software packages. In order to generate the required

switching signals for the proposed , a rectified sine waveform has a frequency equals to the output voltage frequency (50 Hz) is compared with a dc voltage signal has an amplitude equal to half of the sine wave amplitude as shown in Fig. 1.

TABLE III: SWITCHING STATES OF THE PROPOSED TOPOLOGY (SWITCH ON: 1, S WITCH OFF: 0)

V_{AB}	V_{BC}	V_{CA}	S_2	S_3	Q_1	Q_2	S_1	S_4	Q_3	Q_4	S_5	S_6	Q_5	Q_6
E	-2E	E	1	0	1	0	0	0	0	1	0	1	1	0
2E	-2E	0	0	1	1	0	0	0	0	1	0	1	1	0
2E	-E	-E	0	1	1	0	0	0	0	1	1	0	1	0
2E	0	-2E	0	1	1	0	0	0	0	1	0	0	0	1
E	E	-2E	0	1	1	0	1	0	1	0	0	0	0	1
0	2E	-2E	0	1	1	0	0	1	1	0	0	0	0	1
-E	2E	-E	1	0	1	0	0	1	1	0	0	0	0	1
-2E	2E	0	0	0	0	1	0	1	1	0	0	0	0	1
-2E	E	E	0	0	0	1	0	1	1	0	1	0	1	0
-2E	0	2E	0	0	0	1	0	1	1	0	0	1	1	0
-E	-E	2E	0	0	0	1	1	0	1	0	0	1	1	0

The intersection points between them identify six periods P1 to P6.

Four switching signals are constructed from these periods combination in order to generate a sinusoidal output voltage. The control equations for the S1, S2, Q1 and Q2 are presented. The same scenario is applied to inverter poles V_{BO} and V_{CO} after shifting the basic sinusoidal voltage with -120^0 and 120^0, respectively.

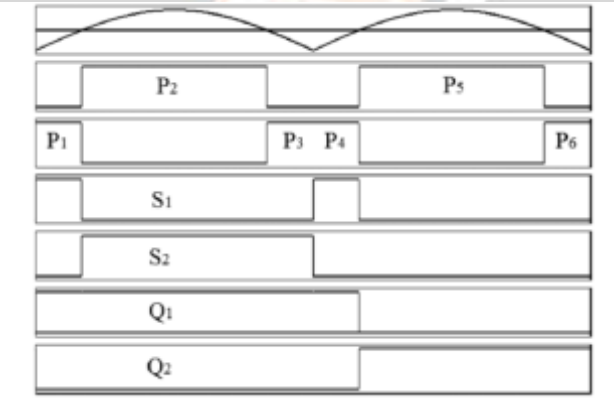

Fig.3 Switching patterns for low frequency modulation technique.

Therefore, the required switching signals for the overall three poles can be generated.

$$S_1 = P_1 + P_4 \quad (6)$$

$$S_2 = P_2 + P_3 \quad (7)$$

$$Q_1 = P_1 + P_2 + P_3 + P_4 \quad (8)$$

$$Q_2 = P_5 + P_6 \quad (9)$$

Balancing three phase output voltage can be achieved by operating the MLI according to switching states shown in Table III. The suggested MLI has 12 modes of operation per one cycle. It is essentially to note that: when switches Q1, Q5 and Q5 are in OFF-STATE, switches S1 *to* S6 have two possibilities for operation. Switches to may be in ON-STATE or at OFF-STATE. Both of them will not affect the output waveforms. However, keeping switches S1 to S6 in the OFF-STATE will reduce the overall voltage stresses on Q1, Q5 and Q5.

5.2. Sinusoidal Pulse-Width Modulation Technique (SPWM)

The straight way to generate the signals is to compare a sinusoidal waveform signal with a triangular waveform. The comparison operation will produce the Boolean signals that are required to synthesize the switches control pulses.

The SPWM technique is successfully applied for the proposed topology. Two different approaches have been proposed as follows.

(a) *Scheme I: SPWM Using Single Carrier Signal:*

This scheme uses one carrier signal centered with the sinusoidal modulation signal (sine waveform), and it has an amplitude equal to peak-to-peak value of the modulation signals as shown in Fig. 4. It worth mentioning that the modulation signal is shifted by dc level equals to, where is the carrier signal amplitude. The resulted Boolean output from the comparison between the carrier and the modulating signal produces the main pulse signal. Also the pulse signal is generated by comparing the modulating signal with zero value. After logical processing on and , the switching pulses and can be generated as specified in (10)–(15).

$$S_1 = (G_1 \times \overline{GP_1}) + (\overline{G_1} \times GP_1) \quad (10)$$

$$S_2 = (G_1 \times GP_1) \quad (11)$$

$$Q_1 = GP_1 + \{(G_1 \times \overline{GP_1}) + (\overline{G_1} \times GP_1)\} \quad (12)$$

$$Q_2 = \overline{\{\overline{GP_1} \times \overline{(G_1 \times \overline{GP_1})}\}} \quad (13)$$

where x stands for logic AND, stands for logic OR, stands for invert, and are the signals which will be applied to the gates drive belong to switches, respectively. In order to avoid dc-power sources short circuit, s1and s2 (Q1 and Q2) operate in a complementary mode with dead time.

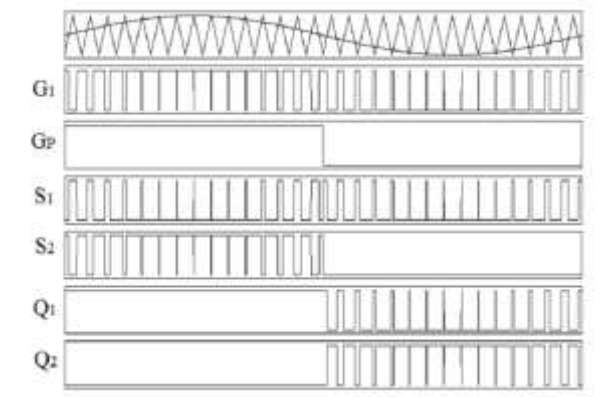

Fig.4 Switching patterns of the proposed MLI for scheme I.

(b) *Scheme II: SPWM Using Two Carrier Signals:*

This scheme compares single modulating signal with two identical and shifted in level carrier signals. Both of them have amplitude equal the modulating signal peak. In addition, the carrier signals are shifted by a dc offset equals to the carrier signal amplitude CR1 as shown in Fig. 5. Using the same procedure followed.

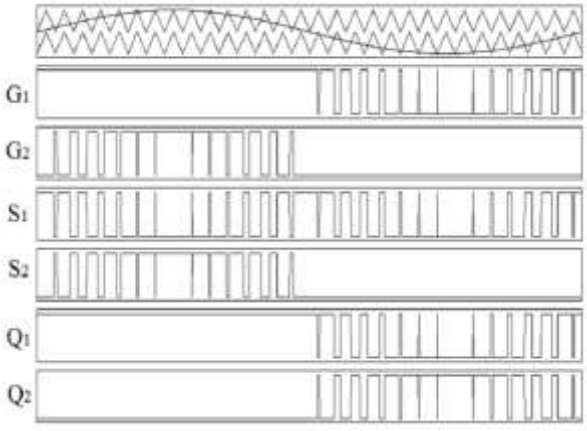

Fig 5 Switching patterns of the proposed MLI for scheme II.

in scheme I, scheme II can be executed. However, due to using two carrier signals, there are two Boolean signals named G1and G2 resulted from the comparison. By Carrying out several logical operations on these two signals G1 and G2as given in (14)–(17), the required control pulses for can be obtained.

$$S_1 = (G_1 \times \overline{G_2}) \quad (14)$$

$$S_2 = G_2 \quad (15)$$

$$Q_1 = \overline{\overline{G_2} \times \overline{(G_1 \times \overline{G_2})}} \quad (16)$$

$$Q_2 = \overline{G_2} \times \overline{(G_1 \times \overline{G_2})}. \quad (17)$$

6. SIMULATION OF PROPOSED MLI

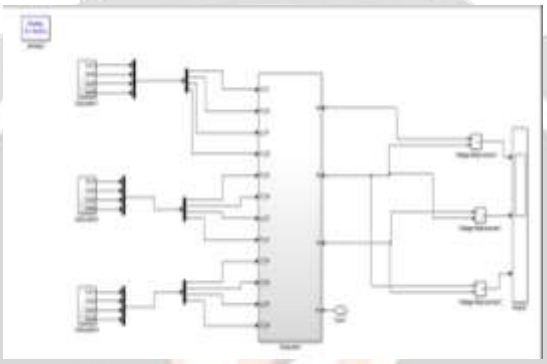

Fig.6 Matlab design of proposed system

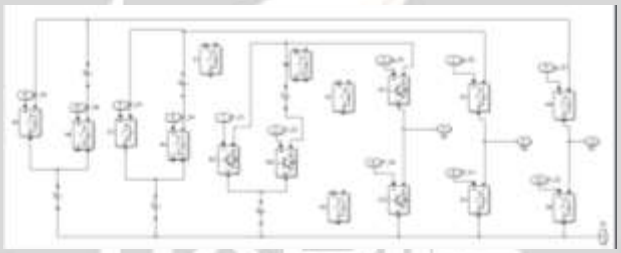

Fig-7: Proposed Inverter Topology

A. Switching patterns for low frequency modulation technique.

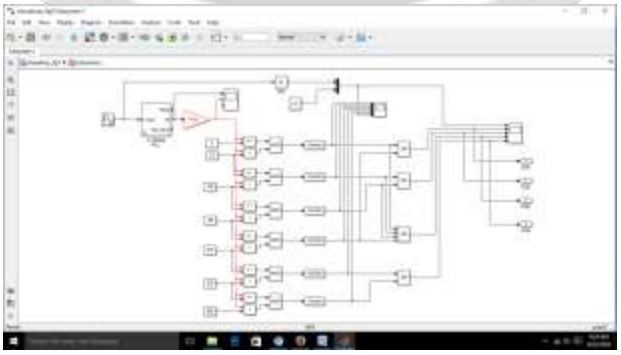

Fig-8: low frequency modulation technique.

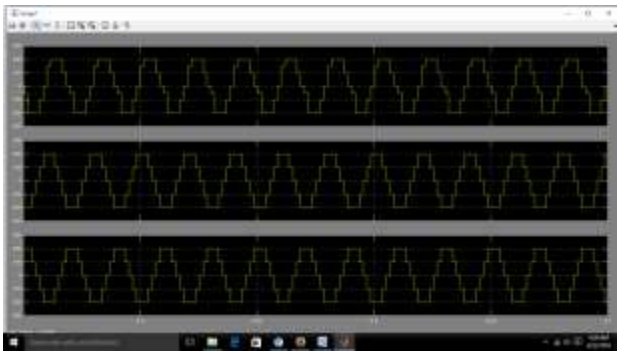

Fig-9: Output Five-level voltage of Inverter

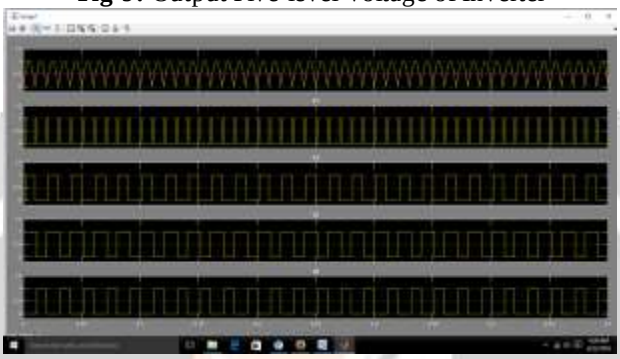

Fig-10: Gate pulses

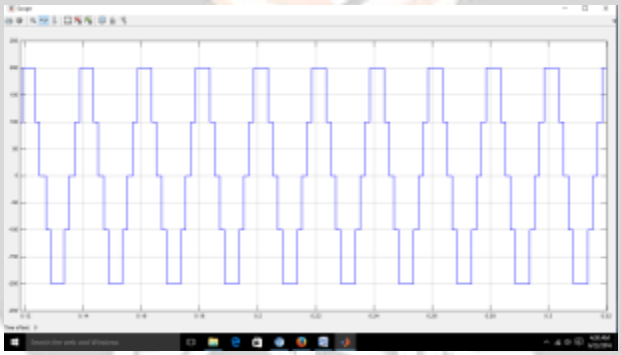

Fig-11: Five-level Output voltage of Inverter

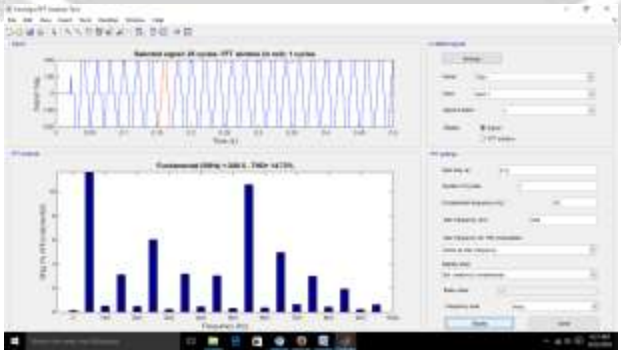

Fig-12: FFT Analysis

B. Switching patterns of the proposed MLI for scheme II.

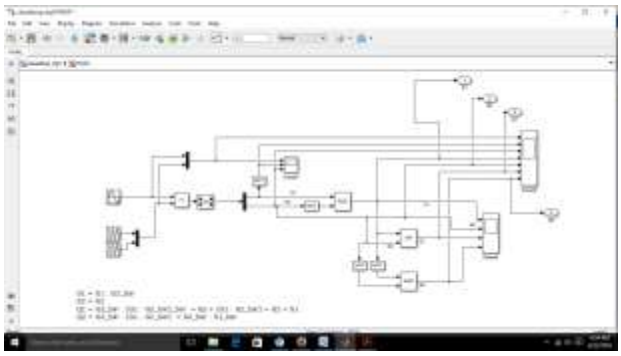

Fig-13: Multi-carrier PWM

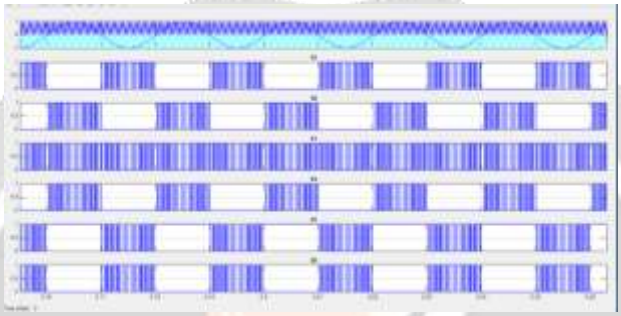

Fig-14: PWM Pulses

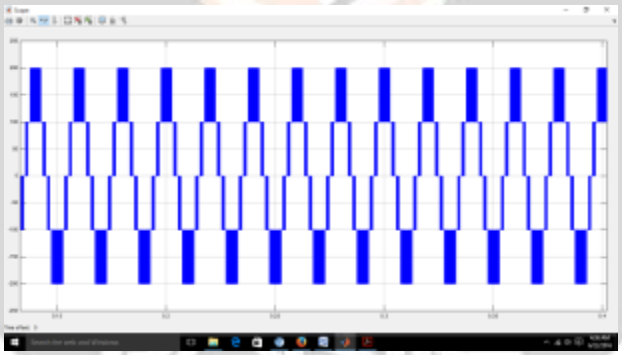

Fig-15: Output Voltage for Multi-carrier PWM

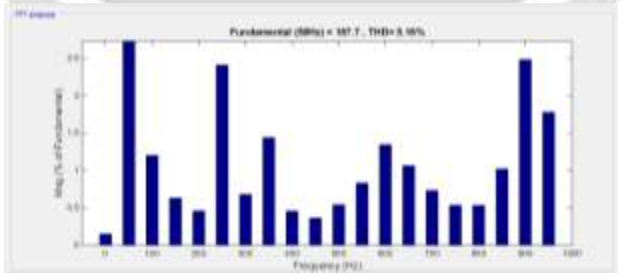

Fig-16: FFT Analysis

7. CONCLUSIONS

Three phase eleven level inverter topology with less number of switches is proposed and simulated. Various PWM methods are analyzed and compared. From the simulation results, it was found that VF-PWM provides minimum THD of 12.51% in the inverter output voltage. This will be the best PWM technique for inverter switching because

small inductance can be used in the LC filter placed in series to the inverter output to produce a rectified AC sine wave of low THD of 1.77%.

8. REFERENCES

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