ANALYSIS AND DESIGN OF THREE PHASE MULTI-LEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES

V. Nagarani [1], MD. Abdul Nadeem [2]

[1] *Student, EEE Department, Nigama Engineering College, Telangana, India*
[2] *Asst.Prof, EEE Department, Nigama Engineering College, Telangana, India*

ABSTRACT

A multilevel inverter for generating multiple voltage levels using a series-parallel connection of modules with intermediate power source has been proposed. As compared to conventional inverter topologies like diode clamped and capacitor clamped inverters, the cascaded multilevel inverter has lesser harmonics as well as lower switching stress. The cascaded topology has more number of power switches leading to greater heat losses, larger size, higher cost and more gate drive circuitry. The proposed configuration contains less number of switches and produces lesser harmonics in the output voltage than the cascaded topology. To analyze the performance of the proposed circuit SPWM technique has used. The results have been verified through simulation study in MATLAB/Simulink in order to select the best PWM method that provides minimum THD in the output voltage. An LC filter has been designed to improve the harmonic profile

Keyword: - *Multilevel inverter, PWM technique, total harmonic distortion, LC filters.*

1. INTRODUCTION

Recently Power electronic devices play a major role in the conversion and control of electric power, especially to extract power from renewable energy sources like photovoltaic array and wind energy [1]. Conversion of DC to AC power can be done with the help of inverters (single phase or three phases). Conventional bipolar inverters produce alternating staircase waveforms with higher harmonics. Thus, the multilevel inverters (MLI) were developed [2]. This paper provides a new three phase configuration to produce the multi-level output with less total harmonic distortion (THD) in its output voltage. IPD, APD, CO and VF PWM techniques were used to produce switching pulses [3].

The cascaded H-bridge (CHB) configuration has lesser number of components as compared to the conventional diode clamped or capacitor clamped inverters [4]. It contains single phase inverters connected in series with separate DC sources that can be derived from renewable energy sources like solar PV cell, bio fuel cell or wind turbine [5]. Each single phase inverter produces two DC voltage levels. Bridges with separate DC sources are cascaded to each other for more DC levels. The switches operate at fundamental frequency of 50Hz. The diode clamped MLI has 20 switches, 90 diodes and 10 main DC-bus capacitors per phase to produce an 11- level staircase as the output voltage. The capacitor clamped MLI uses 20 switches, 45 clamping capacitors and 10 main DC-bus capacitors per phase whereas the cascaded H-bridge inverter uses only 24 switches per phase to produce the same output [6-7]. This paper describes a single phase inverter configuration with eight switches and three DC sources. A three phase multilevel inverter is obtained by interconnecting three single phase inverters to a star connected pure resistive load with a common earth point. Therefore, this circuit offers lesser gate control circuitry, lesser cost, lesser heating, more ease of installation and lesser electromagnetic interference.

Table.I shows the comparison of the number of components between different topologies. The performance of the inverter using IPD, APD, CO and VF PWM methods is shown [8]. A passive series LC filter is designed to produce a sine wave from the staircase inverter output. The purpose of the output LC filter is attenuating voltage ripples due to the inverter switching

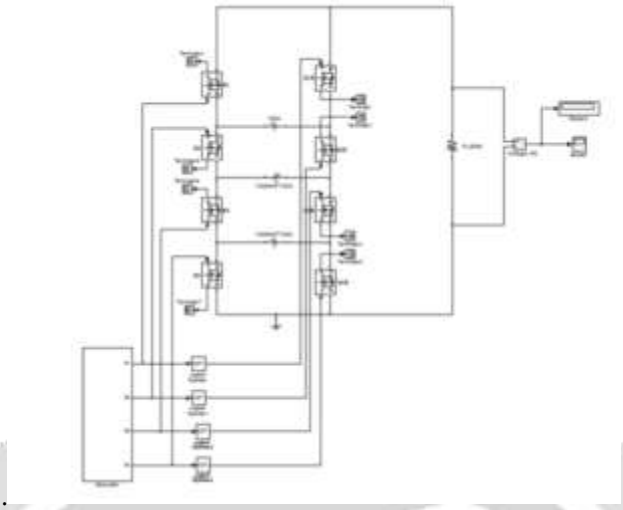

Fig-1: circuit diagram of a single-phase 11 level inverter

The diode clamped MLI has 20 switches, 90 diodes and 10 main DC-bus capacitors per phase to produce an 11-level staircase as the output voltage. The capacitor clamped MLI uses 20 switches, 45 clamping capacitors and 10 main DC-bus capacitors per phase whereas the cascaded H-bridge inverter uses only 24 switches per phase to produce the same output . This project describes a single phase inverter configuration with eight switches and three DC sources. A three phase multilevel inverter is obtained by interconnecting three single phase inverters to a star connected pure resistive load with a common earth point. Therefore, this circuit offers lesser gate control circuitry, lesser cost, lesser heating, more ease of installation and lesser electromagnetic interference.

Tab No- I: NUMBER OF COMPONENTS PER PHASE FOR DIFFERENT 11-LEVEL INVERTER TOPOLOGIES

Sl.No.	*Configuration*	*Number of switches per phase*	*Number of conducting switches per phase*
1	Diode Clamped	20	4
2	Capacitor Clamped	20	4
3	Cascaded H-Bridge	24	14
4	Eight switch type	8	4

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2. PROPOSED TOPOLOGY AND ITS OPERATION

The proposed inverter configuration has eight switches and three DC sources per phase as shown in Fig.l. The series combination among the three DC sources Vdc, 2Vd c and 2Vd c can be used to produce eleven DC levels at the inverter output in a single cycle. Fig.2 provides the simulation operate simultaneously.

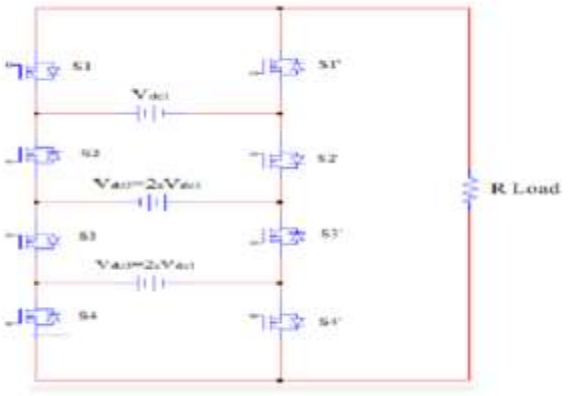

Fig-2: Proposed configuration for single phase inverter

Tab No-II: SWITCHING STATES IN 11-LEVEL INVERTER

Output Voltage	S1	S2	S3	S4	S1B	S2B	S3B	S4B
$+5V_{dc}$	1	0	1	0	0	1	0	1
$+4\ V_{dc}$	0	0	1	0	1	1	0	1
$+3\ V_{dc}$	1	0	1	1	0	1	0	0
$+2\ V_{dc}$	0	0	1	1	1	1	0	0
$+\ V_{dc}$	1	0	0	0	0	1	1	1
0	0	0	0	0	1	1	1	1
$-\ V_{dc}$	0	1	1	1	1	0	1	1
$-2\ V_{dc}$	1	1	0	0	0	0	1	1
$-3\ V_{dc}$	0	1	0	0	1	0	1	1
$-4\ V_{dc}$	1	1	0	1	0	0	1	0
$-5V_{dc}$	0	1	0	1	1	0	1	0
0	1	1	1	1	0	0	0	0

The below figure shows the conducting switches at different operating states. +Vdc level voltage is obtained by turning on the switches S_1, S_2B, S_3B and S_4B together. Similarly, all the DC output voltage levels are obtained as shown in T ABLE above.

2.1 Operation of switches of the circuit at different voltage levels

(a)During 0v operation the switches S1B, S2B, S3B, and S4B are in on mode .the direction of flow is shown in the below figure.3

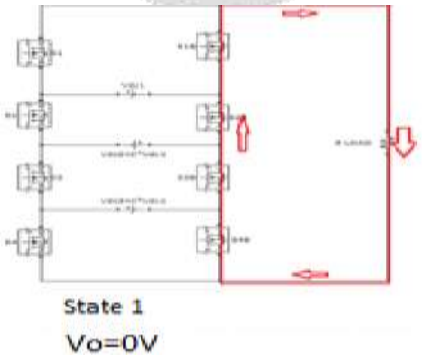

Fig-3: STATE1

(b).During 1v level operation the switches S_1, S_{2B}, S_{3B}, S_{4B} are in the on mode and the direction of flow is shown in side figure.4

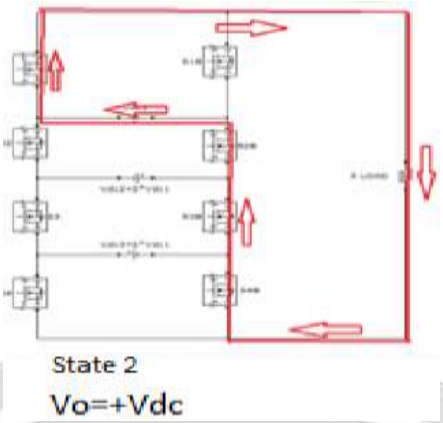

Fig-4: STATE 2

(c). During 2V operation the switches S3, S4, S1B, and S2B are in on mode. The direction of flow is shown in fig. 5

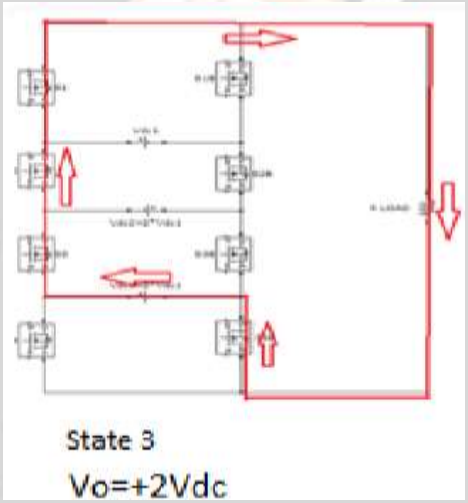

Fig.5 STATE 3

(d) During 3V operation the switches S1, S3, S4, and S2B are in on position and the direction of flow of voltage is given in the figure.

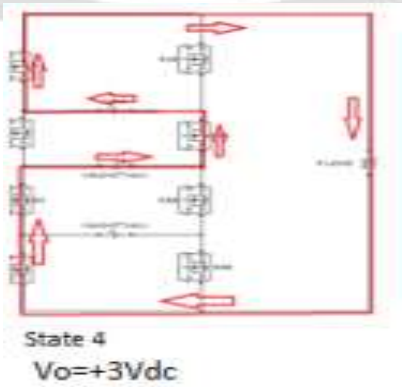

Fig. 6 STATE 4

3. MODULATION SCHEMES

To control the frequency and harmonics of the output voltage of the inverter, we must select the most appropriate PWM technique. The sinusoidal PWM (SPWM) method has been applied to the power switches, in which a reference sinusoidal wave of fundamental frequency is compared to high frequency carrier wave(s). The level, frequency or amplitude of the multiple carrier signals are varied based on the PWM technique. The modulation indices are kept same in all the methods for comparison. Amplitude modulation index is the ratio of the amplitude of the reference sine wave to the amplitude of the carrier waves. Frequency modulation index is defined as the ratio of the frequency of carrier wave to the frequency of the modulating wave. Amplitude modulation index M_a and frequency modulation index m_r are given by and respectively.

$$m_a = A_m / A_c$$

$$m_f = f_c / f_m$$

The PWM techniques discussed in this project are In Phase Disposition (lPD) type level shift pulse width modulation (LS-PWM), Anti-Phase Disposition (APD) PWM, Carrier Overlap (CO) PWM and Variable Frequency (VF) PWM. The amplitude modulation index rna is maintained at 0.9 and the frequency modulation index mr at 200. The RMS value of the fundamental component of the output voltage and the total harmonic distortion (THD) are observed by using simulation results. In all the PWM techniques, 'N' number of carrier signals are used to obtain 2N+1 voltage levels.

3.1 In-Phase Disposition Level-Shift PWM (IPD-LSPWM) Method

The carrier signals are level shifted in this PWM technique. They have the same amplitude of 1 V and a frequency of 10 kHz. The level shifted carrier signals are compared with a diode bridge rectified reference sine wave which is at fundamental frequency, as illustrated in Fig.4. The different levels of the output wave is detected and decoded to produce the pulses required to trigger each switch in the inverter. In order to obtain a three phase inverter, the sine wave is phase shifted by 120°.

3.2 Anti-Phase Disposition Level-Shift PWM (APD-LSPWM) Method

Each carrier signal is out of phase with neighboring carrier signals by 180° and have the same amplitude and frequency. The carrier signals are compared with the reference sine wave (which is at fundamental frequency) to produce required gate pulses as shown in Fig

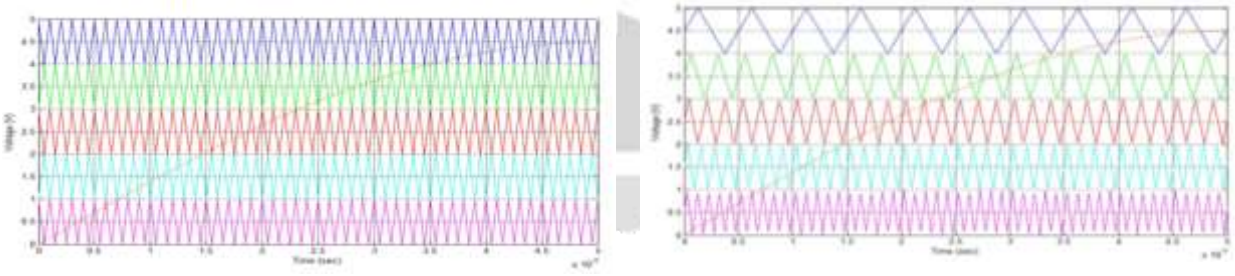

Fig-7: Reference sine wave and carrier wave for APD-PWM method at ma=0.9 and mf=200.

3.3 Carrier Overlap PWM (CO-PWM) Method

This strategy utilizes level shifted carrier waves of the same frequency and amplitude. They are in phase with each other and also overlap each other. They are compared to a diode bridge rectified reference sine wave in Fig.6 in order to produce the gate pulses.

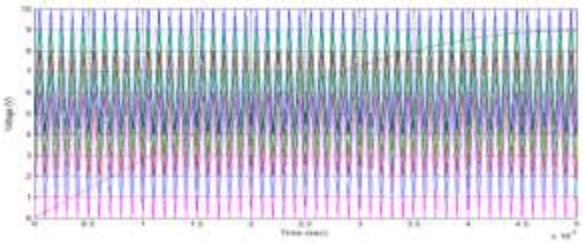

Fig-8: Reference sine wave and carrier wave for CO-PWM method at ma=0.9 and mf=200.

3.4 Variable Frequency PWM (VF-PWM) Method

All the level-shifted carrier waves have the same amplitude. The lowermost carrier wave has very high frequency, 10kHz followed by 8kHz, 6kHz, 4kHz and the uppermost carrier signal has lowest frequency, 2kHz. They are compared with the reference sine wave with fundamental frequency to produce required switching pulses.

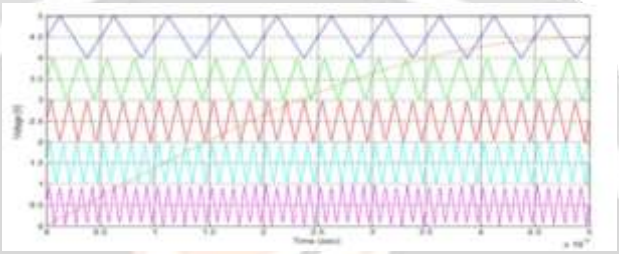

Fig-9: Reference sine wave and carrier wave for VF-PWM method.

4. SIMULATION RESULTS

This section deals with simulation of the proposed system from fig.10 to fig.17

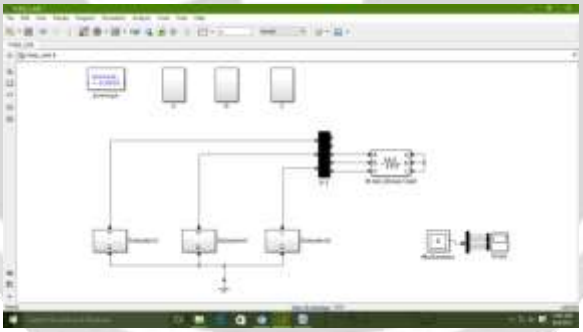

Fig-10: simulation of proposed circuit

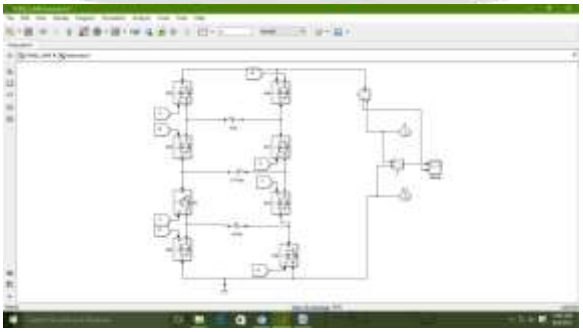

Fig-11: matlab circuit for the three phase 11 level inverter using IPD technique using lc filter

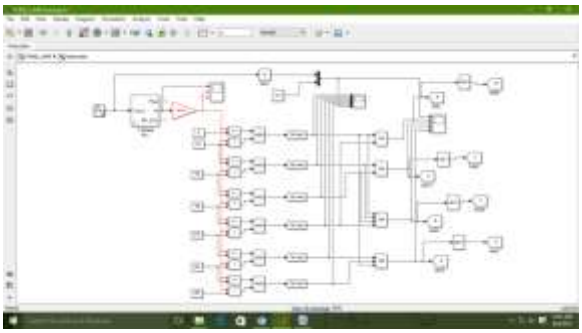

Fig-12: controller design

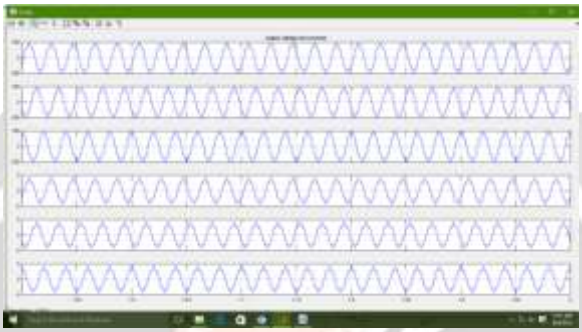

Fig-13: output voltage waveform

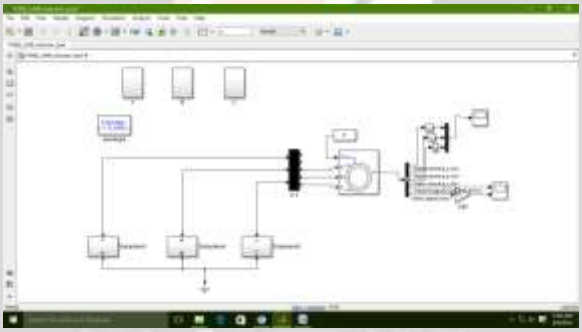

Fig-14: Proposed method with Induction motor output

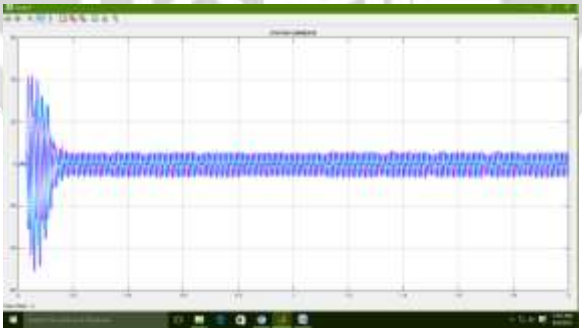

Fig-15: stator currents of induction motor

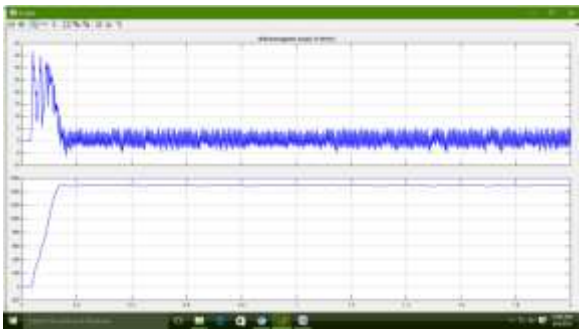

Fig-16: Torque and speed of induction motor

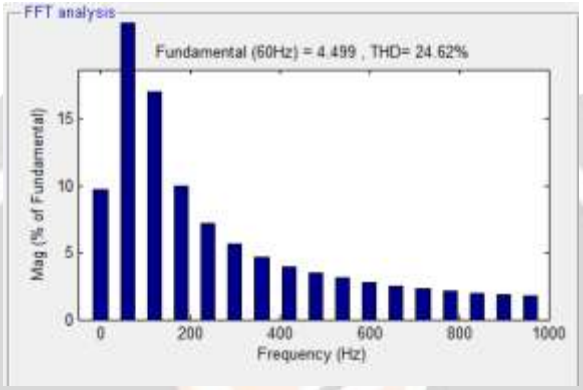

Fig-17: FFT Analysis of the harmonic spectrum for VF PWM technique (with LC filter)

4. CONCLUSIONS

Three phase eleven level inverter topology with less number of switches is proposed and simulated. Various PWM methods are analyzed and compared. From the simulation results, it was found that VF-PWM provides minimum THD of 12.51% in the inverter output voltage. This will be the best PWM technique for inverter switching because small inductance can be used in the LC filter placed in series to the inverter output to produce a rectified AC sine wave of low THD of 1.77%.

5. REFERENCES

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