ANALYSIS OF ASYMMETRICAL MULTILEVEL INVERTER FED TO INDUCTION MOTOR

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ABSTRACT

This paper proposes comparison between Asymmetrical Cascaded 7 level and 9 level Multilevel Inverter (MLI) using multicarrier based Level shift Pulse Width Modulation Technique (LSPWM) with induction motor load. This control scheme is applied to 7 level and 9 level Asymmetrical Cascaded Multilevel Inverter (CMLI). Different topologies of multilevel inverter have been reported in the literature, but this work mainly focuses on the asymmetrical cascaded multilevel inverter circuit with reduced number of input DC sources. Here PWM switching techniques for Asymmetrical cascaded multilevel inverters is Phase disposition (PD) . THD and motor output are analyzed in FFT window. The results are observed by MATLAB/SIMULINK software.

Keyword: - *Asymmetrical CMLI, LSPWM, THD, PD, IGBT, Induction Motor*

1. INTRODUCTION

An induction motor is a paradigm of asynchronous AC machine, which consists of a stator and a rotor. This motor is extensively used because of its well-built features and sensible cost. Induction motors are used in many industrial applications such as heating, ventilation, air conditioning systems, waste water treatment plants, blowers, fans, textile mills, and in rolling mills, etc. An electromagnetic field is generated when sinusoidal voltage is applied to the stator, in the induction motor. A current in the rotor is induced due to this field, which creates an added field that tries to align with the stator field, causing the rotor to revolve. When a load is applied to the motor a slip is formed between these fields. Compared to the synchronous speed, the rotor speed diminishes, at advanced slip values. The frequency of the stator voltage controls the synchronous speed [2]-[3]. The frequency of the voltage is applied to the stator through power electronic devices, which permits the control of the speed of the motor. Finally, the torque begins to fall when the motor reaches the synchronous speed. For many power converter applications, it is desirable for the converter to output a desired waveform with minimum distortion. For example, a DC-AC converter is desired to output a purely sinusoidal waveform. But for the practical converters, they can just output a series of rectangular waves. The key issues for the control of the converters are to get the modulation methods to control the output rectangular waves to synthesize the desired waveforms. Therefore, a modulation control method needs to generate desired fundamental frequency voltage and eliminate other higher order harmonics as much as possible.

Today, the Fourier transformation method has been used to develop all kinds of modulation methods. The most popular modulation method for bi-level converters is the PWM method. Traditional PWM methods employ switching frequencies on the order of several kHz. The traditional PWM methods employ much higher switching frequencies for two reasons. The first reason concerns harmonics. Undesirable harmonics occur at much higher frequencies. Thus, filtering is much easier and less expensive. The second reason concerns audible noise. Several kHz is well above the acoustic noise level. Also, if the generated high frequency harmonics are above the bandwidth of some actual systems, there is no power dissipation due to these harmonics [14]. But as mentioned above, traditional PWM schemes have the inherent problems of producing electromagnetic interference (EMI). Rapid changes in voltages (dv/dt) are a source of EMI. The presence of a high dv/dt can cause damage to electrical motors. A high dv/dt produces common-mode voltages across the motor windings. Furthermore, higher switching frequencies can make this problem worse due to the increased number of times these common-mode voltages are applied to the motor during each fundamental cycle. Problems such as motor bearing failure and motor

winding insulation breakdown can result due to circulating currents and voltage surges [2]. Also, long current-carrying conductors connecting equipment can result in a considerable amount of EMI.

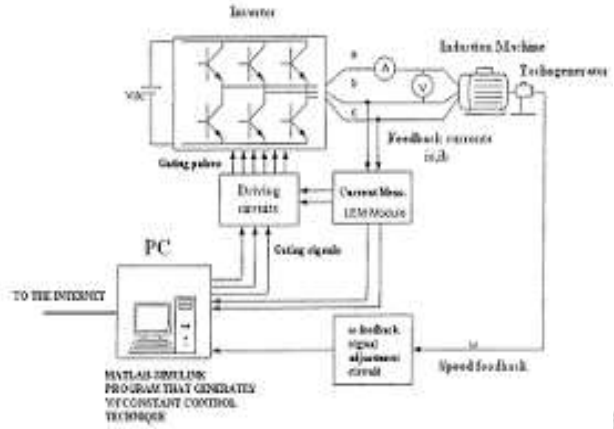

Fig-1: Block Diagram Schematic of V/f control of VSI fed 3- phase Induction Motor Drive

Multilevel converters inherently tend to have a smaller dv/dt due to the fact that switching involves several smaller voltages. Furthermore, switching at the fundamental frequency will also result in decreasing the number of times these voltage changes occur per fundamental cycle. The key issue for multilevel converter modulation is the harmonics elimination. The multilevel fundamental switching method inherently provides the opportunity to eliminate certain higher order harmonics by varying the times at which certain switches are turned "on" and turned "off", which is also called varying the switching angles. Harmonic elimination is performed for several reasons. The first reason is harmonics are a source of EMI. Without harmonic elimination, designed circuits would need more protection in the form of snubbers or EMI filters [14]. As a result, designed circuits would cost more. The second reason is that EMI can interfere with control signals used to control power electronics devices and radio signals. The third reason is that harmonics can create losses in power equipment. For example, harmonic currents in an electrical induction motor will dissipate power in the motor stator and rotor windings. There will also be additional core losses due to harmonic frequency eddy currents. The fourth reason is that harmonics can lower the power factor of a load. Increased harmonic content will decrease the magnitude of the fundamental relative to the magnitude of the entire current. As a result, the power factor would decrease [14].

It was mentioned earlier that an increase in the number of DC voltages in a multilevel converter results in a better approximation to a sinusoidal waveform. Furthermore, the increased number of DC voltages provides the opportunity to eliminate more harmonic contents. Eliminating harmonic contents will make it easier to filter the remaining harmonic content. As a result, filters will be smaller and less expensive. The second advantage of multilevel converters concerns switch ratings. Since multilevel converters usually utilize a large number of DC voltages, several switches are required to block smaller voltages. Since switch stresses are reduced, required switch ratings are lowered.

The third advantage of multilevel converters concerns system reliability. If a component fails on a multilevel converter, most of the time the converter will still be usable at a reduced power level. Furthermore, multilevel converters tend to have switching redundancies. In other words, there might be more than one way to produce the desired voltage [14]. The fourth advantage of multilevel converters concerns application practicality. As an example, consider designing a converter for a large HEV. Such an application would require excessively large components to deal with the relatively large working voltages and currents. These large components are expensive, bulky, and generally not reliable. However, multilevel converters allow for the utilization of smaller, more reliable components.

One disadvantage of multilevel converters is that they require more devices than traditional converters. The system cost may increase (part of the increased cost may be offset by the fact switches with lower ratings are being used). Using more devices also means the probability of a system failure will increase. Another disadvantage of multilevel converters concerns control of the switches. The increased number of switches will result in more complicated control. There are four kinds of control methods for multilevel converters. They are the

1. Selective harmonic elimination method.

2. space vector control method
3. traditional PWM control method and
4. Space vector PWM method.

The traditional PWM, space vector PWM and space vector modulation methods cannot completely eliminate harmonics. Another disadvantage is space vector PWM and space vector modulation methods cannot be applied to multilevel converters with unequal DC voltages. The carrier phase shifting method for traditional PWM method also requires equal DC voltages. Until now, the number of harmonics the selective harmonic elimination method can eliminate is not more than the number of the switching angles in the transcendental equations. Due to the difficulty of solving the transcendental equations, real-time control of multilevel converters with unequal DC voltages is impossible now. No such method can be used to directly compute the output voltage pulses to eliminate any number of the harmonics without any restriction of the number of unknowns in the harmonic equations and available solutions for the equations. For these reasons, in this thesis, a new modulation control method for multilevel converters is developed and referred to as the active harmonic elimination method.

The active harmonic elimination method contributes to the existing methods on it not only generates the desired fundamental frequency voltage, but also completely eliminates any number of the specified harmonics without the restriction of the number of unknowns in the harmonic equations and available solutions for the harmonic equations. Also the active harmonic elimination method can be applied to both equal DC voltage cases and unequal DC voltage cases. The method is referred to as the active harmonic elimination method because the converter itself can eliminate a specific harmonic. For a traditional bi-level converter, to eliminate a specific harmonic in the output voltage, a specific filter is required.

The paper is arranged as follows: stage I presents introduction to the project. It deals with back ground history and problem statements and organization of thesis. stage II presents a summary of the existing literature and the state-of–art in multilevel converter topologies and control technologies. The advantages and disadvantages of various multilevel converter topologies and control technologies are discussed. At the end of the chapter, a summary of "what is already done" and "what needs to be done next" will be given. stage III explains the resultant method used to eliminate the low order harmonics for a multilevel converter, and develops the Newton Climbing method to eliminate higher order harmonics based on the harmonics elimination theory. The triplen harmonic compensation method to extend the modulation index range and decrease the required DC voltage level number is developed in this chapter, too. stage IV presents the active harmonic elimination method for equal DC voltage cases. stage V extends the active harmonic elimination method for multilevel converters with unequal DC voltages. optimizes the active harmonic elimination method and improves its control performance. It can be seen in this chapter that the active harmonic elimination method dramatically expands the scope of the traditional selective harmonic elimination method. Implementation of the active harmonic elimination method on an 11-level multilevel converter. Experiments validate the active harmonic elimination method. stage VI concludes the thesis's work and gives future research directions.

2. CASCADED MULTILEVEL INVERTER TOPOLOGY AND ITS OPERATION

A cascaded H-bridge converter is several H-bridges in series configuration [2], [7], [8], [12]. A single H-bridge is shown in Figure 2. A single H-bridge is a three-level converter. The four switches S_1, S_2, S_3 and S_4 are controlled to generate three discrete outputs V_{out} with levels V_{dc}, 0 and -V_{dc}. When S_1 and S_4 are on, the output is V_{dc}; when S_2 and S_3 are on, the output is $-V_{dc}$; when either pair S_1 and S_2 or S_3 and S_4 are on, the output is 0. A H-bridge cascaded multilevel converter with s separate DC sources is shown in Figure 3. A staircase sinusoidal waveform can be generated by combining specified output levels, which is shown in Figure 2

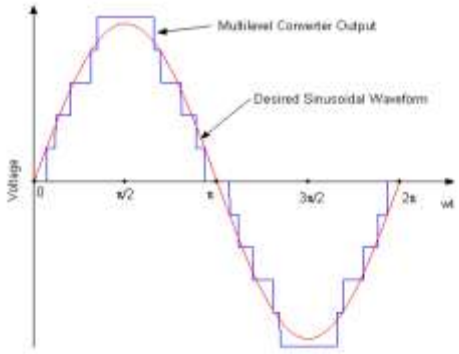

Fig-2: Staircase sinusoidal waveform generated by H-bridge cascaded multilevel converter

The number of output phase voltage levels m in a cascade converter with s separate DC sources is $m = 2s+1$. Load balance control for each H-bridge and each DC source can be acquired by rotating the switching angles to the H-bridges [6]. The advantages for cascaded multilevel H-bridge converter are the following:

(1) The series structure allows a scalable, modularized circuit layout and packaging due to the identical structure of each H-bridge.

(2) No extra clamping diodes or voltage balancing capacitors is necessary.

(3) Switching redundancy for inner voltage levels is possible because the phase voltage is the sum of each bridge's output.

The disadvantage for cascaded multilevel H-bridge converter is the following:

Needs separate DC sources; Another kind of cascaded multilevel converters with transformers using standard three-phase bi-level converters has recently been proposed [8]. The circuit is shown in Figure 2.8. The converter uses output transformers to add different voltages. In order for the converter output voltages to be added up, the outputs of the three converters need to be synchronized with a separation of 120° between each phase. For example, obtaining a three-level voltage between outputs *a* and *b*, the output voltage can be synthesized by $V_{ab} = V_{a1\text{-}b1} + V_{b1\text{-}}$ (b).During 1v level operation the switches S_1, S_{2B}, S_{3B}, S_{4B} are in the on mode and the direction of flow is shown in side figure.4

3. PROPOSED ASYMMETRIC MLI

Hybrid Multilevel Inverter was introduced by means of all 3M possible output voltages, where M is the number of modules allied in series. Though this inverter uses extremely different DC voltage sources in the relation of 1:3:9 etc. In distinguish, the DC voltage sources consider in this paper are still exceptionally close to each other, they fluctuate only by ±20 %. The quantity of cells in sequence determines the number of output levels. 3M= 27 switching states SI, when M= 3 cells. With similar DC voltages, there are numerous switching states that create the same output voltages, resulting in 2.M + 1 = 7 different phase output voltage levels. Uneven DC source voltages direct to an improved number of different output voltage levels. The maximum number of levels is 3M = 27. With the DC source voltages distributed as Viii :Vi12 : Vil3 = 1 Vdc : 3VDc : 9VDc, all the dissimilar output voltage levels are consistently spaced. The aim of such an inverter (Hybrid Multilevel Inverter) has the disadvantage that the preliminary modularity is vanished. Each module must be intended for the equivalent voltage class.

When the DC source voltages are uneven but only ±20 % unlike from each other, the number of different output voltage levels is also superior. As an instance, we believe a case where one cell has 100 % of its nominal DC voltage, other has 120% and the third one has 80%. The DC source voltages are in relation of 4:5:6 in this scheme. As can be seen, the voltage levels are approximately the same as in the 1:3:9 case, apart from some levels not there at high complete values of output voltage. In order to consider the possible benefits of using unlike DC voltages, the 4:5:6 relation is used as an instance in the following part. For a first estimation it is abandoned if these differences are introduced by the moment behavior of the DC voltages, or if they are introduced by design and thus can be supposed to be stable. The second case is considered at this time for the sake of simplicity.

Table I: Switching pattern for asymmetrical cascaded nine level inverter

Output	4V	3V	2V	V	0	-V	-2V	-3V	-4V
S1	1	1	0	1	0	0	0	0	0
S2	1	1	1	1	0	0	1	0	0
S3	0	0	0	0	0	1	0	1	1
S4	0	0	1	0	0	1	1	1	1
S5	1	1	1	0	0	0	0	0	0
S6	1	1	1	1	0	1	0	0	0
S7	0	0	0	0	0	0	1	1	1
S8	0	0	0	1	0	1	1	1	1
S9	1	0	0	0	0	0	0	0	0
S10	1	1	1	1	0	1	1	1	0
S11	0	0	0	0	0	0	0	0	1
S12	0	1	1	1	0	1	1	1	1

The below figure shows the output wave forms the proposed asymmetrical converter. It is clearly seen that the level of inverter varies with the change in the ratios of input voltage. The inverter gives 7 level output voltage when the ratio is 1: 1: 1, while it gives 23 level output voltage when the ratio is 4:5:6 and it gives 27 level output voltage when the ratio is 1: 3: 9. This inverter having 3 bridges connected in series gives different levels of output voltages without changing the circuit except the ratios of input voltages. Switching of the converter is done by following the staircase control technique. Pulse width Modulation technique can also be applied by appropriate calculation of the switching time period.

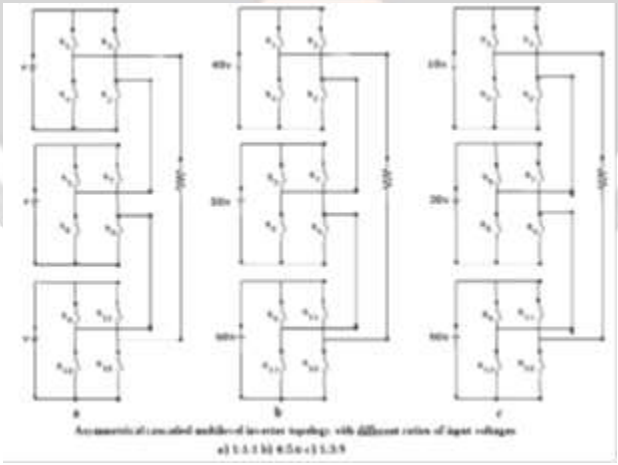

Fig. 3: Proposed asymmetrical cascaded multilevel inverter with different voltage ratios

4. SIMULATION RESULTS

4.1 Asymmetric Nine-level Inverter

This section deals with simulation of the proposed system from fig.10 to fig.17

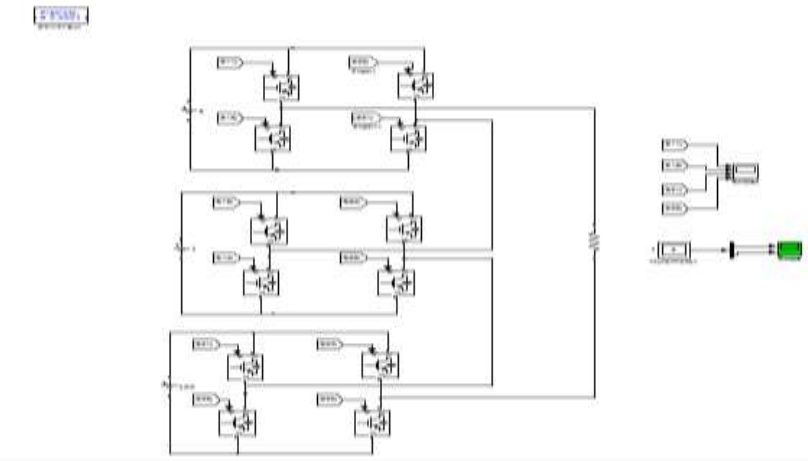

Fig.5: Matlab design of Asymmetric 9-level

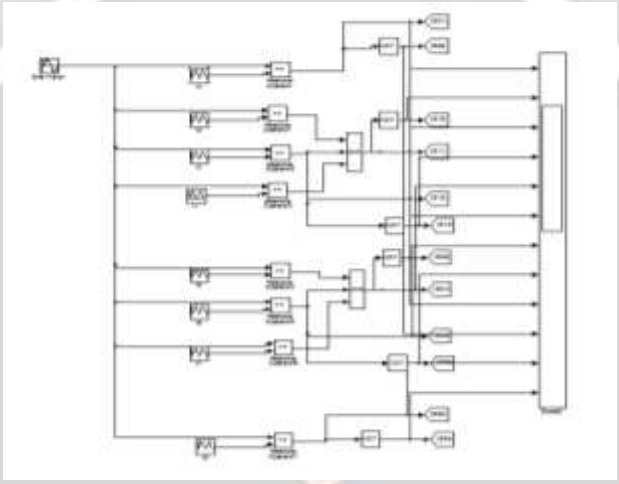

Fig-6: Proposed Phase disposition PWM technique

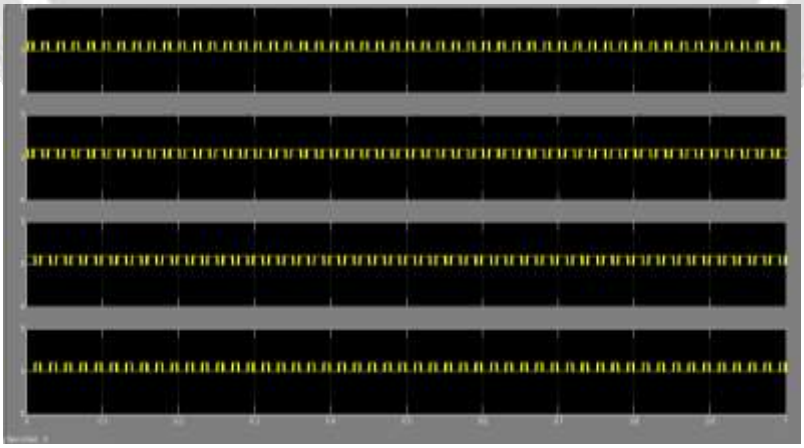

Fig-7: PWM pulses

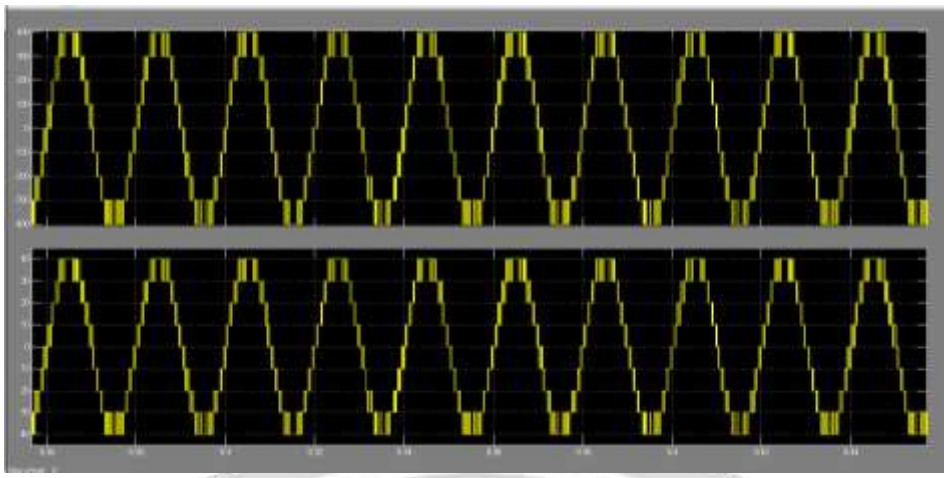

Fig-8: Output voltage waveform

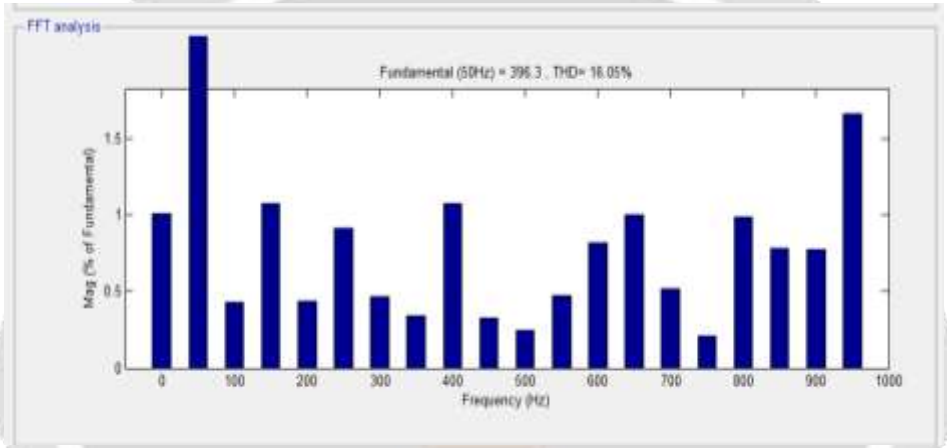

Fig-9: FFT analysis

4.2. Asymmetric 27-level inverter

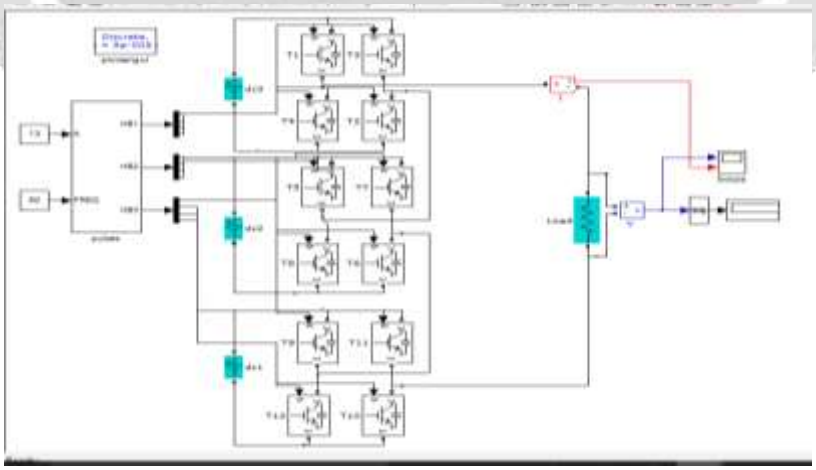

Fig.10 MATLAB design of 27-level inverter

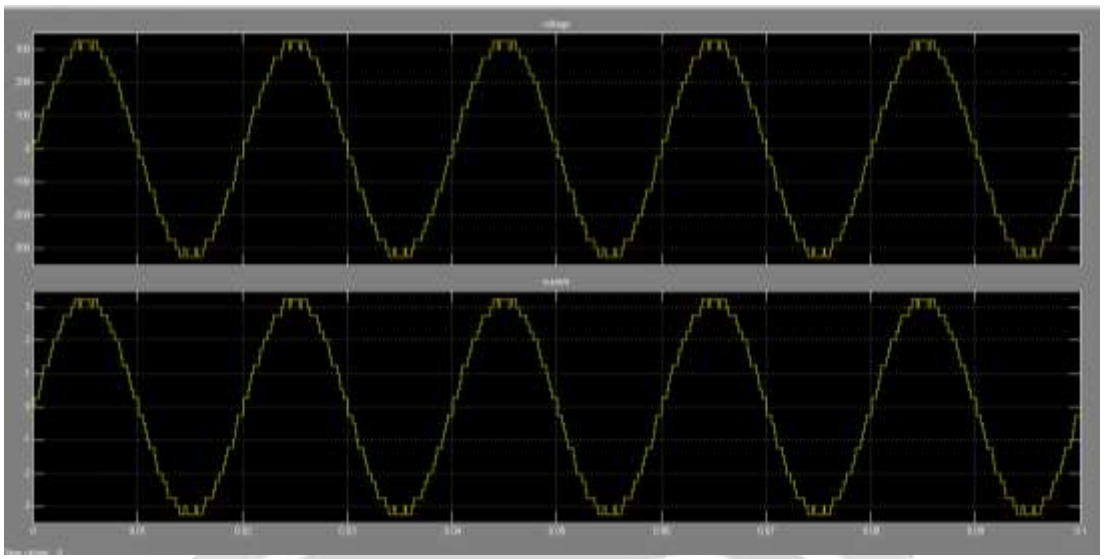

Fig.11: Output voltage of 27-level inverter

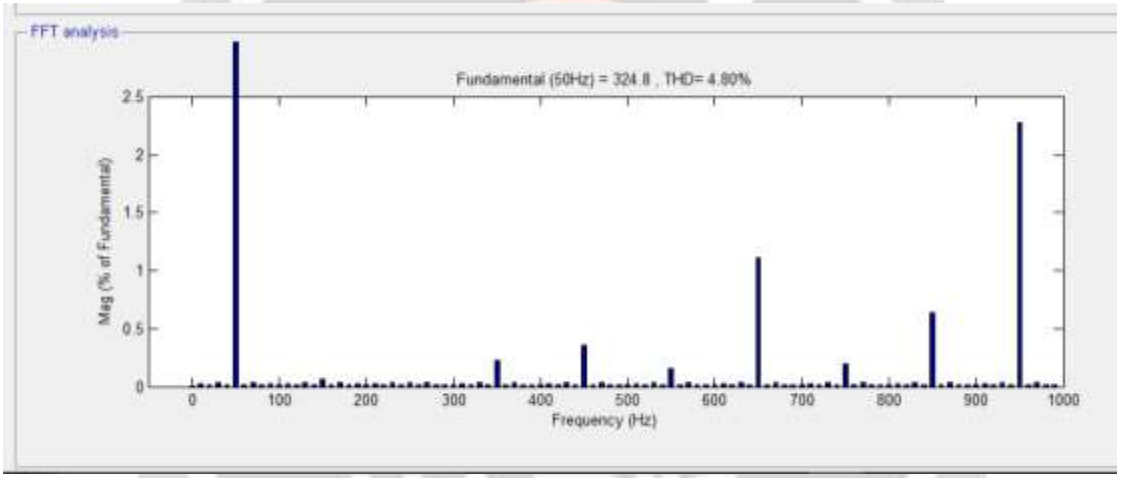

Fig.12 FFT analysis

5. CONCLUSIONS

The simulation results show that in this paper 3-phase 9-level and 27-level asymmetrical cascaded H-bridge inverter are studied. The output voltage of three phase Asymmetrical 9-level CHB gives 16.051 % THD, whereas 27-level asymmetrical CHB gives 4.8% THD. Hence compared to 9-level CHB, a 27-level MLI unequal dc voltage ratio consists of minute number of harmonics and increased output voltage quality.

6. REFERENCES

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