ANALYZING PERFORMANCE METRICS OF LOW POWER 15T SRAM CELL USING FINFET AND GNRFET

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Abstract

Today FinFET(finfield effect transistor), CNTFET(carbon nanotube field effect transistor),GNRFET(graphene nano ribbon field effect transistor) are emerging devices and used as an alternative for planar MOSFETs for reducing leakage power and dealing with submicron issues in the field of electronics and information processing. Memory storage also became important aspect for various applications .SRAM (static random access memory)cell is used for memory storage and it is volatile memory.15T SRAM cell using CMOS is used for various applications but it has some problems like leakage current, short channel effects ,delay etc. To deal with these issues we use low power 15T SRAM cell using FinFET, CNTFET,GNRFET technologies. In this work we analyze the performance metrics like power , delay, area of 15T SRAM cell using FinFET, CNTFET, GNRFET technologies.

Keywords— SRAM cell , FinFET, GNRFET, Power, Delay

I. INTRODUCTION

A low power Static Random Access Memory (SRAM) design is a main concern of implantable devices and wireless applications in which the input power or battery life is of a key concern whose operational frequency ranges between few hundreds of Kilohertz to tens of Megahertz. This is because of the major contribution of the SRAMs on the System on Chips (SoC) as they occupy about 70% of the die area, which could be further increased in the future. The proliferation of the transistors count in SRAMs and the corresponding leaking current of these transistors in the scaled down technologies has made these devices more power hungry.

Static Random Access Memories mostly contribute to the performance, area and power dissipation of the digital integrated systems. The mentioned implantable and wireless applications require low power circuits operating for a long time, occupying less area without degrading the performance, as it provides inconvenience and may even be risky specially while considering the implantable devices. One of the straightest forward and a worthwhile method of achieving power efficiency is of reducing the supply voltage since the leakage power and the active power has an exponential and quadratic relation respectively with the supply voltage. However, lowering the supply voltage would diminish the robustness of the circuit and can also cause the system to

perform malfunction. Therefore, reducing the supply voltage and at the same time maintaining the robustness of the circuit is most important for the power constrained systems, as data stability is one of the main concern of the SRAM cells.

The memory array consists of number of cells in which the data is to be stored or read. Each of the cell is capable of holding one bit of information. A row decoder and a column decoder are used to select a particular cell from the array. The precharge circuit activates the precharging of Bit Lines. A Sense amplifier particularly performs the read functionality. It detects the content of a cell in the form of a small voltage variation obtained between the cell's Bit Lines and produces the corresponding data that is stored in that particular cell.

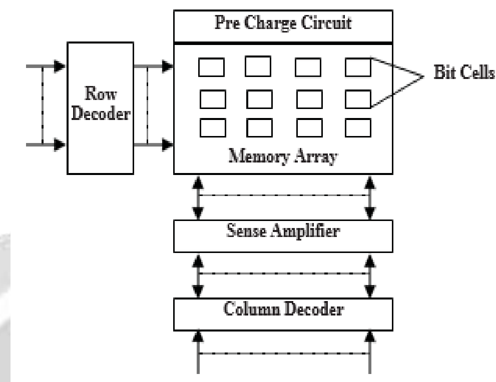

Fig1: Architecture of SRAM

II. RELATED WORKS

Ref No:[1]
The simulatioin results of SPEC 2000 benchmark suite demonstrate that cNV SRAM realizes 86 percent energy savings on average with negligible performance impact and small hardware overhead as compared to conventional SRAM.

Ref No:[2]

The proposed implementation circuit of 65-nm CMOS technology. Simulation results, including Monte Carlo analysis and signal-to-noise ratio comparison, illustrate the resiliency of the 8T cell to leakage power attacks.

Ref no[11]
At the process technology level, well-engineering techniques by retrograde and halo doping are used to reduce leakage and improve short-channel characteristics. At the circuit level, transistor stacking, multiple vth and dynamic vth techniques can effectively reduce the leakage current in high-performance logic and memory design.
Ref No:[12]
The design of the new a ternary logic family based on CNTFETs. As the threshold voltage of the CNTFET is function of the geometry of the CNTFET (i.e., the chirality), a novel multi diameter (multi threshold voltage) CNTFET-based ternary design has been pursued in this paper. A complete set of ternary gates has been implemented using multi diameter CNTFETs. A few ternary arithmetic circuits such as the HA and multiplier have been also designed to show the effectiveness of the proposed ternary family for circuit design. Compared with previous CNTFET-based designs, the proposed ternary gates achieve high performance, low power, and small area due to the removal of resistors and the utilization of binary gates in the design of arithmetic circuits.

III. METHODOLOGY

The existing problems in SRAM cell using MOSFET are
1. Submicron issues
2. Increase in leakage power and short channel effects
3. Read and write failures with low voltage which effects speed and operation of SRAM
4. Increase in delay

To overcome these existing problems we use FINFET, CNTFET, GNRFET technologies, these deals with submicron issues and decrease the leakage power and short channel effects and at low voltages the stability of

read and write operations are maintained and also decrease the delay and increase the performance of 15T SRAM cell.

IV. RESULTS AND ANALYSIS

15T SRAM Cell using FinFET:

Fig2: Power Analysis:

Power can be calculated using the command ".power"

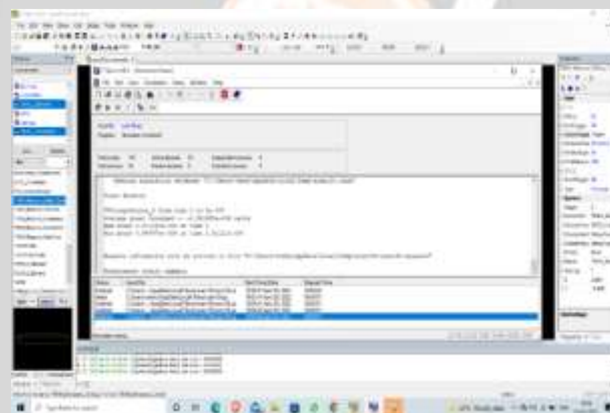

Fig3: Delay Analysis:

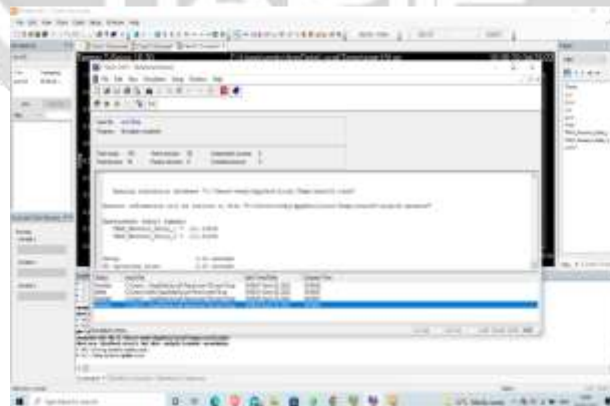

Fig4: 15T SRAM Cell using GNRFET:

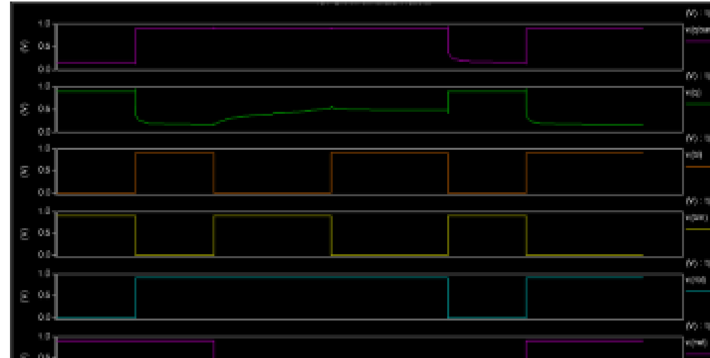

Fig5: Waveforms of 15T SRAM GNRFET

Fig6: Power and Delay Analysis:

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******
 'gnrfet_1'
 ******  transient analysis          tnom=  25.000 temp=  25.000
******
  t1=  1.8516E-12  targ=  2.0021E-09   trig=  2.0002E-09
  t2=  1.9275E-10  targ=  2.1935E-09   trig=  2.0008E-09
  tp=  9.7299E-11
  tpsum=  1.9275E-10
  avgpower=  5.9793E-06  from=  0.0000E+00    to=  1.5000E-08
  tpdp=  5.8177E-16
  tpdp2=  1.1525E-15
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Fig7: Comparsion table:

S.No.	Transistor Technology	Average Power	Delay
1.	FinFET	8.966874e-006 watts	104.5513n
2.	GNRFET	5.8177e-06 watts	9.7299e-11

V. CONCLUSION

The main objective of the project is to design the 15T SRAM Cell by replacing the planar MOSFET's by FinFET and GNRFET technologies to reduce leakage current and power dissipation.We have designed a 15T SRAM Cell using FinFET under 22nm processing technology using tanner tool and using GNRFET under 16nm processing technology using h-spice tool and observed the output waveforms and calculated the average power and delay in both cases.

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