AN ISOLATED FULL-BRIDGE IBB CONVERTER WITH VOLTAGE MULTIPLIER FOR DC MICRO GRID APPLICATIONS

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ABSTRACT

An isolated full bridge buck-boost converter with single-stage power conversion is proposed in this paper based on high-frequency bridgeless interleaved boost rectifiers are presented. The semiconductors, conduction losses, and switching losses are reduced significantly by integrating the interleaved boost converters into the full-bridge diode-rectifier. Various high-frequency bridgeless boost rectifiers are harvested based on different types of interleaved boost converters, including the conventional boost converter and high step-up boost converters with voltage multiplier and coupled inductor. The full-bridge IBB converter with voltage multiplier is analyzed in detail. The voltage multiplier helps to enhance the voltage gain and reduce the voltage stresses of the semiconductors in the rectification circuit. Hence, a transformer with reduced turns ratio and parasitic parameters, and low-voltage rated MOSFETs and diodes with better switching and conduction performances can be applied to improve the efficiency. Moreover, optimized phase-shift modulation strategy is applied to the full-bridge IBB converter to achieve isolated buck and boost conversion. MATLAB software has used to analyze the effectiveness of the proposed IBB converters and its control strategies.

Keyword: - *DC-DC Converter, Full bridge converter, Mosfet, IBB*

1. INTRODUCTION

Recently use of Isolated dc–dc converters are widely required in various applications to meet the requirements of input/output voltage range and galvanic isolation. Isolated converters can be classified into three categories: buck converters [1]–[3], boost converters [4]–[6], and buck-boost converters [7]–[9]. Voltage step-down can be implemented with an isolated buck converter, and the efficiency decreases with the decreasing of the voltage conversion ratio. Contrarily, voltage step-up is achieved with an isolated boost converter, and the efficiency decreases with the increasing of the voltage conversion ratio. Therefore, the isolated buck or boost converters are not flexible in terms of conversion efficiency and voltage range [8], [9]. Take the maximum power point tracking converters for renewable power generation systems as an example. Since the open-circuit voltage of renewable sources, such as photovoltaic [10], fuel-cell [11], and thermoelectric generator [12], is much higher than the maximum power point voltage, the highest conversion efficiency is usually achieved at the open-circuit voltage if an isolated boost converter is employed. In this case, high efficiency at the maximum power point, which is very important for the renewable power system, cannot be ensured. For the applications of battery charging and discharging [1], [13], high conversion efficiency over the entire operating range is needed. Therefore, achieving high-efficiency power conversion in a wide-voltage range is an important research topic, especially for the power systems that are sourced by batteries and renewable energy sources.

From the view of conversion efficiency, an isolated buck boost (IBB) converter would be a promising approach. Unfortunately, in the past decades, a lot of work has been done for the isolated buck and boost converters, but the research on the IBB converters is still insufficient. The flyback converter is a typical IBB converter [14], but the efficiency is still lower because of the high voltage/current stresses on components and hard switching of the active switch and rectifying diode. In fact, an IBB converter is an isolation version of a corresponding non isolated buck-

boost converter. Therefore, an IBB converter can be derived easily by inserting a transformer into a non isolated buck boost converter, for example the Cuk, SEPIC, and ZETA converters.

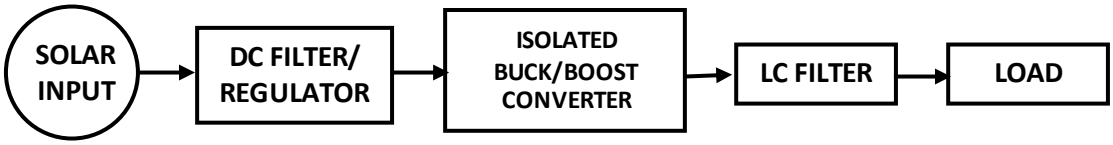


Fig-1: Block diagram of proposed system

However, similar to the flyback converter, the isolated Cuk [15], ZETA[16], and SEPIC [17] converters still suffer from the disadvantages of high component stress, hard-switching, and low efficiency. Moreover, these single-switch IBB converters can be used only in small-power applications. For non-isolated buck-boost conversion, the two-switch buck-boost converter shown in Fig. 1(a), which is composed by a buck cell, a boost cell, and an inductor, is an attractive and popular solution due to its flexible control and high efficiency[18]–[20]. Based on this topology, a family of IBB converters is derived in [8] by replacing the non-isolated buck cell in the non-isolated two-switch buck-boost converter with an isolated buck cell; the structure of the IBB converters presented in [8] is illustrated in Fig. 1(b). be achieved, it should be noted that the conversion efficiency.

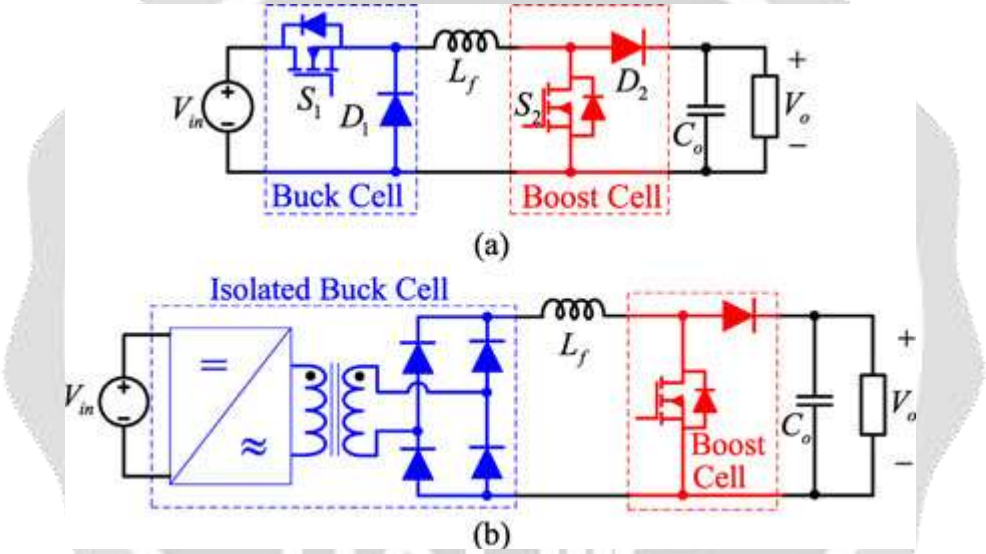


Fig-2: (a) Non-isolated two-switch buck-boost converter. (b) IBB converters presented in [11].

Although wide-voltage gain range with flexible control can will be hurt by the cascaded two-stage conversion architecture of Fig. 1.1 (b) due to the additional conduction and switching losses. Moreover, the active switches and rectifying diodes on the secondary side of Fig. 1(b) are hard-switching, which has negative influence on the conversion efficiency as well. From the view of conversion efficiency, how to implement IBB converters with single-stage and soft-switching power conversion characteristics is an interesting and valuable research topic.

From Fig. 1(b), it can be seen that the secondary-side circuit of the cascaded IBB converter is very similar to a conventional boost power factor corrector [21], which is composed of a rectifying bridge and a non-isolated boost converter. In the research area of power factor correctors, it has been demonstrated that the rectifying bridge and the boost power factor correction circuit can be integrated to build a bridgeless power factor correction circuit topology, which features higher efficiency, less power loss, and component count [22], [23]. The research results of the bridgeless power factor correction circuit drop a hint that we may build an IBB converter featuring single-stage power conversion if the rectifying bridge and the non-isolated boost converter are merged in a cascaded IBB converter. The major contribution of this paper is to propose novel IBB converters with single-stage power conversion based on integration of non-isolated-interleaved boost converters and isolated buck converters. Novel IBB converters are harvested. Moreover, optimized phase-shift modulation strategy is presented and applied to the proposed converter to achieve soft-switching operation of all of the switching devices within the entire operating range.

2. PROPOSED TECHNIQUE

The FB-IBB converter taken as an example to be analyzed is redrawn in Fig. 6. *vDS*1, *vDS*4 , and *vDS*6 are the drain to source voltages of *S*1 , *S*4 , and *S*6 , respectively. *vNP* and *vS*56 are the voltages of the primary side and secondary side of the transformer. And *iLf* is the current flowing through the inductor *Lf* . A proper dead-time is necessary for the primary-side switches to achieve ZVS and avoid shot-through of the switching bridges, but dead-time is not needed for the secondary-side switches *S*5 and *S*6 . To simplify the analysis, the parasitic capacitance of the MOSFET is ignored.

The normalized voltage gain *G* is defined as

$$G = \frac{NV_o}{2V_{\text{in}}} \qquad (1)$$

where *V*in , *Vo* , and *N* are the input voltage, output voltage, and transformer turns ratio *nP /nS* , respectively. The secondary-side phase-shift angle ϕ is defined as the phase difference between *S*6 gate signal and *S*4 gate signal. Because this phase shift serves the same function as duty cycle in the PWM converter, we define duty cycle *Ds* as

$$D_s = \frac{\varphi}{\pi}. \qquad (2)$$

And the primary-side phase-shift angle α is defined to be the phase difference between the gate signals of *S*1 and *S*3. So, the duty cycle D_p is defined as

$$D_p = \frac{\alpha}{\pi}. \qquad (3)$$

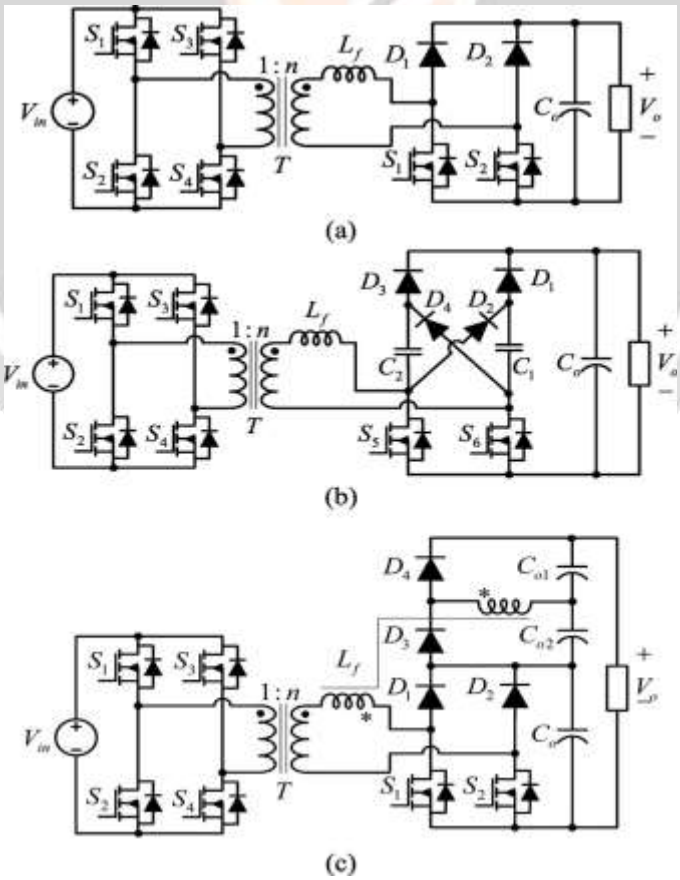


Fig-3: Novel full-bridge IBB converters with (a) bridgeless boost rectifier, (b) bridgeless boost rectifier with voltage multiplier, and (c) bridgeless boost rectifier with a coupled inductor

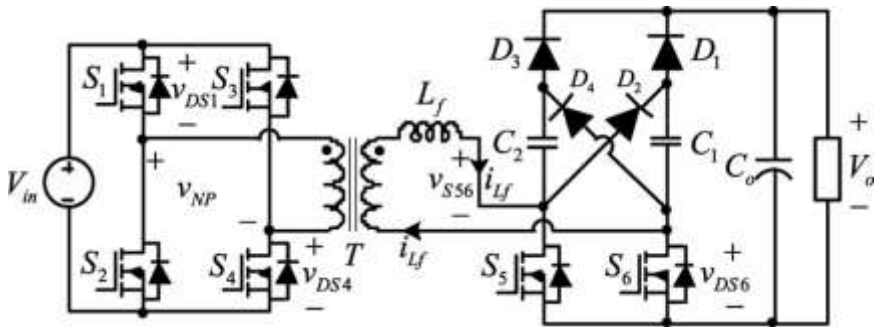


Fig-4: Proposed FB-IBB converter.

The converter can work either in the buck mode ($G < 1$) or the boost mode ($G \geq 1$). According to the waveform of the secondary-side current *iLf* , each operation mode can be further divided into continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

2.1 BOOST-CCM OPERATION

In the boost mode, the primary-side MOSFETs *S*1 and *S*4, and *S*2 and *S*3 conduct simultaneously which means D_p = 1. The secondary-side phase-shift angle is employed to regulate the output power. If the primary-side switches commute before the secondary-side current decreases to zero, the converter operates in the boost-CCM mode. The key waveform of this mode is shown in Fig. 5.3, where *D*0 is defined as the equivalent duty cycle during which the inductor current returns to zero after the primary side switches turn OFF, and *TS* is the switching period.

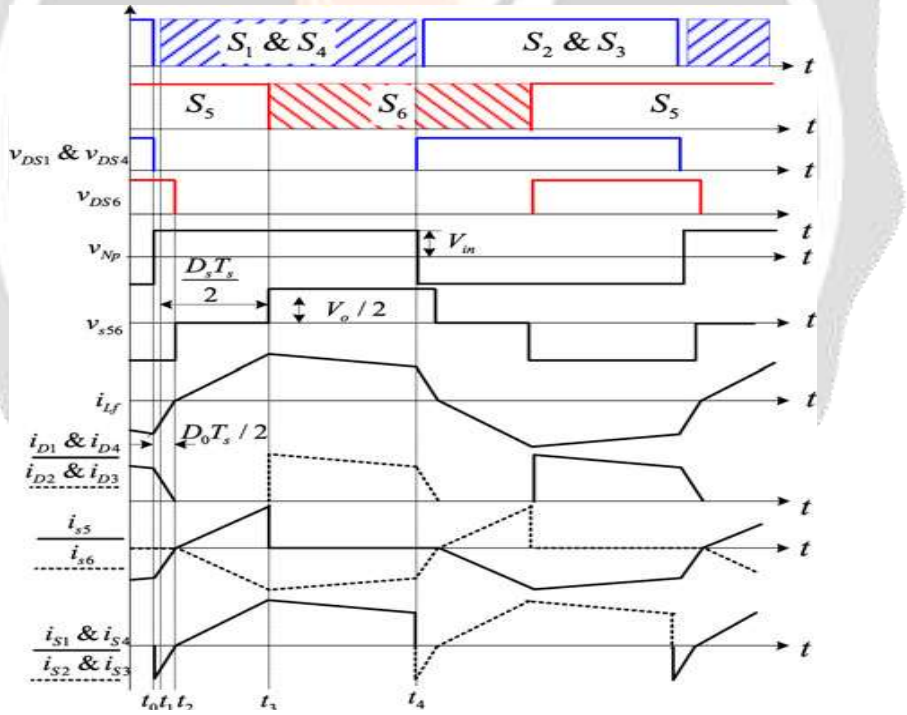


Fig-5: Key waveform of the proposed converter in the boost- CCM mode.

There are eight stages in one switching period. Due to the symmetry of the circuit, only four stages are analyzed here and corresponding equivalent circuits for each operation stage are shown in Fig. 5.4.

Stage 1—[t0, t1] [see Fig. 5.4(a)]: Before *t*0 , *S*2 , *S*3 , *S*5 , *D*1 and *D*4 are ON. On the secondary side, *S*5 , *D*1 and *C*1 make up for one current loop, while *D*4 and *C*2 make up for another one. At *t*0 , *S*2 and *S*3 turn OFF. Body diodes of *S*1 and *S*4 begin to conduct due to the energy stored in *Lf*, which results in ZVS of *S*1 and *S*4. Due to the negative voltage across *Lf*, the current *iLf* decreases rapidly

$$i_{Lf}(t) = i_{Lf}(t_0) + \frac{V_o/2}{L_f}(1/G + 1)(t - t_0). \qquad (4)$$

Stage 2—[t1, t2] [see Fig. 5.4(b)]: At *t*1 , *S*1 and *S*4 are turned ON with ZVS. This stage ends when *iLf* returns to zero, and *D*1 and *D*4 are OFF naturally without reverse recovery.

Stage 3—[t2, t3] [see Fig. 5.4(c)]: At *t*2, *iLf* returns to zero. The body diode of *S*6 begins to conduct and *Lf* is charged by the input voltage

$$i_{Lf}(t) = i_{Lf}(t_2) + \frac{V_o/2}{GL_f}(t - t_2). \qquad (5)$$

Stage 4—[t3, t4] [see Fig. 5.4(d)]: At *t*3, *S*5 turns OFF, and *S*6 turns ON with ZVS. *D*2 and *D*3 are ON and the power is transferred to the load during this stage

$$i_{Lf}(t) = i_{Lf}(t_3) + \frac{V_o/2}{L_f}(1/G - 1)(t - t_3). \qquad (6)$$

At the end of this stage, *iLf* has the same absolute value but in the reverse direction as that in the beginning of Stage 1, which is expressed as

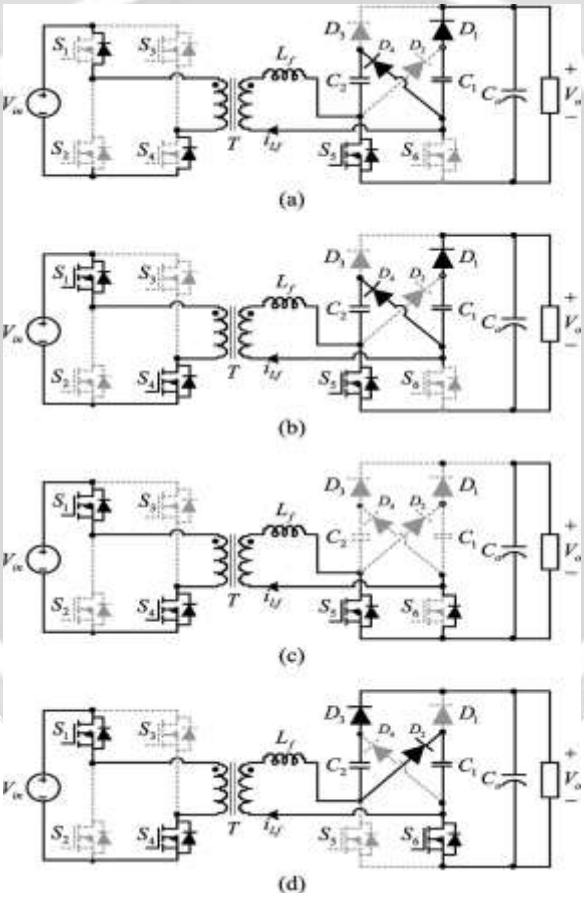


Fig-6: Equivalent circuits for each operation stage in the boost-CCM mode: (a) Stage 1 [*t*0 , *t*1], (b) Stage 2 [*t*1 , *t*2], (c) Stage 3 [*t*2 , *t*3], and (d) Stage 4

2.2 BOOST-DCM OPERATION

In the boost mode, if the secondary-side current has decreased to zero before the primary-side switches commutate, the converter enters the boost-DCM operation. The key waveform of the converter operating in the boost-DCM mode is shown in Fig. 5.5. There are also eight stages in one switching period. Due to the symmetry of the circuit, only four stages are analyzed here and corresponding equivalent circuits for each operation stage are shown in Fig. 8

Stage 1—[t0, t1] [see Fig. 5.6(a)]: Before *t*0 , *S*2 , *S*3 , and *S*5 are ON. Since *iLf* = 0, there is no energy transferred between the input and output. At *t*0 , *S*2 and *S*3 turn OFF with zero voltage and zero current.

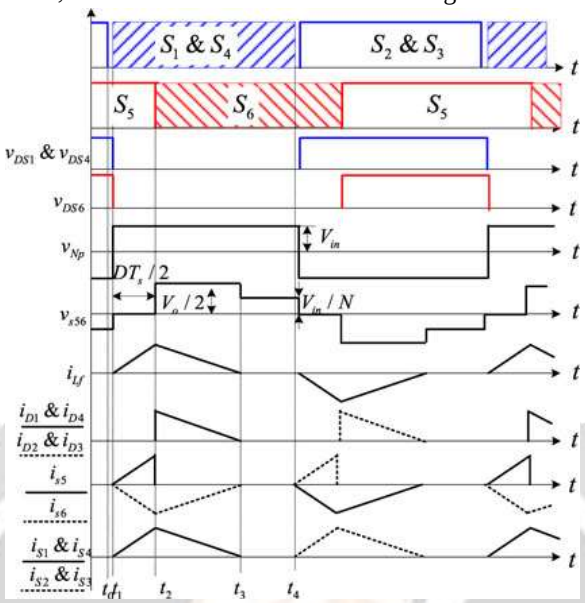


Fig-7: Key waveform of the proposed converter in the boost-DCM mode.

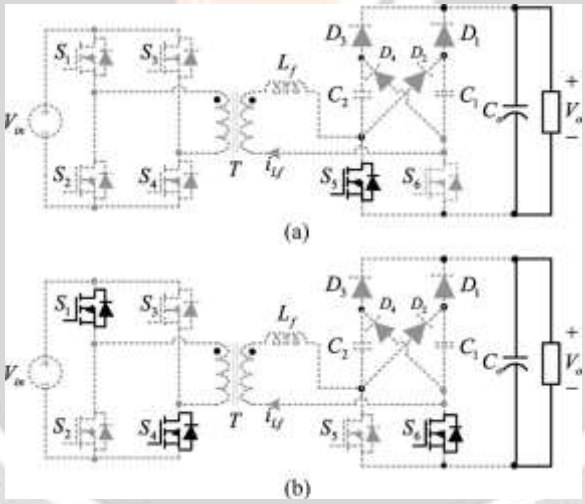


Fig-8: Equivalent circuits for each operation stage in the boost-DCM mode: (a)Stage 1 [*t*0 , *t*1] and (b) Stage 4 [*t*3 , *t*4].

Stage 2 [t1, t2] and Stage 3 [t2, t3]: At *t*1 , *S*1 and *S*4 are turned ON with ZCS. The operation principles of Stages 2 and 3 of the boost-DCM mode are the same as that of the Stages 3 and 4, respectively, in the boost-CCM mode.

Stage 4—[t3, t4] [see Fig. 10(b)]: At *t*4 , *iLf* reaches zero. *iLf* will stay in the zero state in this stage and there is no energy transferred between the input and output. A similar operation works in the rest stages in a switching period.

2.3 BUCK-CCM OPERATION

In the buck mode, a dual-phase-shift control scheme is employed. In the buck-CCM mode, the primary phase-shift angle α is fixed and the phase-shift angle between the primary- and secondary-side MOSFETs ϕ is employed to regulate the output power and voltage. The key waveform is shown in Fig. 5.7. There are twelve stages in one switching period. Due to the symmetry of the circuit, only six stages are analyzed here and corresponding equivalent circuits for each operation stage are shown in Fig. 5.8.

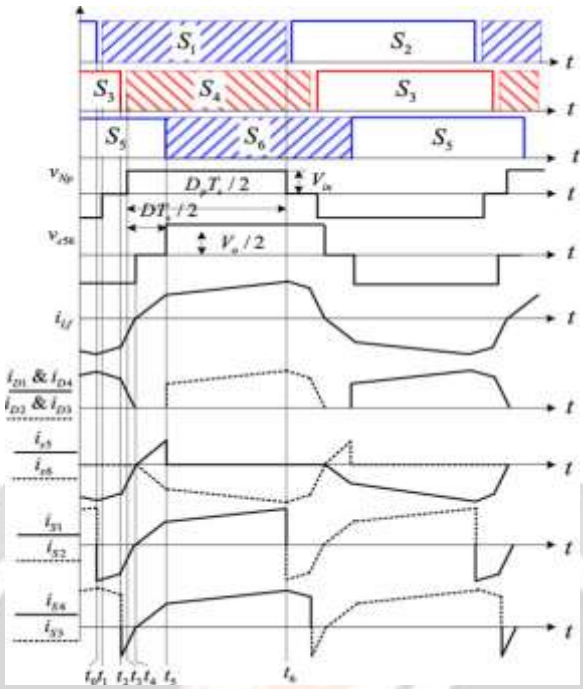


Fig-9: Key waveform of the proposed converter in the buck-CCM mode

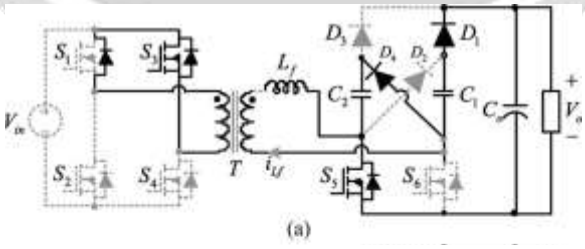
Stage 1—[t0, t1] [see Fig. 5.8(a)]: Before *t*0 , *S*2 , *S*3 , *S*5 , *D*1 and *D*4 are ON. At *t*0 , *S*2 turns OFF. The body diode of *S*1 begins to conduct due to the energy stored in *Lf* , which results in ZVS of *S*1 . The energy stored in *Lf* is delivered to the output.

$$i_{Lf}(t) = i_{Lf}(t_0) + \frac{V_o/2}{L_f}(t - t_0). \qquad (8)$$

Stage 2—[t1, t2] [see Fig. 5.8(b)]: At *t*1 , *S*1 is turned ON with ZVS. This stage ends when *S*3 turns OFF. *Stage 3—[t2, t3] [see Fig. 12(c)]:* At *t*2 , *S*3 turns OFF. The body diode of *S*4 begins to conduct. Due to the negative voltage across the inductor, the current *iLf* decreases rapidly.

$$i_{Lf}(t) = i_{Lf}(t_2) + \frac{V_o/2}{L_f}(1/G + 1)(t - t_2). \qquad (9)$$

Stage 4 [t3, t4], Stage 5 [t4, t5], and Stage 6 [t5, t6]: At *t*3 , *S*5 turns OFF, *S*6 is turned ON with ZVS. The operating principle of this state is the same as that of Stage 2 in the boost-CCM mode, whereas the operating principles of Stages 5 and 6 of the buck-CCM mode are the same as that of the Stages 3 and 4, respectively, in the boost-CCM mode



(a)

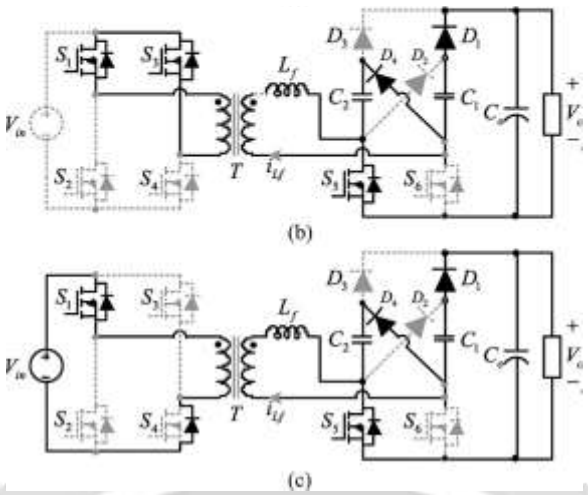


Fig-10: Equivalent circuits for each operation stage in the buck-CCM mode: Stage 1 [*t*0 , *t*1], (b) Stage 2 [*t*1 , *t*2], and (c) Stage 3 [*t*2 , *t*3].

At the end of this stage, *iLf* has the same absolute value but in the reverse direction as that in the beginning of Stage 1. A similar operation works in the rest stages of a switching period.

2.4 BUCK-DCM OPERATION

When ϕ decreases to zero, the converter enters in the buck- DCM mode, in which ϕ is fixed at zero while α begins to decrease. In order to achieve ZVS of the secondary-side MOSFETs, a dead-time between the primary-side and the secondary side MOSFETs is needed. The key waveform is shown in Fig. 5.9. There are twelve stages in one switching period. Due to the symmetry of the circuit, only six stages are analyzed here and corresponding equivalent circuits for each operation stage are shown in Fig. 5.10.

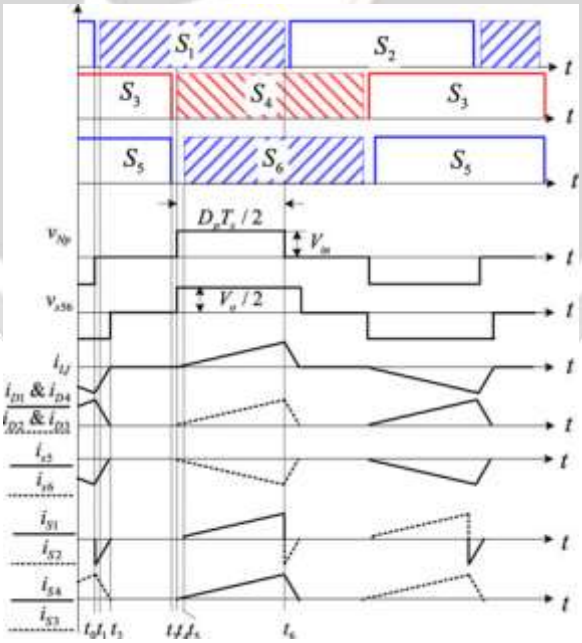


Fig-11: Key waveform of the proposed converter in the buck-DCM mode.

Stage 1 [t0, t1] and Stage 2 [t1, t2]: Before t_0 , S_2 , S_3 , S_5 , D_1 andD_4 are ON. At t_0 , $S2$ turns OFF. The operating principles of Stages 1 and 2 of the buck-DCM mode are the same as that of the Stages 1 and 2, respectively, in the buck-CCM mode.

Stage 3—[t2, t3] [see Fig. 5.10(a)]: At *t*2 , *iLf* reaches zero. *iLf* will stay in the zero state in this stage and there is no energy transferred between the input and output.

Stage 4—[t3, t4] [see Fig. 5.10(b)]: At *t*3 , *S*5 and *S*3 turn OFF.

Stage 5—[t4, t5] [see Fig. 5.10(c)]: At *t*4 , *S*4 turns ON. *Lf* is charged by the input voltage

$$i_{Lf}(t) = i_{Lf}(t_2) + \frac{V_o/2}{GL_f}(t - t_2). \qquad (10)$$

Stage 6—[t5, t6]: At *t*5 , *S*6 turns ON. The operating principle of this stage is the same as that of the Stage 4 in the boost-CCM mode. A similar operation works in the rest stages of a switching period.

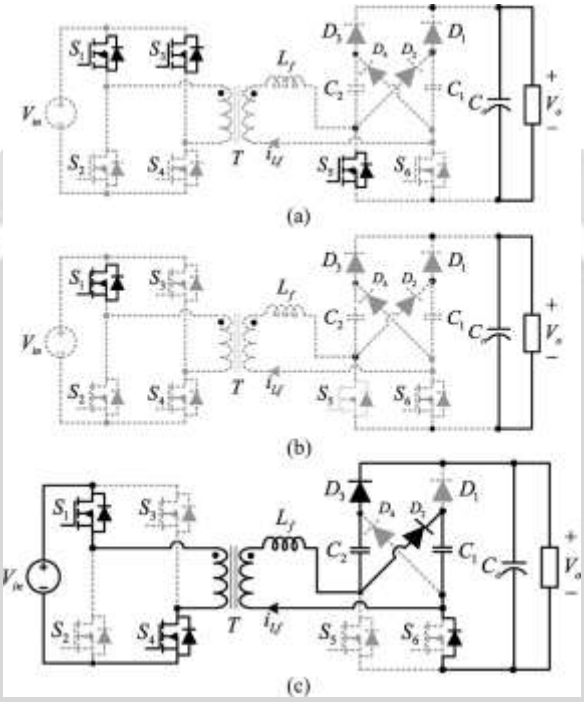


Fig-12: Equivalent circuits for each operation stage in the buck-DCM mode: (a) Stage 3 [*t*2 , *t*3], (b) Stage 4 [*t*3 , *t*4], and (c) Stage 5 [*t*4 , *t*5].

4 SIMULATION RESULTS

Simulation design has built to verify the theoretical analysis. The specifications are listed in Table I. The input voltage is 40 V–60 V and the output voltage is 380 V. Fig. 15 shows the voltage *vNp*, *vS*56, and current *iLf* waveforms of the converter under boost-CCM, boost-DCM, buck-CCM, and buck-DCM modes, respectively. As shown in Fig. 16 and 17 the primary current decreases linearly when the input power is transferred to the output side through the filter inductor, because the normalized voltage gain *G* is greater than Fig. 16. Voltage *vN P* , *vS* 56 , and current *iLf* waveform in (a) boost-CCM mode, (b) boost-DCM mode, (c) buck-CCM mode, and (d) buck-DCM mode.1 and the converter works in the boost mode. When the inductor current decreases to zero, a small voltage ringing can be seen on the secondary winding of the transformer, which is caused by the parasitic parameters. On the other hand, the primary current increases linearly during the power transferring state, as shown in Fig. 18, with the voltage gain $G < 1$. The waveform in Fig. 19 satisfies the theoretical analysis pretty well. The soft-switching waveforms of the switches under different operation modes are shown in Figs. 20–23. *vGS*1, *vGS*4, and *vGS*6 are the driving voltages of the switches *S*1, *S*4, and *S*6, while *vDS*1, *vDS*4, and *vDS*6 are corresponding drain to-source voltages.

4.1 CCM-BOOST

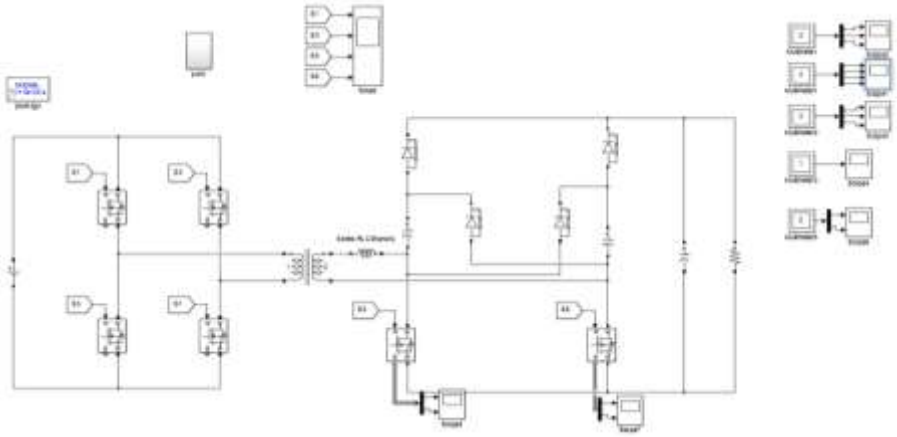


Fig-12: Simulation diagram of the proposed system

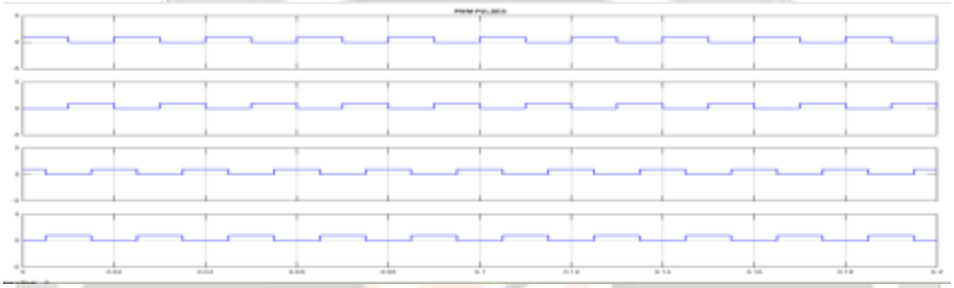


Fig-13: PWM pulses

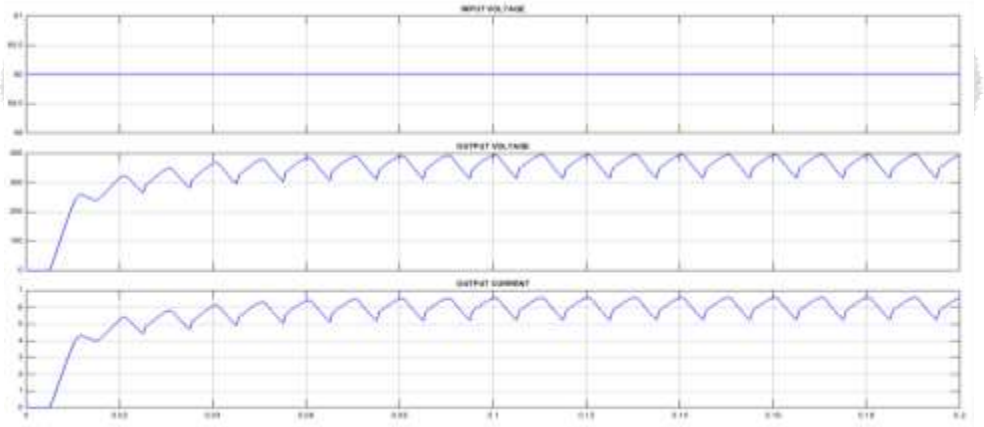


Fig-14: input and output voltages and current

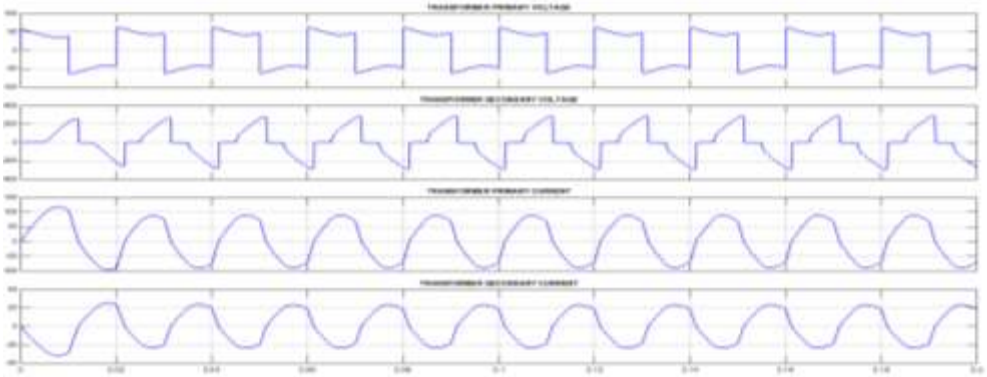


Fig-15: Transformer primary and secondary voltages and currents

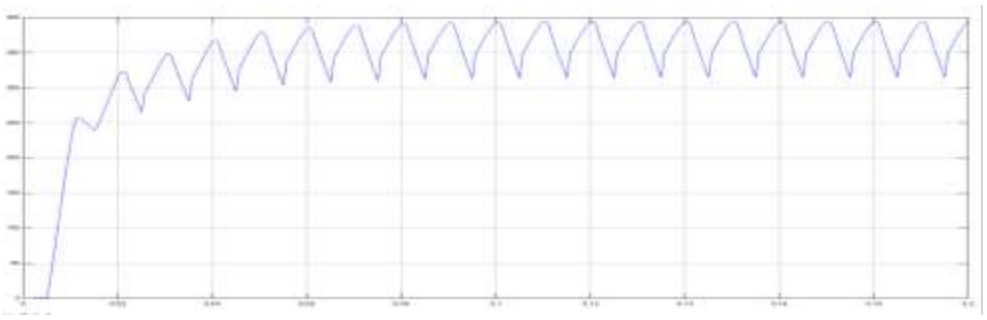


Fig-16: Output DC voltage

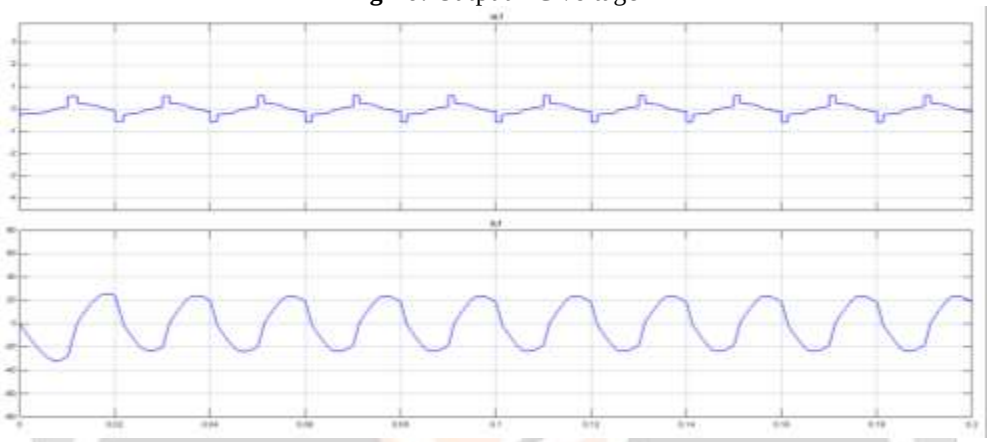


Fig-17: voltage and current of Lf

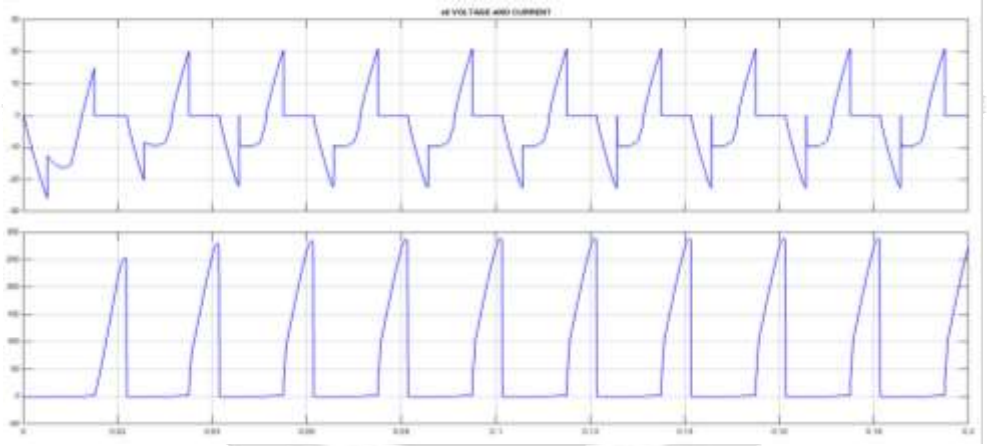


Fig-18: Voltage and current of switch S1

- **DCM MODE**

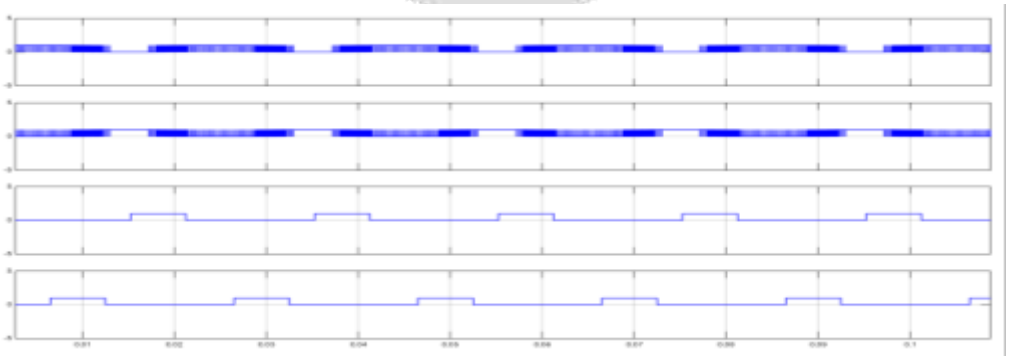


Fig-19: PWM pulses

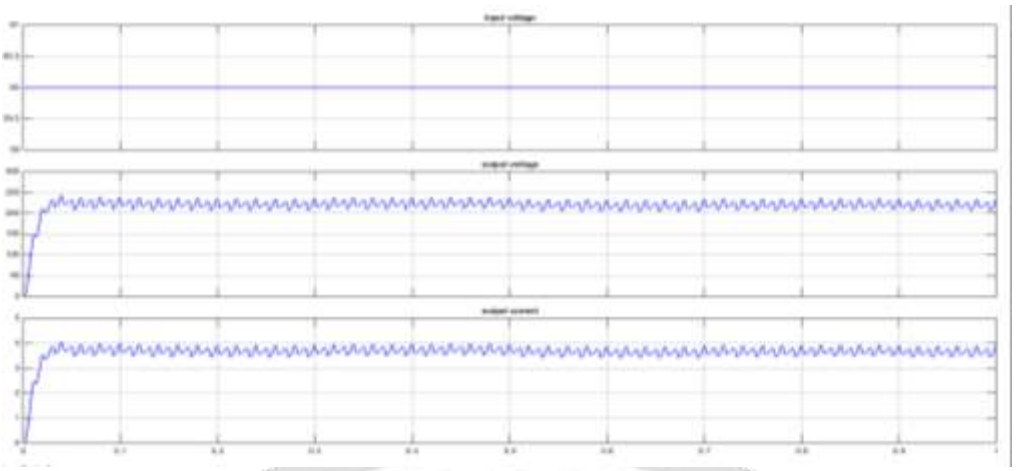


Fig-20: input and output voltages and current

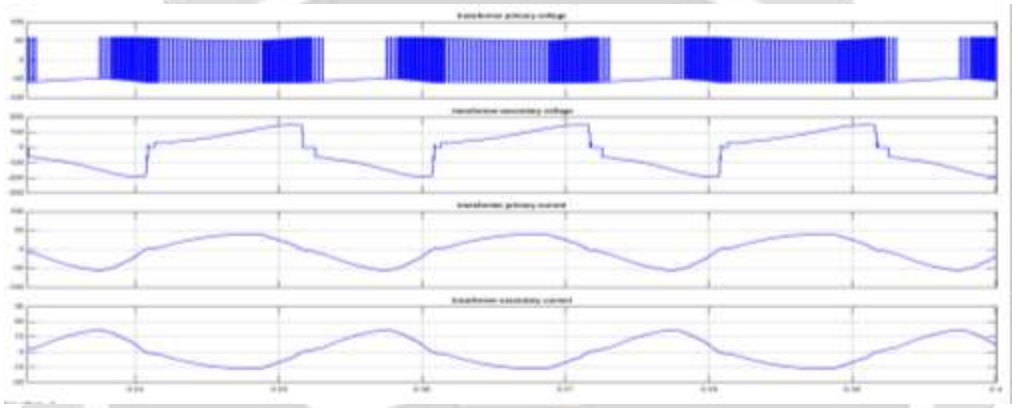


Fig-21: Transformer primary and secondary voltages and currents

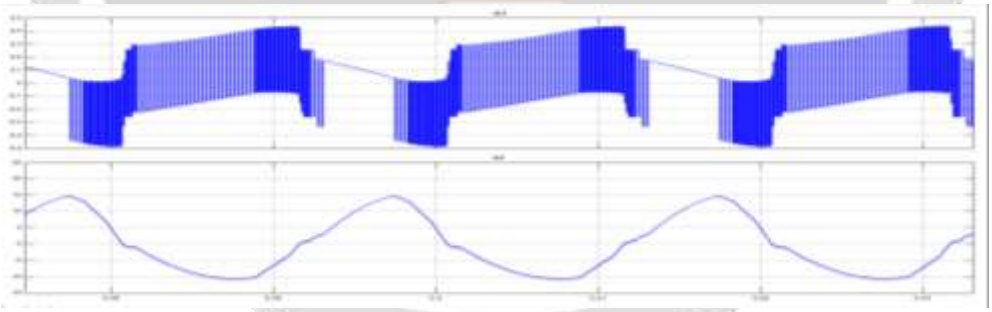


Fig-22: voltage and current of Lf

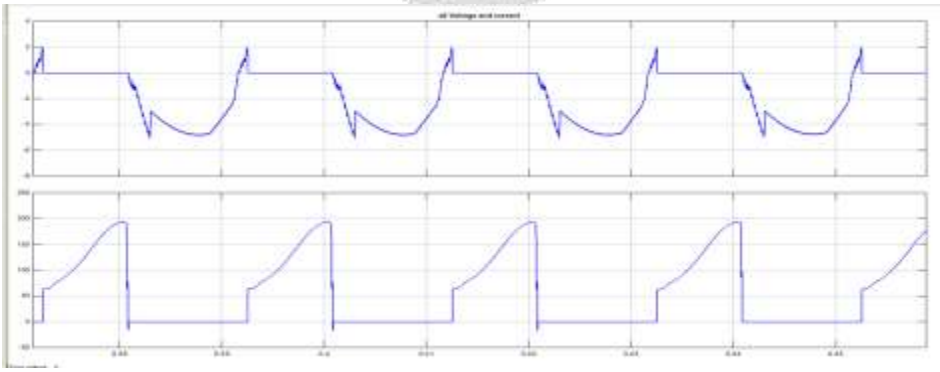


Fig-22: Voltage and current of switch S1

5. CONCLUSIONS

Novel IBB converters with single-stage power conversion based on high-frequency bridgeless-interleaved boost rectifiers have been proposed and investigated in this paper. The concept of high-frequency bridgeless-interleaved boost rectifiers, which are built by integrating a full-bridge diode-rectifier and interleaved boost converters, are rooted in the bridgeless ac–dc power factor corrector circuit. A full-bridge IBB converter with a voltage multiplier on the secondary-side bridgeless boost rectifier has been investigated. The voltage stresses of the semiconductors in the boost-rectifier are reduced significantly due to the voltage multiplier; hence, low-voltage-rated devices with better conduction and switching performance can be used to improve efficiency. In other words, this converter is more attractive for high-output-voltage applications. Optimized phase-shift control strategy is applied to the proposed converter to realize isolated buck and boost conversion. Moreover, soft-switching within the whole operating range have been achieved for all of the active switches and diodes, respectively, by adopting the optimized phase-shift control. The analysis and performance have been validated using MATLAB software on a 40–60 V-input, 380-V-output type system

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6. REFERENCES

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