AN ISOLATED SINGLE STAGE AC-DC CONVERTER WITH SOURCE PF CORRECTION FEATURE

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ABSTRACT

This paper proposes a new single-stage three-level isolated ac/dc PFC converter for high dc-link voltage low-power applications, achieved through an effective integration of ac/dc and dc/dc converter stages, where all of the switches are shared between two operations. With the proposed converter and switching scheme, input current shaping and output voltage regulation can be achieved simultaneously without introducing additional switches or switching actions. In addition, the middle two switches are turned on under zero current in discontinuous conduction mode operation, and the upper and bottom switches are turned on under zero voltage. Due to the flexible dc-link voltage structure, high power factor can be achieved at high line voltage. To analyze the proposed topology MATLAB/SIMULINK software tool has used. Initially conventional model shown will be simulated and then proposed model will be simulated to compare for power factor and peak efficiency at low input line voltage.

Keyword :- *Isolated dc–dc converter, power factor (PF) correction, single-stage converter, three-level converter, variable dc-link voltage, zero-current switching, zero-voltage switching.*

1. INTRODUCTION

The ac/dc power converters are required to operate with high power factor (PF) and low total harmonic distortion (THD) for improved grid quality and full capacity utilization of the transmission lines. Passive PF correction (PFC) circuits consist of inductive and capacitive filters followed by a diode bridge provide the simplest way of achieving high PF with high efficiency; however, they require low line frequency filters which are bulky and heavy. In order to operate at high frequency and reduce the size of the circuit, high frequency two-stage active PFC converters have been proposed [1]–[4]. In this architecture, a front-end ac/dc PFC converter is operated with a switching frequency in the order of tenths to several hundred kHz for converters with Si semiconductor devices, and from several hundreds of kHz to tenths of MHz with wide-band gap devices, to shape the input current close to sinusoidal waveform in phase with the grid voltage [4]. The second stage dc/dc converter provides the galvanic isolation and output voltage regulation. The controllers of the two stages are completely independent.

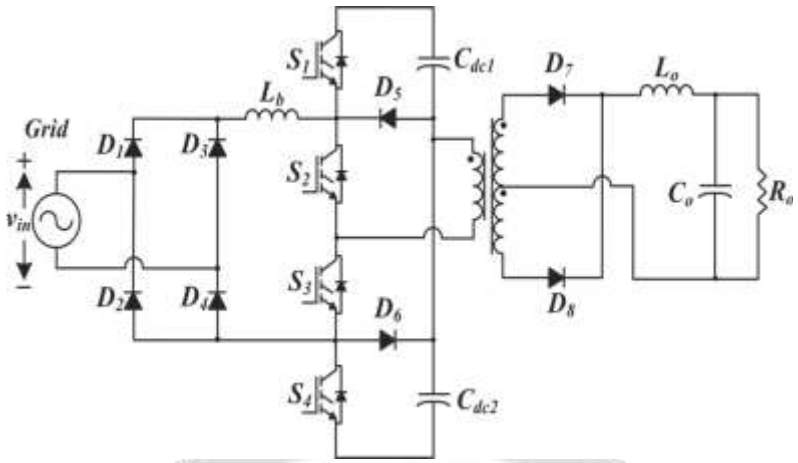

Fig-1: Conventional three-level single-stage fully integrated PFC ac–dc converter

The flexibility in control allows optimizing power stages, fast output voltage regulation and operating with high PF and low THD. However, this method comes with the expense of more components and larger size. Moreover, the constant switching losses such as parasitic capacitance losses associated with power switches reduce the efficiency of the converter at light load condition.

A cost-effective approach to reduce the number of switches is to use single-stage ac/dc converters [5]–[10]. In single-stage PFC converters, the front-end PFC stage and dc/dc stages are integrated and their operations are performed in a single-stage, basically, by sharing some of the switches and control scheme. An energy storage unit, capacitor or inductor, is located in between two stages, acting as a power buffer and providing sufficient hold up time. Numerous PFC ac/dc single-stage topologies have been proposed in literature, particularly, operating in discontinuous conduction mode (DCM) for simple yet effective PF control. Majority of the proposed single-stage converters are proposed for low-power applications, where a flyback or forward converter derived topologies are used to achieve input current shaping and output voltage regulation [11]–[13]. These converters offer cost-effective solution for low-power applications; however, they suffer from excessive voltage/current stresses on the switches, and are suitable for power levels lower than 200 W.

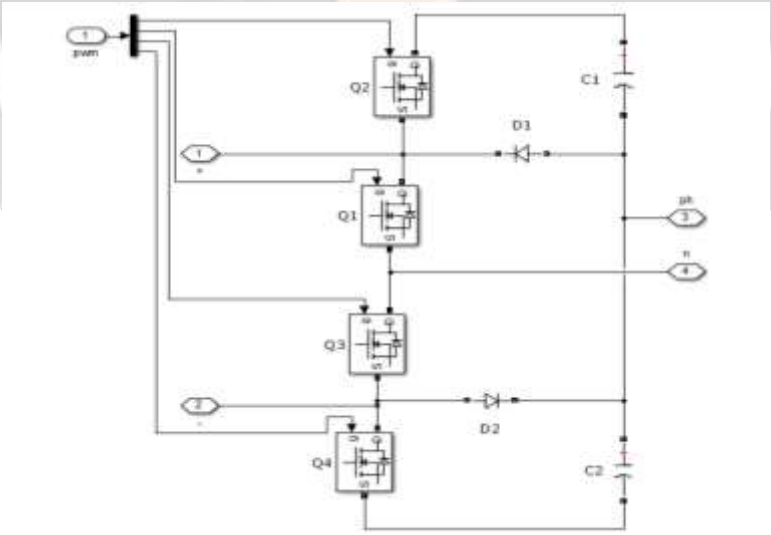

Fig-2: Conventional DC-DC converter

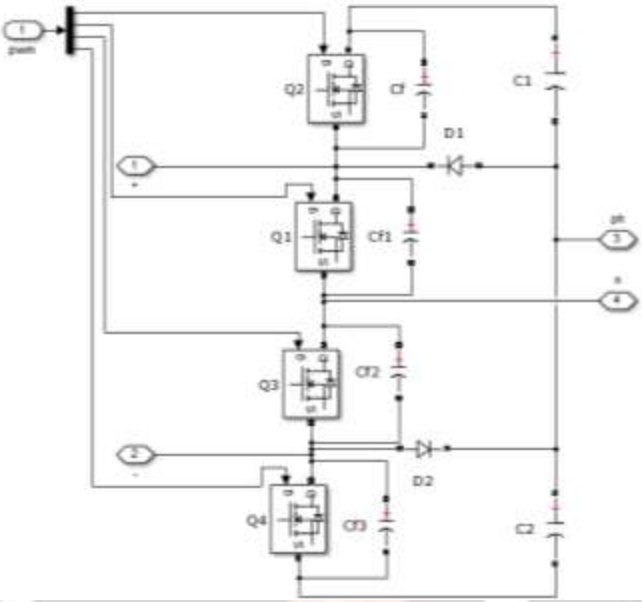

Fig-3: Proposed DC-DC converter with capacitors across each switch.

Few modifications have done to Fig.1 as Fig.3 to get more efficiency and better power factor i.e.

1) Capacitors of equal values are additionally provided to make the switch ZVS and ZCS OFF/ON.
2) Hysteresis PWM technique has used for switching.

This feature allows having lower output current ripple and less distorted input current even at light load condition. In addition, the middle two switches are turned ON under zero current in DCM operation, and the upper and bottom switches are turned on under zero voltage, which increases the efficiency of the converter in comparison to hard-switched ac/dc single-stage converter. Furthermore, higher PF can be achieved at high line voltage due to the flexible dc-link voltage structure.

2. PROPOSED THREE-LEVEL SINGLE-STAGE PFC CONVERTER

The proposed converter is essentially an integrated version of a boost PFC circuit and three-level isolated dc–dc converter. Basically, a diode bridge and an inductor are added to the three-level isolated dc–dc converter topology as shown in Fig. 1 and 2. Here, the inductor is charged when S2 and S3 are turned on simultaneously. Body diodes of S1 and S4 serve as the boost diode of the PFC boost converter. At the same time, S1 to S4 are switched to apply *V*dc/2,−*V*dc/2, and zero voltage across the primary side of the transformer. Thus, all of the switches are shared between the two-stages, which makes it fully integrated single-stage converter without any additional auxiliary switches. The switching scheme of the conventional three-level isolated dc/dc converter is given in Fig. 4.

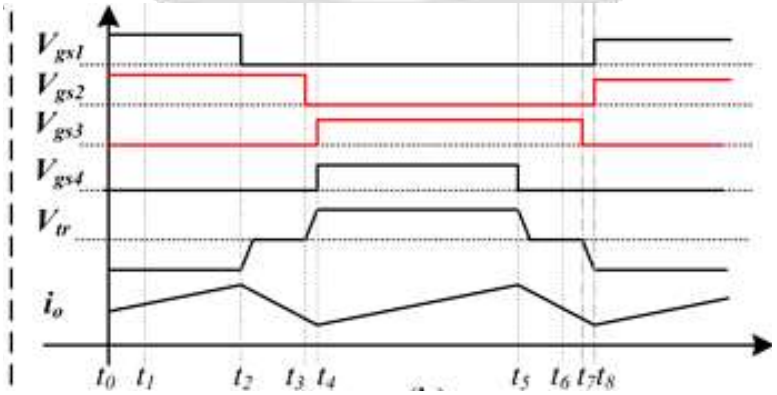

Fig-4: The switching scheme of the conventional three-level isolated dc/dc converter

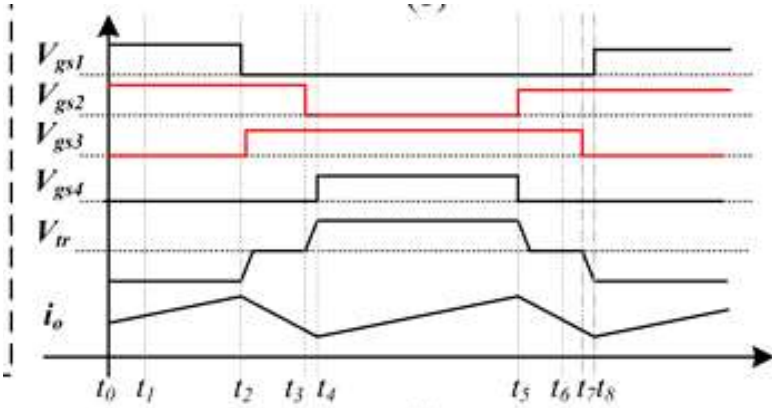

Fig-5: The switching scheme of the modified three-level isolated dc/dc converter

In this conventional scheme, the duty ratios of S2 and S3 are fixed close to 50% for simplicity in control and to ensure upper or lower three switches are not turned ON simultaneously as this would cause short-circuit through dc-link capacitors. Overlapping these two signals, as long as short-circuit condition is avoided, has no impact on the operation of the circuit. Similar to that in the conventional scheme, zero voltage is applied across the primary side of the transformer. This modified switching scheme is presented in Fig. 5. When a boost inductor and a diode bridge is added to the nodes as in Fig. 1, the overlap of gate signals of S2 and S3 enables applying input voltage across the boost inductor. The switching scheme of the converter is given in Fig. 6. The switches S2–S3, and S1–S4 have 180° phase shift with respect to each other. The duty ratios of S2–S3 should be greater than 0.5 such that two signals overlap. Here, the circuit is explained considering that input inductor current is discontinuous and the switching scheme is as follows; S1 is turned on right after S3 is turned OFF, and similarly, S4 is turned on when S2 is turned OFF. A dead-time should be inserted in between the turning ON instant of S1 and turning OFF instant of S3, and likewise between switching of S2 and S4 to avoid short-circuit.

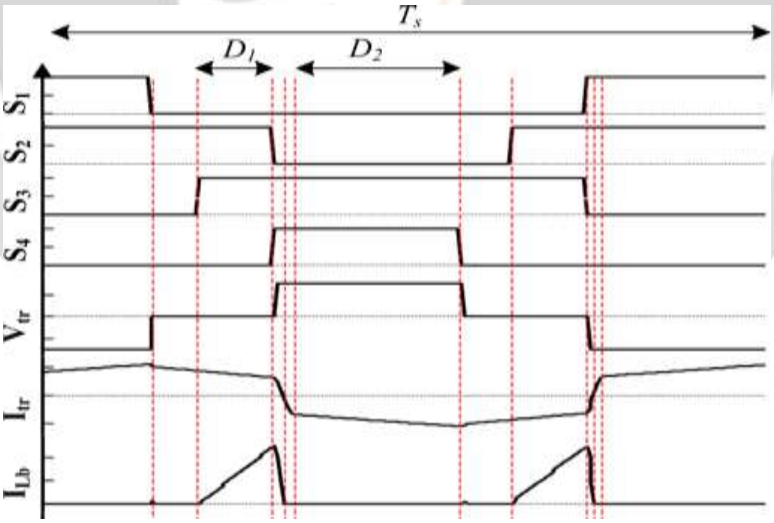

Fig-6: Switching scheme of the proposed integrated three-level ac–dc converter.

2.1 Operation Modes

The operation modes of the circuits, which are given in Fig. 7, are explained in this section.

Mode 1 [$t_0 < t < t_1$]: In this mode, both S1 and S2 are on. The upper capacitor, *C*dc1, discharges to the load by applying −*V*dc/2 to the primary side of the transformer. The primary side current increases linearly under constant voltage. *D*8 conducts at the secondary side of the transformer. The voltage across the output inductor is $V_{Lo} = V_{dc}/2N - Vo$. In this mode, the boost inductor, *Lb*, does not interfere to the operation of the circuit.

Mode 2 [t1 < t < t2]: At $t = t1$, S1 is turned OFF and S2 is kept on. The current in the leakage inductance conducts $D5$ and the primary side current freewheels; hence, zero voltage is applied across the primary side of the transformer. The output inductor voltage is equal to $-Vo$. The output inductor current decreases linearly.

Mode 3 [t2 < t < t3]: At $t = t2$, S3 is turned on, while S2 still remains on. The primary current continuous to freewheel and zero voltage is applied across the primary side; hence, the output inductor current continuous to decrease under output voltage. Meantime, Vin is applied across Lb, and input current increases linearly storing energy in the inductor.

Mode 4 [t3 < t < t5]: In the beginning of this mode, S2 is turned OFF, S4 is turned ON, while S3 is kept on. Within this time interval, the following two operations are completed. The energy stored in the input inductor is transferred to the dc-link capacitors. The inductor current decreases linearly under Vin $-V$dc. Meantime, Vdc/2 is applied across the primary side of the transformer. The current in the leakage inductance is transferred to Cdc2. This causes the output current to commute from $D8$ to $D7$. At the end of this time interval, the energy in the input inductor is completely transferred to the dc-link capacitors and the commutation of the output diodes is completed. Depending on the dc bus voltage, and input current, one of these operations ends earlier than the other one. In this case, the energy stored in Lb is transferred to the dc-link at $t = t5$. Then, the current commutation from $D8$ to $D7$ is completed at $t = t6$.

Mode 5 [t5 < t < t6]: Cdc2 discharges over to the load and Vdc/2 is applied across the primary side of the transformer. The voltage across the output inductor is $V_{Lo} = V\text{dc}/2N - Vo$. The input current remains at zero in DCM mode.

Mode 6 [$t6 < t < t7$*]:* At $t = t6$, S4 is turned OFF, and only S3 is on. This allows leakage current to freewheel through $D6$, and zero voltage is applied to the primary side. The output current decreases linearly under $-Vo$.

Mode 7 [$t7 < t < t8$ *]:* At $t = t7$, S2 is turned ON. The energy from the input is stored in the inductor. This is similar to Mode 3, except that this time the primary side current is opposite to that in Mode 3 and freewheels through $D6$.

Mode 8 [$t8 < t < t10$*]:* At the beginning of this interval, S3 is turned OFF, S1 is turned ON, and S2 remains ON. This mode is similar to Mode 4, where the stored energy in the inductor is transferred to the dc bus capacitors, and $-V\text{dc}/2$ is applied to the primary windings. In the meantime, the output inductor current commutates from $D7$ to $D8$.

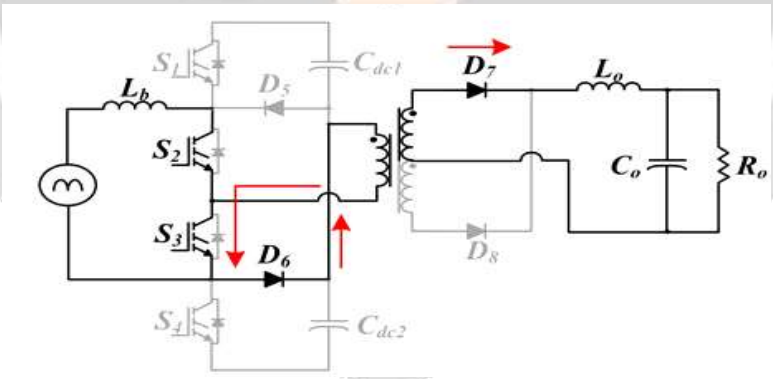

Fig-7: Operation mode of the converter Mode 8: $t8 < t < t9$.

3. SOFT SWITCHING TECHNIQUE

Soft switching can mitigate some of the mechanisms of switching loss and possibly reduce the generation of EMI Losses due to high voltage and high current present in switch during transitions, e.g. due to diode reverse recovery Losses due to shorting device capacitances Semiconductor devices are switched on or off at the zero crossing of their voltage or current waveforms:

3.1 Zero-current switching

Transistor turn-off transition occurs at zero current. Zero current switching eliminates the switching loss caused by IGBT current tailing and by stray inductances. It can also be used to commutate SCR's.

3.2 Zero-voltage switching

Transistor turn-on transition occurs at zero voltage. Diodes may also operate with zero-voltage switching. Zero-voltage switching eliminates the switching loss induced by diode stored charge and device output capacitances. Zero-voltage switching is usually preferred in converters based on MOSFETs. ZCS vs. ZVS depends on tank current zero crossings with respect to Transistor switching times equal to tank voltage zero crossings operation below resonance: input tank current leads voltage Zero-current switching (ZCS) occurs.

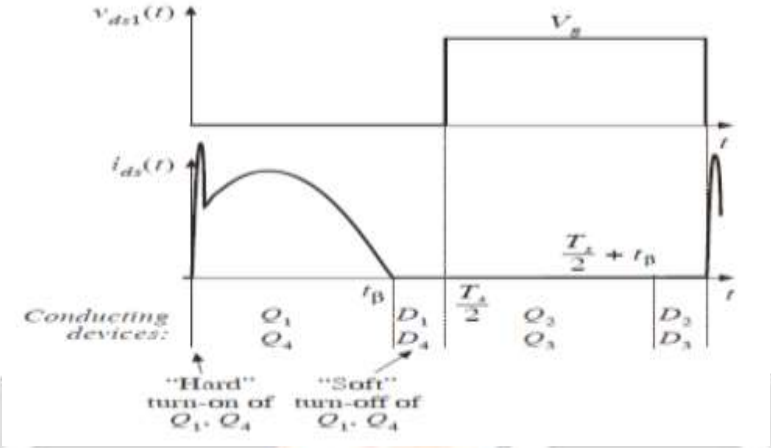

Fig-8: Turn-on/off transitions

4. HYSTERESIS CURRENT CONTROL

The PFC of boost converter with CCM condition is possible with certain control strategy (Moon et al., 2011; Roggia et al., 2012). Among the various control Methods, Hysteresis Current Control (HCC) is extensively used technique owing to its noncomplex implementation, enhanced system stability, fast response and less distortion in input current wave form (Zhou et al., 1990). In this study , HCC technique is used for wave shaping and regulating the output voltage.

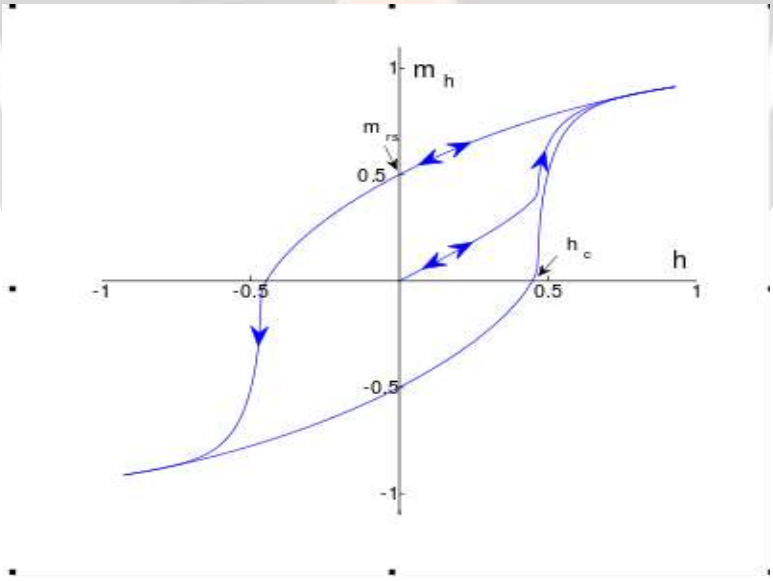

Fig-9: hysteresis loop deign

Different current control techniques are usually used for controlling the PFC converters .For implementing the closed loop control, the supply voltage and the output voltage, input current of the boost converter are sensed. In outer voltage control loop, the boost converter output voltage is scaled down and compared with the reference value. The difference is given to the PI controller. The sine template obtained from the supply voltage is multiplied with the output of PI controller and the resulting signal sets the reference current.

5. SIMULATION RESULTS AND ANALYSIS

This section deals with simulation of the proposed circuit in different conditions.

5.1 Conventional system

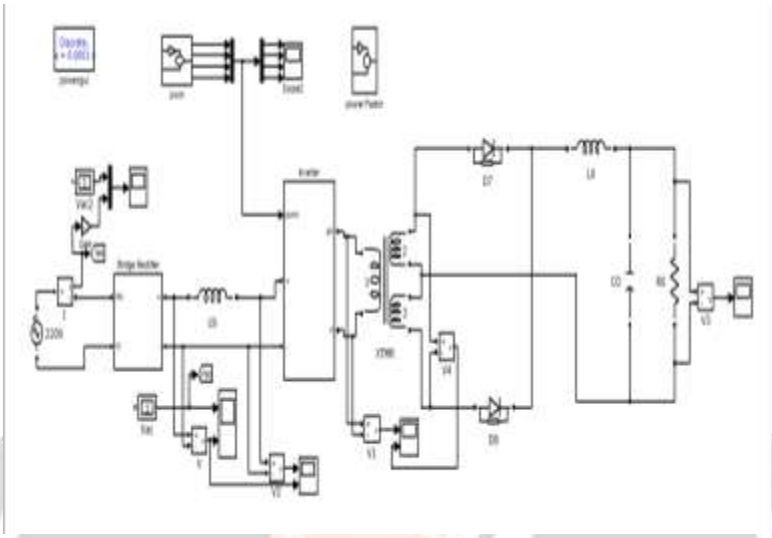

Fig-10: Matlab design of conventional system

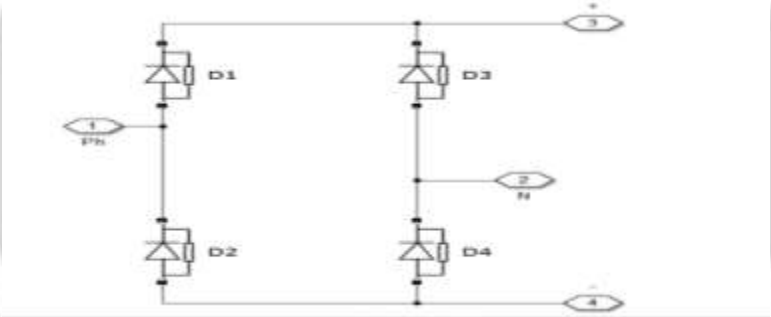

Fig-11: diode rectifier drawn using matlab design

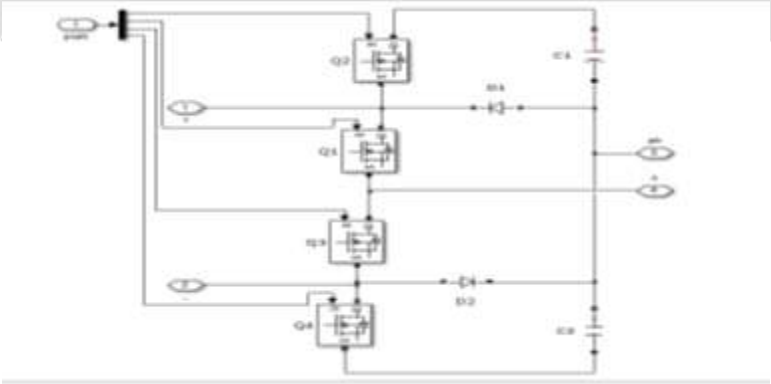

Fig-12: conventional dc-dc converter

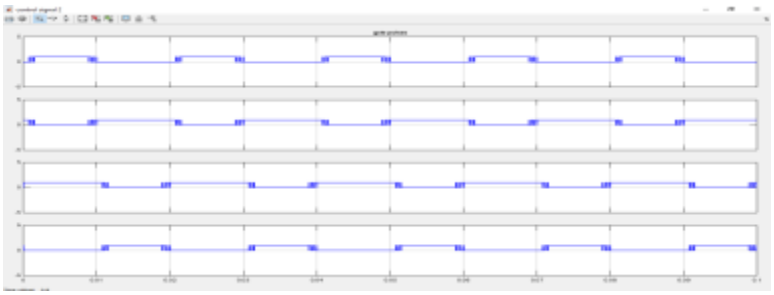

Fig-13: switching pulses

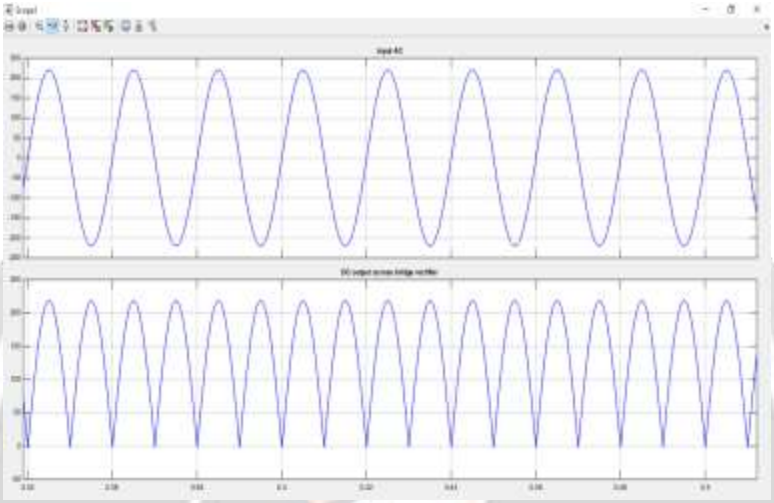

Fig-14: rectified sine waveform before filter inductor

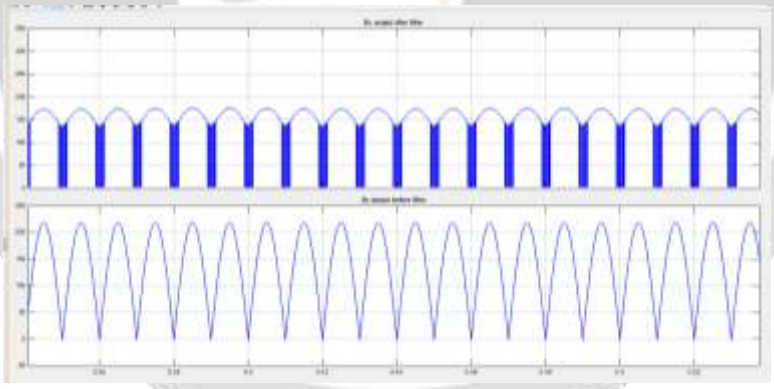

Fig-15: rectified sine waveform before filter inductor

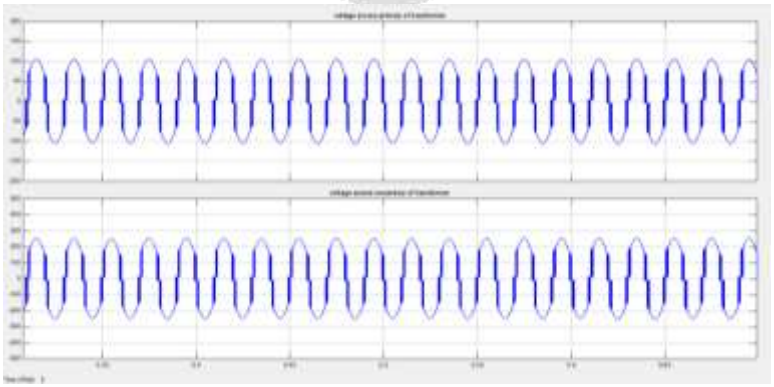

Fig-16: Transformer primary and secondary voltages

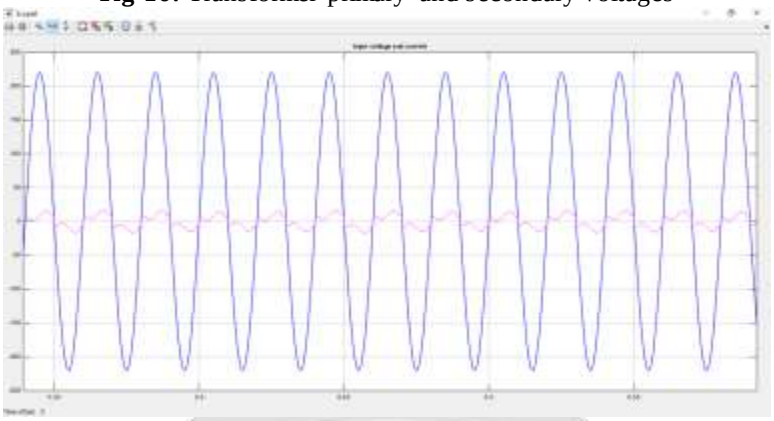

Fig-17: An in phase Voltage and current of the source

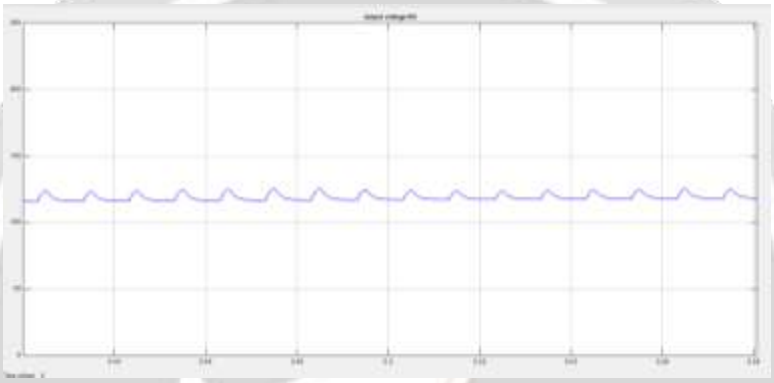

Fig-18: Output voltage of the proposed system

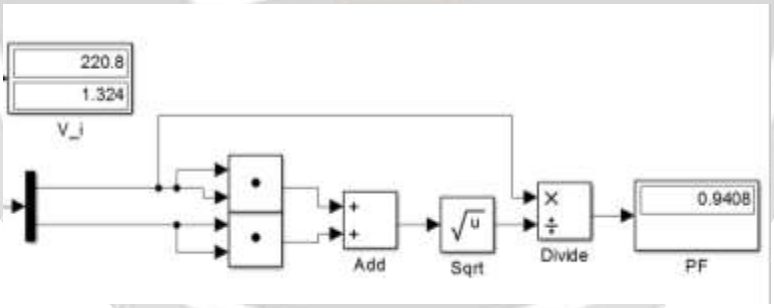

Fig-19: Power factor of the conventional system

Using this method the power factor is about 0.94.

5.2 Modified System

In this method the prototype has modified by varying the parallel capacitance across each switch which is rated about 2200e-6. So that the switch will prone to ZVS and ZCS.

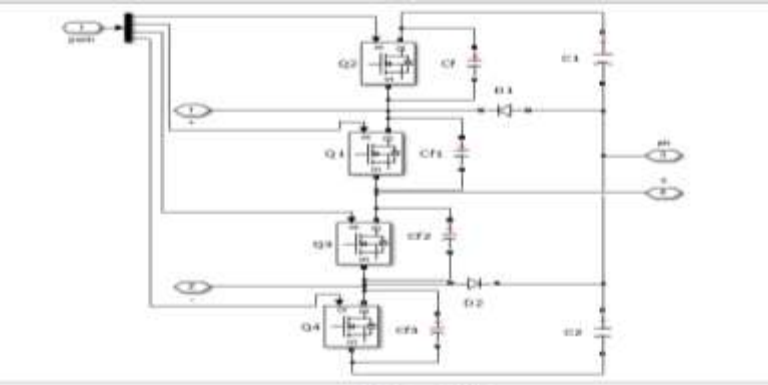

Fig.21 proposed dc-dc converter

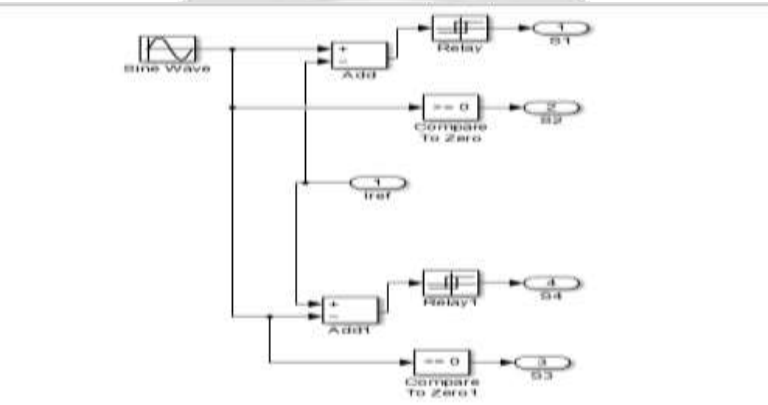

Fig.22 PWM generation using hysteresis loop

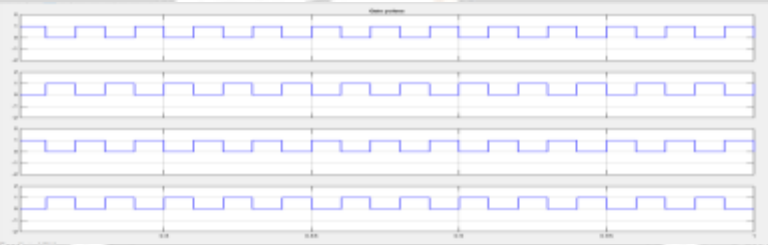

Fig.23 PWM pulses to DC_DC converter

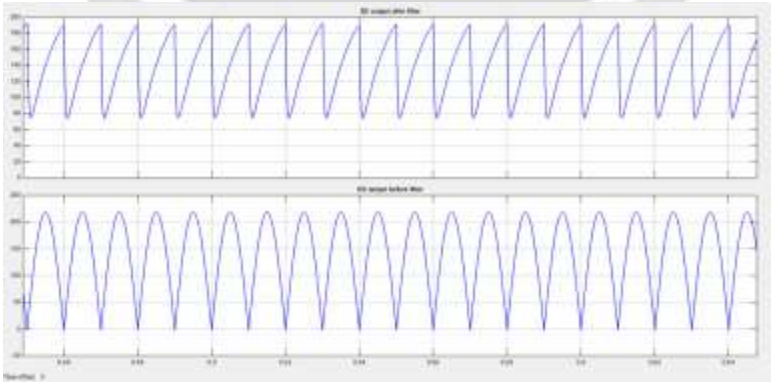

Fig.24 Rectified input for dc load applications

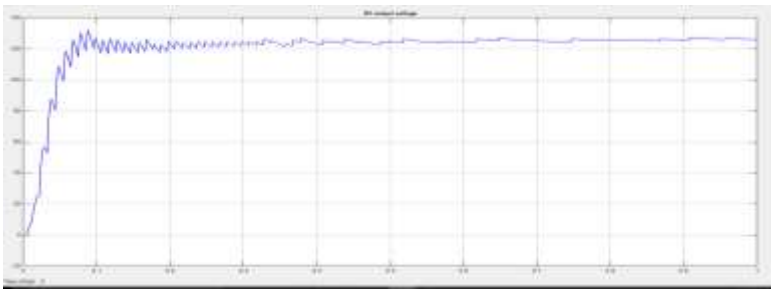

Fig.25 output voltage of the proposed system

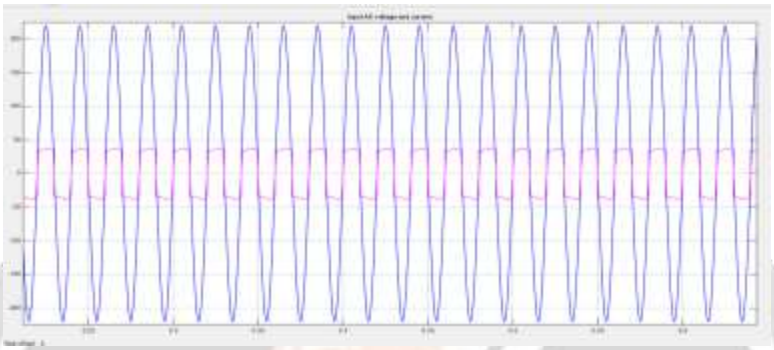

Fig.26 Input voltage and current coming to inphase

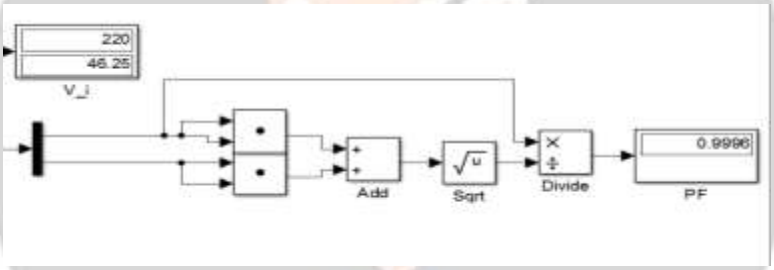

Fig.27 Power factor of the proposed system

6. CONCLUSION

In this paper, a three-level single-stage PFC ac/dc converter is proposed for low-power applications. The proposed converter exhibits high PF with less number of switches/diodes, operated at constant duty ratio. A PFC inductor and a diode bridge are added to the conventional three-level isolated dc/dc converter, while the switching scheme is modified to be compatible with single-stage operation. The input current ripple frequency is twice of the switching frequency contributing to using smaller PFC inductor. Two independent controllers, in favor of shaping the input current and regulating the output voltage, are adopted which simplifies the design and control of the circuit. The tradeoff between the PF and overall efficiency in the case of adopting a variable dc-link voltage is analyzed through developed loss model. The results of the analyses show that under 265 V line voltage, the PF can be increased to 0.99 from 0.88 by varying the dc-link voltage from 400 to 800 V. On the other hand, the efficiency of an 800 W/48 V converter can drop from 95.2% to 90% at full load. A 500Wprototype has been designed to serve as a proof-of-concept achieving a peak efficiency of 90.8% at low input line voltage.

7. REFERENCES

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