A LOW–POWER WIDEBAND LOW NOISE AMPLIFIER FOR BROADBAND WIRELESS APPLICATION

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ABSTRACT

A low power wideband low noise amplifier (LNA) for 1GHz to 10GHz wireless application presented low power consumption. A broadband Low-Noise-Amplifier LNA is presented and designed based on Resistive shunt feedback, current reuse, and gain flatting and inductive feedback technique. A current reuse scheme to lower the power consumption, along with inductive series peaking in the feedback path to increase the bandwidth, are analyzed and employed in LNA. In the low power wideband, LNA has considered low power consumption resistive shunt feedback low noise amplifier (LNA), current reuse, gain flatting technique, and inductive feedback technique for improving the deflection used high mobility electron transistor for further improvement in noise figure (NF) and s-parameter. Resistive shunt-feedback is a viable option for low power wideband LNA provides wideband input matching with the aid of feedback network. The current reuse inverter-type input facilitates doubling the effective transconductance without any extra power consumption or deterioration of output conductance.Inductive series peaking technique use to enhance the gain, input matching and noise performance. The LNA presented here achieves the lowest power consumption and employs the lowest supply voltage, when compared with other works. It also offers comparable performance in terms of gain, NF, and linearity. The LNA operates over the bandwidth of 1–10 GHz and achieves a minimum NF of 4.31 dB while consuming only 0.69 mW from a 0.5-V supply voltage. The parameters like gain input matching, output matching, reverse isolation and stability are examined by S-parameters. The Broadband low noise amplifier achieve input impedance matching S11< -22.4dB and S12< -72 for BW 1 GHz to 10GHz.

Keyword: - ADC, CMOS, LNA, LPF, WLAN, ULP**,** ULV**.**

1. INTRODUCTION

Wireless Sensor Networks (WSNs) have become highly sought after in myriad of applications, including health-care, environmental monitoring, industrial settings, and agriculture. The nature of these applications appoints accurate restrictions on the power consumption of a WSN node. As a result, Ultra-Low-Power (ULP) RF front-end circuits are required to maximize battery lifetime and to allow operation from energy cultivate from the environment.

At the same time, as the feature size in standard CMOS technologies is shrunk, the maximum allowed supply voltage is reduced as well. While operation from a low supply voltage is desirable in systems powered by energy cultivate to minimize conversion losses, it also leads to constriction on the usable circuit topologies and the speed at which they can operation from energy cultivate from environment.

Acceptable the above design challenges and the limitations of CMOS technologies like, higher output conductance, velocity saturation, and mobility debasement, the high transit frequency, f_T , of short channel CMOS technologies can be traded with power consumption to implement low power RF circuits with high bandwidths. This compromise was first highlighted in which a biasing metric is introduced for low-power RF design. This biasing metric does not include the effects of the output conductance, g_{ds} and the drain–source voltage V_{DS} on the intrinsic gain, both of which are becoming very important in Ultra-Low Voltage (ULV) and ULP designs. To address these issues, this

work suggests an extended biasing metric that is suitable for ULV and ULP low noise designs and demonstrates its applicability by designing an ULP, ULV ultra-wideband Low Noise Amplifier (LNA). The LNA is the first active component in the front-end of the receiver, and is generally considered as one of the most power hungry blocks. The high power consumption stems from the fact that an LNA must provide simultaneous wideband matching, high gain, low noise, and high linearity, all of which typically require high power and high supply voltages. These combined specifications have made the design of low-power and low voltage UWB LNAs a challenging research topic. This work reviews the challenges encountered when designing ULP, ULV circuits, and introduces an extended ULP, ULV biasing metric to optimize transistor performance. A combination of circuit techniques that are suitable for ULP ULV designs are presented, and a broadband resistive-feedback LNA in a 90-nm CMOS technology is designed using these techniques and its measured performance is hang with state-of-the-art works. The principles in the prospective low voltage and low-power design methodology presented here can be swimmingly adapted and correlated to other RF circuits.

2. LITERATURE SURVEY

[1] In this work the main focus on A D-band low-noise amplifier with gain boosting is implemented in a 0.13 SiGe BiCMOS technology, occupying 0.4 mm of IC area. This design circuit consists of two stages of cascade amplifiers with inductive common-base termination, which improves the gain by increasing the output impedance. The measurements result show more than 20 dB gains from 110 to 140 GHz, engrossing 12 mW of total dc power from a single voltage supply of 2.0 V. The measured noise figure is within 5.5 to 6.5 dB in the same frequency range. In this paper the best silicon low-noise amplifier performances up to date in this frequency range.

[2] This paper presents an innovative architecture to drastically boost the bandwidth of the Doherty power amplifier (DPA). The proposed methodology based on novel input or output splitting and combining networks, allows overcoming the typical bandwidth limiting factors of the conventional DPA. A complete and scrupulous theoretical investigation of the developed architecture is presented leading to a closed-form formulation suitable for a direct synthesis of ultra-wideband DPAs.

[3] The simultaneous noise and impedance matching (SNIM) condition for a common-source amplifier is rationalized. Transistor noise parameters are derived based on the more complete hybrid Model, and the dominant factors jeopardizing simultaneous noise and impedance matching (SNIM) are identified. Design for narrowband and broadband SNIM (BSNIM) are derived accordingly. A corresponding reactive feedback circuit along with an LC-ladder matching network is introduce to achieve the (BSNIM). It consist a capacitive and an inductive feedback, where the former supervise the transistor parasitic gate-to-drain capacitance. This circuit topology has been validated in 0.18- and 0.13- m CMOS technologies for a 3-11-GHz ultra-wideband (UWB) and a 2.4-5.4-GHz multi standard application, respectively.

[4] This paper presents the design and characterization of two broadband millimetre-wave LNAs realized in 0.25- m and 0.13- m SiGe BiCMOS technologies. Both circuits adopt a T-type matching topology to achieve the wide bandwidth (47–77 GHz for the -band LNA and 70–140 GHz for the W/F-band LNA). The measured maximum gain is about 23 dB for both LNAs. The measured noise figure (NF) is below 7.2 dB (from 50 to 75 GHz) for the -band LNA and below 7 dB for the W/F -band LNA. Both LNAs are differential circuits and consume 52/54 mW dc power. In this paper work both LNAs achieve the widest bandwidth in corresponding frequency bands with very competitive gain and NF.

[5] In this work (LNAs) fabricated in a 65-nm CMOS process are presented. By using the gain-enhanced noise-cancelling technique, the gain at noise-cancelling condition is increased, while the input matching is control. The first design work is a common-source LNA with resistive shunt feedback. It achieves a maximum power gain of 10.5 dB, a bandwidth of 10 GHz, a noise figure (NF) of 2.7–3.3 dB and an IIP3 of -3.5dBm. The power consumption is 13.7 mW from a 1-V supply, and the area is 0.02 mm. The second design work is a common-gate LNA. It executes a maximum power gain of 10.7 dB, a bandwidth of 5.2 GHz, a NF of 2.9–5.4 dB, and an IIP3 of -6dBm. The power consumption is 7 mW from a 1-V supply, and the area is 0.03 mm. Progressive results demonstrate that the first LNA shows the largest bandwidth, and the second LNA has the low power consumption among the inductor less wideband LNAs.

[6]Ultra-low voltage, highly linear, low noise integrated CMOS receiver executing from a 0.6-V supply. The receiver accumulates programmable, in band feed-forward interferer cancellation at the baseband to acquire high linearity and low noise operation at ultra-low supply voltages. Being able to reject adjacent channel or far-out blockers, the digitally calibrated interferer cancellation improves the IIP and IIP by more than 13 dB and 8 dB respectively with very little impact on the receiver noise figure. As such, it split the trade-off between linearity and noise figure, making it accessible to use a high-gain RF front-end to achieve low noise figure without affecting the linearity of the ultra-low voltage baseband circuits. The 0.6-V 900-MHz direct-conversion receiver archetype integrates a differential LNA, RF transconductors, linear quadrature current driven passive mixers, feed-forward interferer cancellation circuits, second-order channel-select filters and baseband variable gain transimpedance amplifiers.

2.1 Summary Table for Literature Review

S.No	Author Name	Publication-on year	Title of Paper	Methodogy use	Scope of year
1.	A.Cagri Ulusoy	2017	A SiGe D-Band Low-Noise Amplifier Utilizing Gain Boosting Technique	SiGe BiCMOS	Improves the gain by increasing the output impedance
2.	Sang-Ho Kam	2013	A Wideband Distributed Amplifier Employing an Envelope Tracking Technique	Envelope tracking (ET) technique	High efficiency and linearity.
3.	Gang Liu	2013	Broadband Millimetre-Wave LNAs (47–77 GHz and 70–140 GHz) Using a T-Type Matching Topology	BiCMOS technologies	Measured maximum gain, wide bandwidth,
4.	Ke-Hou Chen	2012	Inductor less Wideband CMOS Low-Noise Amplifiers Using Noise-Cancelling Technique	Gain-enhanced noise-cancelling technique	the gain at Noise -cancelling condition is increased,
5.	Ajay balankutty	2011	Ultra-Low Voltage, Low-Noise, High Linearity 900-MHz Receiver With Digitally Calibrated In-Band Feed-Forward Interferer Cancellation in 65-nm CMOS	Feed-forward Interferer cancellation	high linearity and low noise operation at ultra-low supply voltages.

2.2 TABLE II Performance summary and comparison with state-of-the-art LNAs

2.2 PROBLEM IDENTIFICATION

Parameter	[21] 2009 MCL	[35] 2010 TCAS-I	[37] 2010 MTT	[33] 2011 E,Lett.	[34] 2011 MTT	[14] 2009 ISSCC	[1] 2017 IEEE
Power (mW)	12.6	3.2	21.6	0.99	7.2	3.6	0.75
Supply (V)	1.2	0.85	1.2	1.1	1.2	1.8	0.5
S_{11} (dB)	<-9	<-9	<-10	<-10	<9.9	<-9	<-10
Gain max (dB)	12.7	14.8	10.7	7.9	16.5	21	12.6
NF (dB)	4.4	3.5~4.1	2.9~3.2	5.5~6.5	2.1~2.9	2~3.6	5.5~6.5
FOM	9.3	12.9	9	15.93	15.67	5.1	20.89

The achieve Broadband low-noise-amplifier (LNA), a combination of techniques has been utilized to enhance the performance of a shunt-feedback amplifier. As discussed in paper [1], the current reuse architecture shows the best performance for low-power and low voltage application. Goal of this work is to finding S_{11} and S_{12} parameter, to reduce the power dissipation, Improve and reduce the noise figure (NF), and Improving band width. For improving all parameter we use three analysis, first one is AC Analysis, second one is Noise analysis and third one is transient analysis.

3. METHODLOGY

Broadband Low-Noise-Amplifier for wireless amplifier is presented and designed based on an extended biasing metric for low-power and low voltage circuit design. The biasing metric is the product of the transit frequency, the transconductance efficiency, and the intrinsic voltage gain of a MOS transistor. The ULV circuit design challenges were discussed. A current-reuse scheme to lower the power consumption, along with inductive series peaking in the feedback path to increase the bandwidth, are analyzed and employed in the LNA.

The LNA originated here effectuate the lowest power consumption and employs the lowest supply voltage, when compared with other works. It also offers comparable performance in terms of gain, NF, and linearity and achieves the highest FOM I. The overall performance of this LNA based on FOM I versus power consumption and compares it with the other works in this thesis. When comparing the works using FOM II (which includes linearity), this LNA has the third highest FOM. Reduced linearity is expected due to the ultra-low supply voltage used for this LNA, however, it is interesting to note that the FOM achieved here is higher than LNAs operating from a supply voltage twice as large. The measured performance of this LNA shows that this topology is suitable for ULP, ULV, and broadband LNAs in deep sub micrometer CMOS technologies. In summary, the designed LNA outperforms the previously published works due to the following reasons having:

(1) Resistive shunt Feedback Amplifier
(2) The right choice of R_f;
(3) The right value of the bias voltages based on the extended ULP ULV biasing metric;
(4) Employing a current reuse scheme; and
(5) Using inductive series peaking in the feedback path.
(6) Gain flatting technique

Circuit Analysis of The Proposed ULP, ULV Shunt Feedback LNA

To achieve Broadband LNA, a combination of techniques has been utilized to enhance the performance of a shunt-feedback amplifier. The current reuse architecture shows the best performance for low-power and low voltage applications. As a result, this technique is employed to reduce power consumption and at the same time to improve the gain and noise performance. Input matching is achieved using the standard resistive shunt feedback technique.

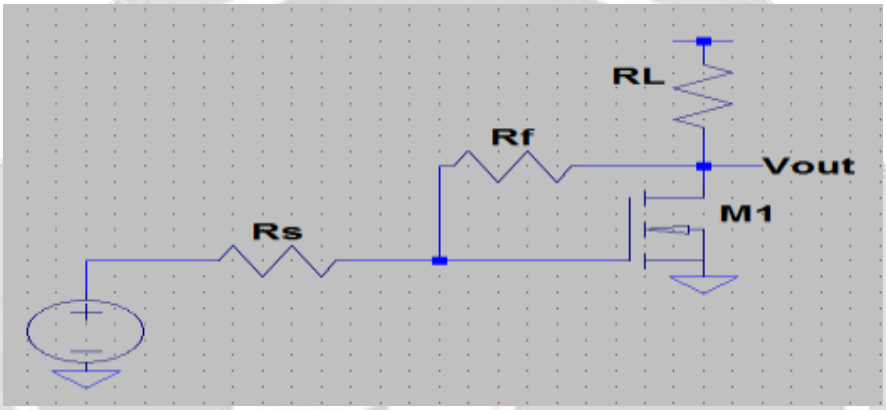
Furthermore, inductive series peaking in the feedback loop is exploited to cancel the parasitic gate–source capacitance, C_{gs}, and the Miller effect of the parasitic gate–drain capacitance, C_{gd}, to extend the input matching and bandwidth.

In this section, the proposed resistive feedback LNA will be discussed in detail with a focus on the inductive series peaking to enhance the gain, input matching, and noise performance.

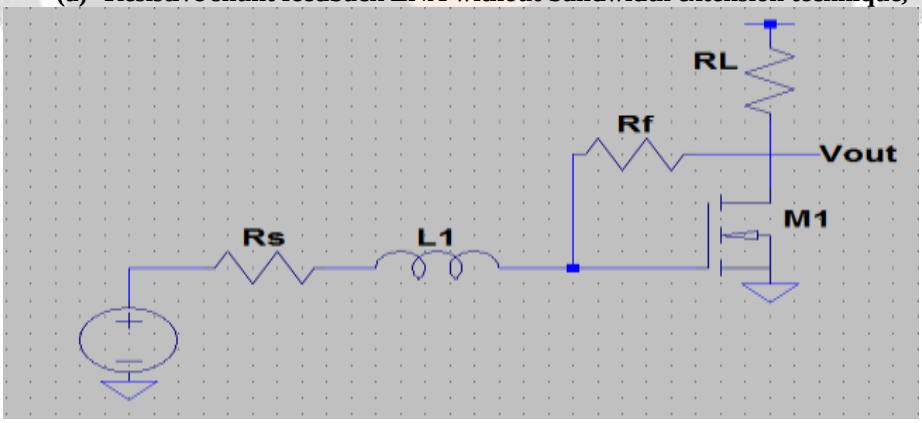
Inductive Series Peaking in the Feedback Path

Low supply voltages impose several restrictions on the circuit topologies that can be used. One common technique in LNA design is to use a cascade transistor for bandwidth and output resistance enhancement. However, the voltage drop needed by this transistor makes it impractical at low supply voltages. Consequently, other approaches must be used to extend the bandwidth of the amplifier, preferably without increasing the power consumption.

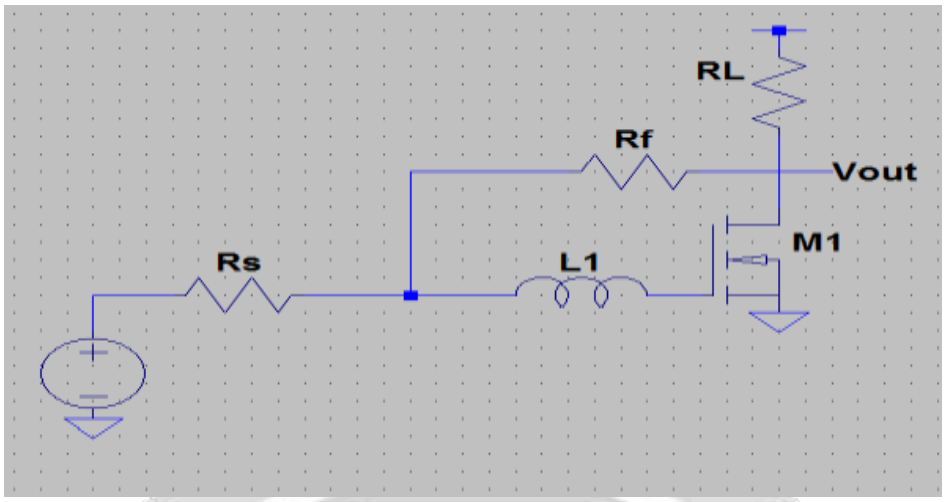
A conventional technique to extend the bandwidth without additional power consumption is to use inductors to resonate with the parasitic capacitances of the transistors.



(a) Resistive shunt feedback LNA without bandwidth extension technique,



(b) Resistive shunt feedback LNA with inductive series peaking at the input



(c)Resistive shunt feedback LNA with inductive series peaking in the feedback path.

Figure Resistive shunt feedback LNA (a) without bandwidth extension technique, (b) with inductive series peaking at the input, and (c) with inductive series peaking in the feedback path.

The core of the LNA in this work is shown in Figure in which two series peaking inductors are employed at the gates of nMOS and pMOS transistors. The ac equivalent-circuit model is also shown in Figure As can be seen in the equivalent ac model, exploiting the two inductors inside the feedback loop has two advantages. First, the inductors split the MOS Cgs and Cgd from the pad capacitance at the input of the amplifier and facilitate bandwidth extension. Another positive effect of adding the inductors inside the feedback loop is that R f and Cgd are not in parallel any more, therefore, the bandwidth of the feedback loop is also broadened. From pole-zero perspective, this technique pushes the dominant poles of the circuit to higher frequencies.

4. SIMULATION RESULTS

S-parameter There are certain parameters which are very important in design and verification of Low Noise Amplifier. Scattering parameters or S-parameters (the components of a dispersing grid or S-framework) portray the electrical conduct of straight electrical systems while experiencing different consistent state boosts by electrical signs. In this work, great input impedance matching was accomplished. Inductive peaking technique of the input helps in characterizing the matching bandwidth and the matching center frequency. By using AC analysis we can find S11, S12.

AC analysis The AC analysis is a small signal analysis in the frequency domain. In AC analysis, the DC operating point is first calculated to obtain linear, small-signal models for all non-linear components. Then the equivalent circuit is analyzed from a start to a stop frequency. The result of an AC analysis is display in two parts first gain values frequency and second one is phase versus frequency. In AC analysis we can find out quantities, voltage, current, reflection (s-parameter), impedance, admittances with respect to frequency.
In the theoretical design we calculate the result of S-parameter. In this figure shown that the value of S_{11} parameter under -10dB

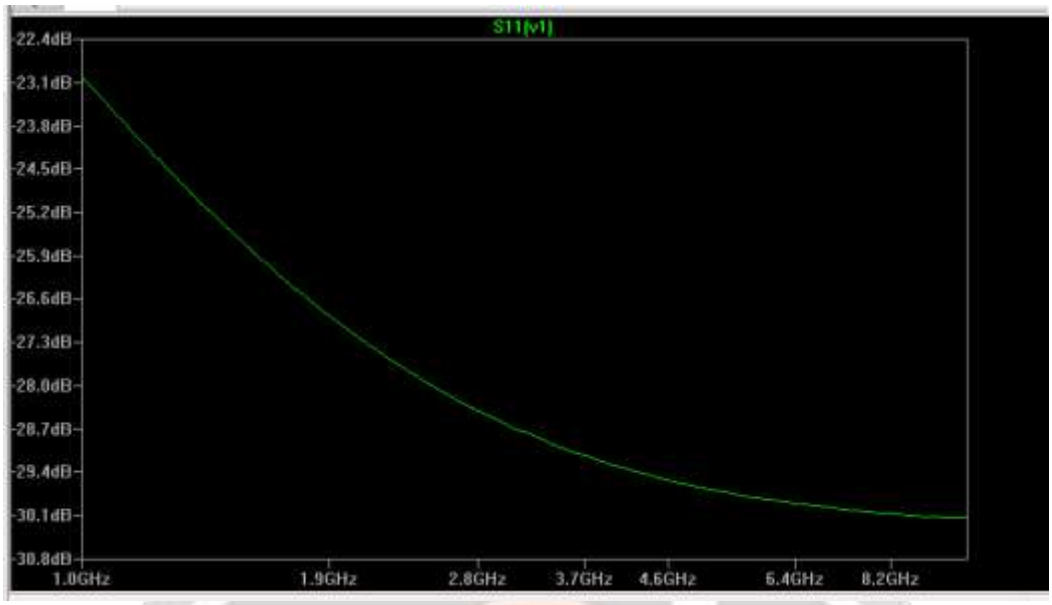


Fig. S_{11} –parameter result of theoretical design

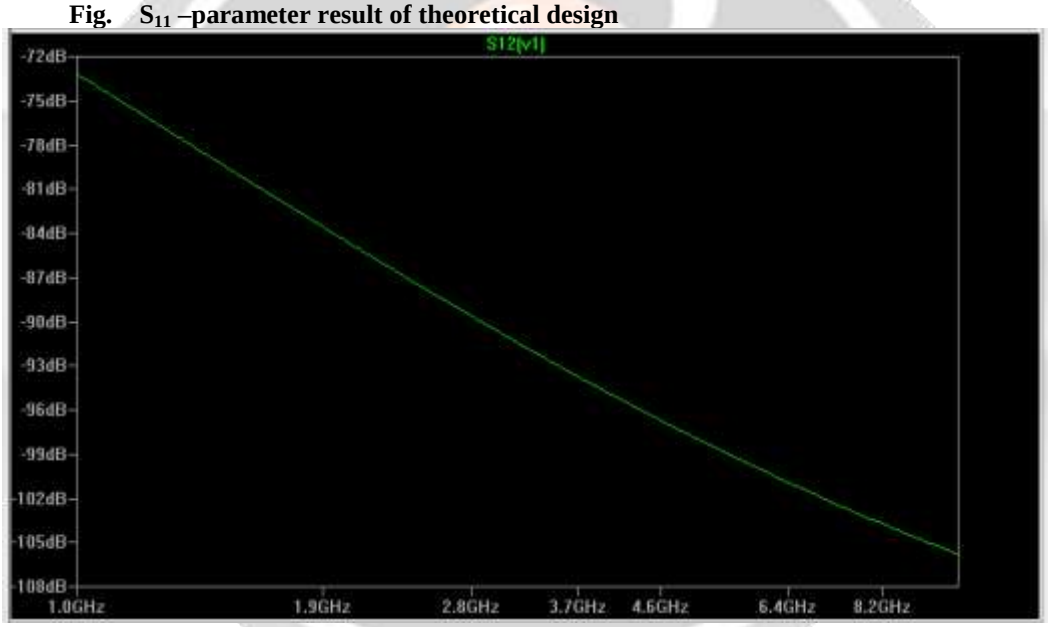


Fig. S_{12} –parameter result of theoretical design

Transient analysis The transient analysis is the calculation of a networks response on arbitrary provocation. The results are network agglomeration branch current and node voltage. Transient analysis is the consideration of energy storing components, i.e. inductors and capacitors. Transient analysis attempts to find an approximation to the analytical solution at discrete time points using numeric integration.

Figure Transient analysis output

Noise Figure In theoretical design we calculate the noise figure, output and input.Noise analysis is used to calculate the noise power spectral density generated by a circuit and the total noise power over a specified frequency range. In noise analysis type of sweep is Decade, number of points per decade is 100, starting frequency 1G, and stop frequency is 10G

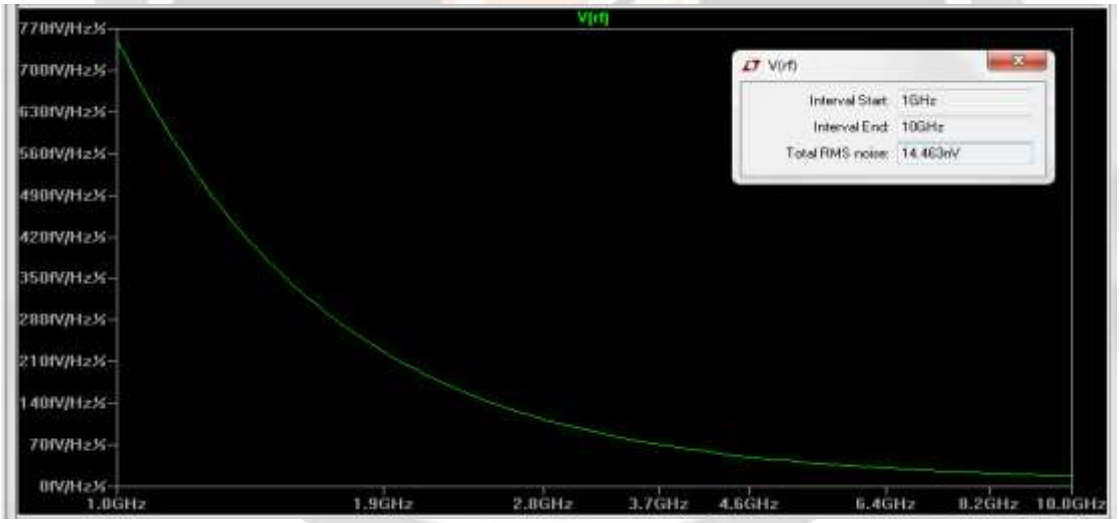


Figure Noise analysis Input noises

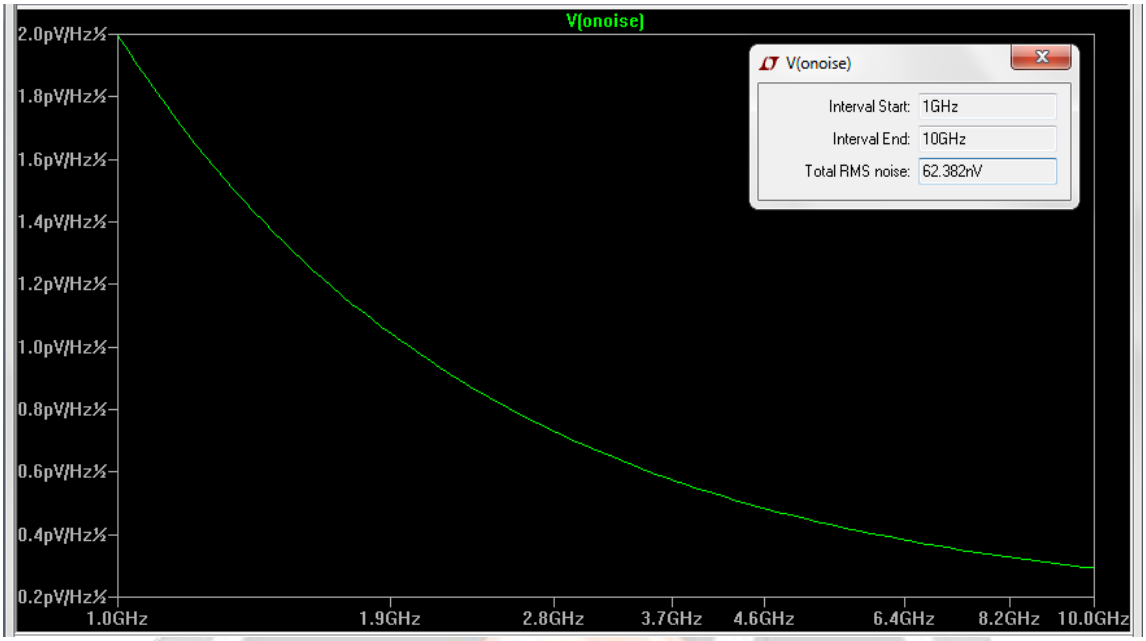


Figure Noise analysis output noise

The minimum noise figure (NF), $NF_{min,}$, of a MOS transistor is the NF at the optimum source resistance .The NF_{min} is inversely proportional to the square root of g_m and hence increases as the V_{DS} decreases.

5. CONCLUSION

This work presented a successfully investigate Broadband Low-Noise-Amplifier (LNA).The design concept is validated through three analysis AC Analysis, Noise Analysis and Transient Analysis. A broadband Low-Noise-Amplifier LNA is proposed and designed based on Resistive shunt feedback, current reuse, and gain flatting and inductive feedback technique. A current reuse scheme to lower the power consumption, along with inductive series peaking in the feedback path to increase the bandwidth, are analyzed and employed in LNA. The LNA presented here achieves the lowest power consumption and employs the lowest supply voltage, when compared with other works. It also offers comparable performance in terms of gain, NF, and linearity. The LNA operates over the bandwidth of 1–10 GHz and achieves a minimum NF of 4.31 dB while consuming only 0.69 mW from a 0.5-V supply voltage. The parameters like gain, input matching, output matching, reverse isolation and stability are examined by S-parameters. The Broadband low noise amplifier achieve input impedance matching S11< -22.4dB and S12< -72 for BW 1 GHz to 10GHz.

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