A METHOD BASED ON DYNAMIC VOLTAGE SCALING TECHNIQUE FOR POWER OPTIMIZATION

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ABSTRACT

Dynamic voltage scaling (DVS) has become a primary means for achieving power efficiency on many processor architectures. However, traditional DVS techniques cannot provide tight performance guarantees while scaling the clock frequency. We are present an elegant, theoretical approach to stochastically differentiate workloads. Based on load characterization, It is demonstrated our load-aware stochastic approach is able to reduce processor power consumption. It delivered a performance guarantee that is much better than what it is achievable with classical feedback controller. The relationship between voltage and energy makes dynamic voltage scaling (DVS) one of the powerful techniques for reduction of system power demands. Recently, techniques such as voltage downscaling, Razor DVSand Intelligent energy management have occurred as methods to voltage reduction.

Keywords- *power efficiency, clock frequency, feedback controller, power dissipation, power consumption, voltage down scaling,power demands.*

I.INTRODUCTION

A key concern in embedded systems today is power consumption. Increasing demands for heating issues and longer battery life associated with power have led researchers to develop new ways to reduce energy and power consumption in embedded systems. The importance of energy-efficient microprocessors is increasing as popularity of electronic devices increases, such as PDAs and laptops, which offer a substantial portion to general purpose processing of their power budgets. Dynamic Voltage Scaling (DVS) is the energy consumed by a microprocessor system can be scale down by dynamically adjusting the operating voltage. Lowering the voltage also requires a exposing a fundamental energy/delay trade-off and reduction in the clock frequency.

Application requirements in terms of completion deadline and execution cycles are get together to form an estimate of the perfect operating speed. The operating system is responsible for merging multiple application necessities to determine the required speed and voltage.

In recent years the power dissipation increases rapidly in a level of the order of ten of Watts because processors speed reaches Gigahertz and it converts as significant consideration in the design of microprocessors, especially battery-powered handy systems.

The research community is trying to obtain energy-efficient computing at a considerable scale. The existing or proposed approaches can be divided into two parts. The first part of methods focuses on designing software and

hardware systems that consume minimum energy as possible. In hardware design auspicious progress are evolving in processor and memory design.

Processors use a large portion of energy around 50% of the overall used energy of computer systems. Now a day's most digital circuits are constructed using CMOS circuits, especially processors, therefore to find out the relation between power, supply voltage, and clock frequency the study of power dissipation in CMOS circuits is necessary. The power dissipation for CMOS circuits is the summation of static, dynamic and short circuit powers.

The high power dissipation of a processor has at least the following disadvantages:

- Because of high power systems tend to run hot the processor and other system components get fails. The failure rate of a processor is doubles as 10 degree Celsius increase.
- It increases the operation costs.
- It reduces the battery or UPS life. The processor power get doubles after every four years, accordingly UPS life will be reduces.
- It harmful to the human body. Around 70- 100W is consumed for current high performance processors.

II. NECESSITY OF LOW POWER PROCESSORS

In the domain of analog circuit design the power management and optimization issues were considered as an essential aspect and not very demanding parameter. There is a steady and increasing requirement for low power electronic devices with the ever growing market. In order to incorporate the power issues in the design, many other significant factors associated with the system are to be observed. The delay related with the Quality of Service (QoS), system, functional and temporal requirements of the system, performance, throughput, area, reliability cost etc. So, before supporting a low power design, these major criteria has to be observed into, after examining each design alternative to find a better system design meeting all the specifications.

The battery technology has not suffered a similar growth which always puts gap called as the battery gap even though there is a significant growth in the device density. This factor also forces the need of power consumption reduction in embedded processors. Though less weight and more compact, sturdy design is demanded by the consumers, without an increase in power consumption of the system it is hard to achieve these requirements.

It affects the cooling and the packing cost as the system becomes more complex. The average current consumption in the rsange of Amperes (A) and power dissipation of high computing processors is in the form of Watts (W). Also, insusceptibility to digital noise is a problem to be find and these factors demand the need of low power processors.

III. SOURCES OF POWER CONSUMPTION IN EMBEDDED SYSTEM

The power consumption of embedded systems can be divided in two classes, namely static power and dynamic power. The dynamic power ($\boldsymbol{P_{dyn}}$) consumption gets up from the short circuit currents and discharging and charging of the load capacitance. The leakage power ($\boldsymbol{P_{leak}}$) rises again due to leakage currents that flow even when the device is not working. Thus, we have

$$\boldsymbol{P_{dyn} = \alpha C V^2 F}$$

$$\boldsymbol{P_{leak} = I_{leak} V}$$

V shows the operating voltage, F shows the operational frequency and α shows the interchanging activity. $\boldsymbol{I_{leak}}$ Shows leakage current. DVS based techniques works while the techniques which transition the system to low-power aim to reduce leakage energy by reducing dynamic energy

IV. DYNAMIC VOLTAGE SCALING

Dynamic voltage scaling (DVS) is a technique used for reducing energy consumption of processors by varying the frequency and voltage at run time. The main idea is to reduce voltage or frequency during periods when the processor has a decrease in workload. The energy consumed by GPU is given by the following equation

$$E = CV^2 * f_{clk}$$

Where,

E = Energy used by GPU Measured in joules (J);

C = Capacitance;

V = Voltage supply to GPU;

f_{clk} = Clock frequency of GPU.

Thus, the power used by a task may be reduced by decreasing V or F, or both. However, reducing the frequency may simply take more time to complete the work for tasks that require a fixed 5 amount of work. So there will be no energy saving. Therefore, intelligent DVS techniques are needed to expand the energy efficiency of GPUs. Since processor frequency has a strong impact on temperature and power consumption. Dynamic voltage scaling (DVS) are the most commonly used techniques in modern processors.

A. Analysis of DVS Technique

Dynamic voltage scaling (DVS) is preferred as a method to scale down power and energy utilization of microprocessors. Lowering only the operating frequency f_{clk} can scale down the power utilization but the energy utilization remains the same because the computation needs more time to end. Lowering the supply voltage V_{dd} can scale down a significant amount of energy because of the quadratic relation between power and V_{dd} as given in Equation 2. Lowering the supply voltage and operating frequency scale downs the power and energy utilization further. Figure 1 shows the power saving feasible by using variable.V_{dd}

When the clock frequency f_{clk} is scale down by half, this lowers the processor's power utilization and still allows task to complete by deadline, the energy utilization remains the same. Decline the voltage level $V_{dd}$by half scale down the power level more without any corresponding increase in execution time. As a result the energy utilization is scale down significantly, but the appropriate performance is remained .

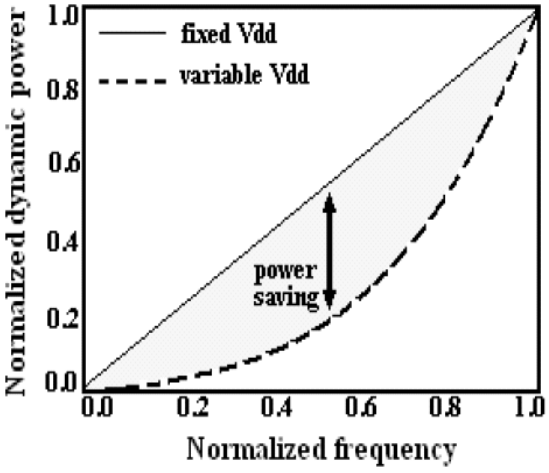

Fig. 1: Power saving achievable by using variable V_{dd}

There are three key components for implementing DVS technique in processors:

1. An operating system which cleverly vary the processor speed.

2. A control loop which generates the voltage desired for the required speed.

3. A microprocessor which operates over a range of voltages.

We now discuss some power management technique.

B. DVS and Power-Aware Scheduling based Techniques

DVS is a method for changing the voltage or frequency of an estimating system based on work and power requirements. For CMOS circuits, dynamic power is accompanying with voltage and frequency as $\boldsymbol{P \alpha F V^2}$ and hence, by scale down the frequency, the voltage at which the circuit necessities to be operated for steady operation can also be sinker, which leads to energy saving. Several commercial microprocessors support DVS technology for saving power, e.g. AMD Power Now and Intel's Speed Step. The disadvantage of DVS is that it may increase execution time and also harms the performance.

DVS needs programmable clock generator and DC-DC converter. Further, voltage transitions may need time on the order of tens of microseconds. Finally, the returns from DVS are decline due to increase in leakage energy and trend of using multi-core processor instead of increasing clock frequency.

C. Using Power Modes

In embedded systems, to save energy the hardware typically provides a range of operating modes. Different modes to return back to the normal mode consume different amount of power and take different time for each mode. In general, the modes with higher energy consumption also take the shortest time to return to the normal mode and vice versa. Keep the performance loss limited for saving energy and these modes should be carefully used. Also, when the system is idle a low-power mode can be used, for actually performing or servicing a request the task the system must return back to the normal mode.

V. EXPERIMENTAL RESULT

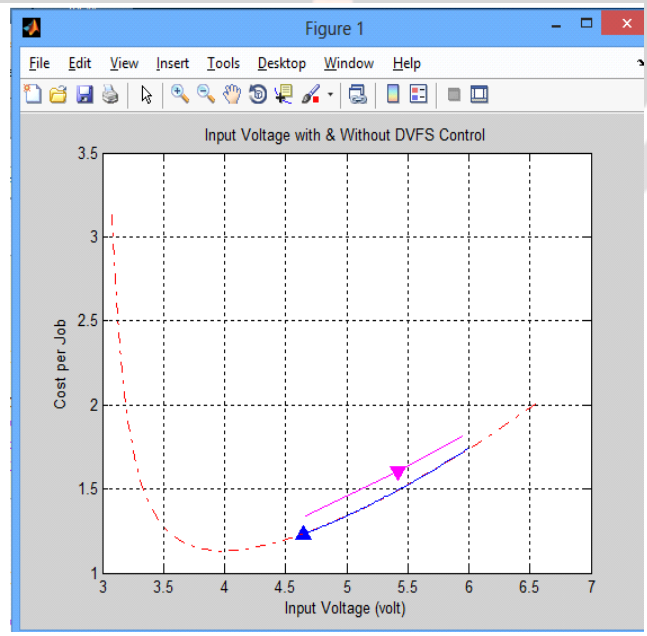

Fig.2: Input Voltage with and without DVFS Control

VI. CONCLUSION

In this paper, technique for power consumption reduction for a processor is carried out using dynamic Voltage Scaling technique. The presented technique can decrease the processors average energy consumption.

The proposed scheme produced to provide a performance bound and achieve significant power saving that is tighter than the existing feedback control scheme. The future work will extend this method to nonlinear controllers using the systemanalysis tools.

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