A NOVEL REDUCED-SWITCH MLI TOPOLOGY FOR GRID TIED SOLAR-PV SYSTEM

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ABSTRACT

Due to the depletion of conventional energy sources and environmental impacts, the role of renewable sources for energy generation has become a prior choice nowadays. A solar photovoltaic (PV) based micro-grid with a reduced-switch MLI topology has been presented. The proposed MLI topology is designed with the aim of reducing the number of switches and the number of dc voltage sources with modularity while having a higher number of levels at the output. For the determination of the magnitude of dc voltage sources and a number of levels in the cascade connection, three different algorithms are proposed. The optimization of the proposed topology is aimed at achieving a higher number of levels while minimizing other parameters. A detailed comparison is made with other comparable MLI topologies to prove the superiority of the proposed structure. A fundamental frequency PWM technique is used for pulses to the switches to achieve high-quality voltage at the output. Finally, the proposed 71-level RSMLI topology is designed by using cascading form of two basic 11-level RSMLI topologies to drive the micro-grid system powered by solar-PV system, simulated results are presented with proper comparisons.

Keyword: - *Multilevel Inverter (MLI), Fundamental Frequency Switching Technique, Reduced-Switch MLI, Micro-Grid, Solar-PV System*.

1. INTRODUCTION

A mid of crucial period is implied during its evolution in an electric power industry. A high range of violations are occurred in both transmission-distribution levels which have some critical expectations followed in a very near future. The energy generation plays a key role to determine the economic growth level & sustainable development in all over the country. Several ranges of eminent challenge & significant despite growth level in overall generation plays a major concerns facing by India's power sector. Over the several years ago, India's power sector is highly suffering from unconstrained supplies & energy shortages. To implement this energy standard challenges are developed based on economy range of world 21st century by grid standards [1]. Nowadays Renewable Energy Sources (RES) are getting widely used with the accumulation of demanded energy and major concerns related to environmental impacts around the world due to usage of fossil fuels. Over the various renewable energy sources, the solar-PV is best suited due to ample in nature, virtuous and toxic nature, etc.

The energy coming from the solar-PV is integrated to micro-grid by using power conditioning system; it consists of DC-DC converters and DC-AC inverters with a suitable control scheme. But, various issues in traditional 2-level and 3-level VSI are not suited affectively due to square-wave output voltage, high dv/dt stress, more common-mode voltage, high switching losses and low efficiency, requires large-sized filters for getting sinusoidal outputs [2]. All the above issues are eliminated by introducing the Multi-Level Inverters (MLIs), at present MLIs plays a key role in grid-connected system. The concept of multilevel converters has been introduced since 1975. The cascade multilevel inverter was first proposed in 1975. Separate DC -sourced full-bridge cells are placed in series to synthesize a staircase AC output voltage. The term multilevel began with the three-level converter [3].

Subsequently, several multilevel converter topologies have been developed. In 1981, diode-clamped multilevel inverter also called the Neutral -Point Clamped (NPC) inverter schemes were proposed. In 1992, capacitor-clamped (or flying capacitor) multilevel inverters, and in 1996, cascaded multilevel inverters were proposed.

Although the cascade multilevel inverter was invented earlier, its application did not prevail until the mid-1990s. The advantages of cascade multilevel inverters were prominent for motor drives and utility applications [4]-[6].

These multilevel inverters can extend rated inverter voltage and power by increasing the number of voltage levels. They can also increase equivalent switching frequency without the increase of actual switching frequency, thus reducing ripple component of inverter output voltage and electromagnetic interference effects. A multilevel converter can be implemented in many different ways [7]. The simplest techniques involve the parallel or series connection of conventional converters to form the multilevel waveforms. More complex structures effectively insert converters within converters. The voltage or current rating of the multilevel converter becomes a multiple of the individual switches, and so the power rating of the converter can exceed the limit imposed by the individual switching devices. For higher levels, these MLI topologies are not suitable due to increasing of number of switches with respect to increased voltage levels, to overcome these issues by adopting novel Reduced-Switch MLI topologies [8]-[12].

The proposed MLI topology is designed with the aim of reducing the number of switches and the number of dc voltage sources with modularity while having a higher number of levels at the output. For the determination of the magnitude of dc voltage sources and a number of levels in the cascade connection, three different algorithms are proposed [13]-[17]. The optimization of the proposed topology is aimed at achieving a higher number of levels while minimizing other parameters [18]-[21]. A detailed comparison is made with other comparable MLI topologies to prove the superiority of the proposed structure. A fundamental frequency PWM technique is used for pulses to the switches to achieve high-quality voltage at the output. Finally, the proposed 71-level RSMLI topology is designed by using cascading form of two basic 11-level RSMLI topologies to drive the micro-grid system powered by solar-PV system, simulated results are presented with proper comparisons.

2. ANALYSIS AND DESCRIPTION OF PROPOSED MULTILEVEL TOPOLOGY

2.1 Basic Unit of Proposed Topology

Fig.1 shows the basic unit of the suggested multilevel inverter topology. The assembly consists of three dc voltage sources along with six unidirectional switches and one bidirectional switch. Switch pair (S1, S2) and (S5, S6) can be termed as outer switches, and only one switch is necessary to be turned ON from each pair. The switches of outer pairs should also operate in a complementary mode to avoid short-circuiting the dc voltage sources. These outer switches are connected across voltage source V1. The remaining two dc voltage sources with V2 magnitude are connected in series with additive polarity, along with unidirectional switches S3, S4 and bidirectional switch S11 forms the inner portion of the proposed basic unit. Only one switch is required to be turned ON in between these three switches. Considering these facts, the switching table for the proposed basic unit is given in Table 1.

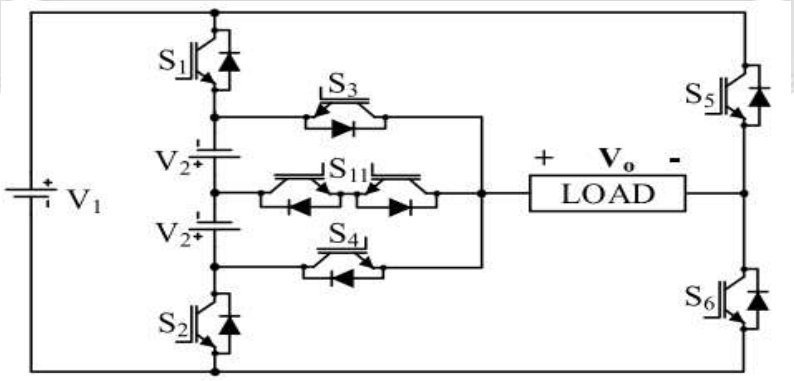


Fig.1. Basic unit of the proposed topology

Table.1. Switching table of the proposed basic unit

S_1	S_2	S_3	S_4	S_5	S_6	S_{11}	V_o
ON	OFF	ON	OFF	ON	OFF	OFF	0
ON	OFF	ON	OFF	OFF	ON	OFF	V_1
ON	OFF	OFF	OFF	ON	OFF	ON	V_2
ON	OFF	OFF	OFF	OFF	ON	ON	V_1+V_2
ON	OFF	OFF	ON	ON	OFF	OFF	$2V_2$
ON	OFF	OFF	ON	OFF	ON	OFF	V_1+2V_2
OFF	ON	OFF	ON	OFF	ON	OFF	0
OFF	ON	OFF	ON	ON	OFF	OFF	$-V_1$
OFF	ON	OFF	OFF	OFF	ON	ON	$-V_2$
OFF	ON	OFF	OFF	ON	OFF	ON	$-(V_1+V_2)$
OFF	ON	ON	OFF	OFF	ON	OFF	$-2V_2$
OFF	ON	ON	OFF	ON	OFF	OFF	$-(V_1+2V_2)$

2.2 Generalized Structure of Proposed Topology

The proposed basic unit is able to achieve 11 levels at the output employing three dc voltage sources. In order to generate more number of levels, the basic unit can be extended as shown in Fig.2. In this extension, the number of dc voltage sources, which is connected to the inner portion of the module, is increased along with bidirectional switches. The switches used in the proposed topology can be grouped into three cells. Cell 1 is made up of switches S1 and S2. Switches in cell 1 are operated at fundamental frequency as both have to bear maximum voltage stress.

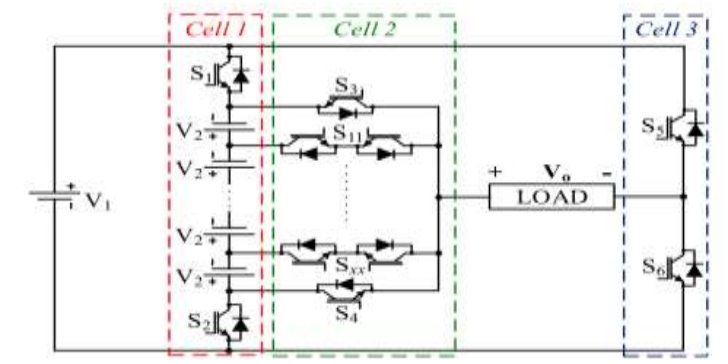


Fig.2. Generalized structure of the proposed topology

In cell 2 consist of all the inner switches and each switch turns ON for any two levels in the one-half cycle. Similarly, cell 3 consists of two switches S5 and S6 and both of them operate at a high frequency. The generalized equations for the proposed topology with k number of dc voltage sources are given as:

$$\text{Maximum number of Levels} = N = 4k - 1 \quad (1)$$

$$\text{Number of Switches} = N\text{switch} = 2k + 2 \quad (2)$$

$$\text{Number of Driver Circuits} = N\text{driver} = k + 4 \quad (3)$$

$$\text{Peak Output Voltage} = V_{o,max} = V1 + (k - 1)\, V2 \quad (4)$$

$$\text{Variety of dc sources} = N\text{variety} = 2 \quad (5)$$

2.3 Selection of Magnitude of DC Voltage Sources

The selection of dc voltage sources used in the proposed topology is an important criterion for practical applications. One such benchmark is the variety of dc voltage sources i.e. how many different magnitudes of dc voltage sources are employed in the topology. For the proposed topology, only two different magnitudes of dc voltage sources are required. Another important aspect related to dc voltage sources is their magnitude selection. For the proposed topology, the peak output voltage of the proposed topology is given in (6).

$$V_{o,max} = V_1 + (k-1)\, V_2 = \left(\frac{N-1}{2}\right) \times V_{dc} \quad (6)$$

For the generalized structure, the selection of dc voltage sources can be done in two modes. In MODE I, the magnitude of V1 is selected as Vdc. Then from (1) and (6), the magnitude of V2 is calculated as

V1-Vdc, V2 = 2Vdc (7)

Similarly, in MODE II, the magnitude of V2 is fixed as Vdc. Then the magnitude of V1 from (1) and (6) is

$$V_1 = \frac{N - 2k + 1}{2} V_{dc} = kV_{dc} \quad (8)$$

The magnitude of dc voltage sources in MODE I is fixed as V1 = Vdc and V2 = 2Vdc irrespective of the number of dc voltage sources, whereas for MODE II, the magnitude of V1 is depend on k. Therefore, with a higher number of dc voltage sources, the magnitude selection of dc voltage sources in MODE II becomes impractical. Fig.3 shows all the voltage states in a positive half cycle of the basic unit with voltage sources configured in MODE I.

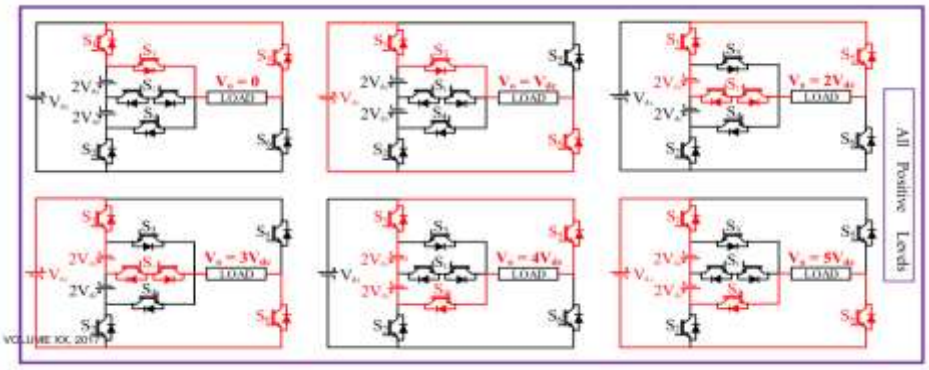


Fig.3. Different switching states of the proposed basic unit with MODE I in positive half cycle

3. PROPOSED CASCADE CONNECTION OF BASIC 11-LEVEL RSMLI TOPOLOGY

Cascading several modules is another way to increase the number of levels at the output. Fig. 4 shows the cascade connection of the proposed topology with m modules.

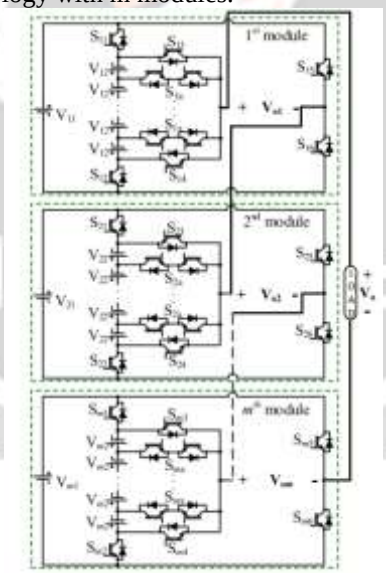


Fig.4. Cascade connection of proposed RSMLI Topology using Basic 11-Level Modules

The output voltage across the load is the sum of all the voltages generated by each module connected in cascade, i.e.,

Vo = Vo1 + Vo2 + . . . + Vom (9)

In order to maintain the modulatory, each module connected in cascade is assumed to be identical i.e. each module has the same number of switches and dc voltage sources. The equations for the proposed topology with m modules in cascade, and with k number of dc voltage sources in each module are given as:

Nswitch = m × (2k + 2) (10)

Ndriver = m × (k + 4) (11)

Nsource = m × k (12)

The number of output levels for the cascade connection depends on the magnitude of dc voltage sources in each module. The magnitude of dc voltage sources of each module can be selected by three different algorithms, described as follows.

4. GRID CONNECTED PV CELL MODEL

4.1 PV Cell Model

The equivalent circuit of a PV cell is shown in Fig.5. It includes a current source, a diode, a series resistance and a shunt resistance.

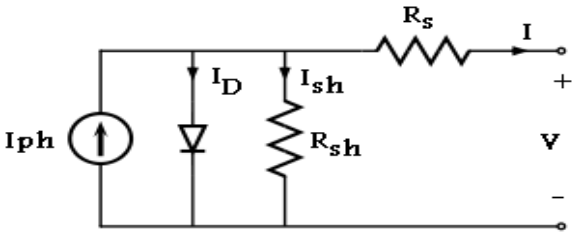


Fig.5 PV cell equivalent circuit

In view of that, the current to the load can be given as:

$$\mathrm{I} = I_{ph} - I_s\left(\exp q\frac{\left(v + R_s I\right)}{NKT}\right) - 1 - \left(\frac{v + R_s I}{R_{sh}}\right) \tag{13}$$

In this equation, *Iph* is the photocurrent, *Is* is the reverse saturation current of the diode, *q* is the electron charge, *V* is the voltage across the diode, *K* is the Boltzmann's constant, *T* is the junction temperature, *N* is the ideality factor of the diode, and *Rs* and *Rsh* are the series and shunt resistors of the cell, respectively. As a result, the complete physical behavior of the PV cell is in relation with *Iph*, *Is*, *Rs* and *Rsh* from one hand and with two environmental parameters as the temperature and the solar radiation from the other hand.

4.2 Grid Connected System

Grid-connected photovoltaic power system is electricity generating solar PV system that is connected to the utility grid. A grid-connected PV system consists of solar panels, one or several inverters, a power conditioning unit and grid connection equipment. They range from small residential and commercial rooftop systems to large utility-scale solar power stations. Unlike off-grid systems, a grid-connected system rarely includes an integrated battery solution, as they are still very expensive. When conditions are right, the grid-connected PV system supplies the excess power, beyond consumption by the connected load, to the utility grid. The energy coming from the solar-PV is integrated to micro-grid by using proposed 71-Level RSMLI Topology is depicted in Fig.6; it consists of solar-PV system and 71-level RSMLI topology integrated to micro-grid system.

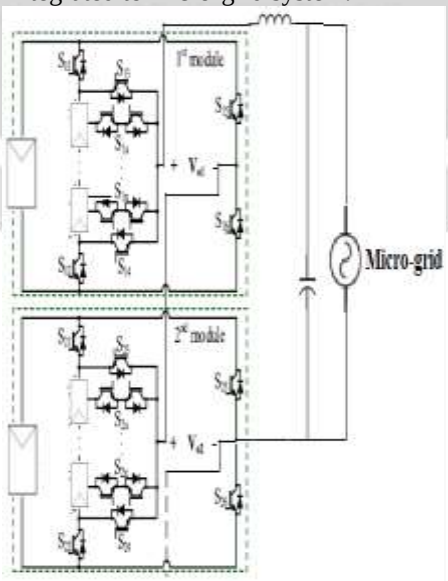


Fig.6 Proposed Solar-PV Tied Grid Integrated RSMLI Topology

5. MATLAB/SIMULINK RESULTS & ANALYSIS

The Matlab/Simulink modelling is carried based on various cases and the proposed models are developed by using described system specifications illustrated in Table.2.

Table.2 System Specifications

S. No	Parameter	Value
1	Input DC Source	Vdc1-10V, Vdc2-20V
2	Load Impedance	R-Load-100 Ω; RL-Load= R-80Ω, L-200mH
3	Fundamental Switching Frequency	Fs-50Hz
4	Solar-PV	Vpv1-7.5V, Vpv2-13V
5	Line Interfacing Filter	R_f-50Ω, L_f-1000 µH, Lf-100mH
6	Grid System	Vg-230V, 50Hz

5.1 DESIGN OF PROPOSED 11-LEVEL RSMLI TOPOLOGY FOR STANDALONE R-LOAD SYSTEM

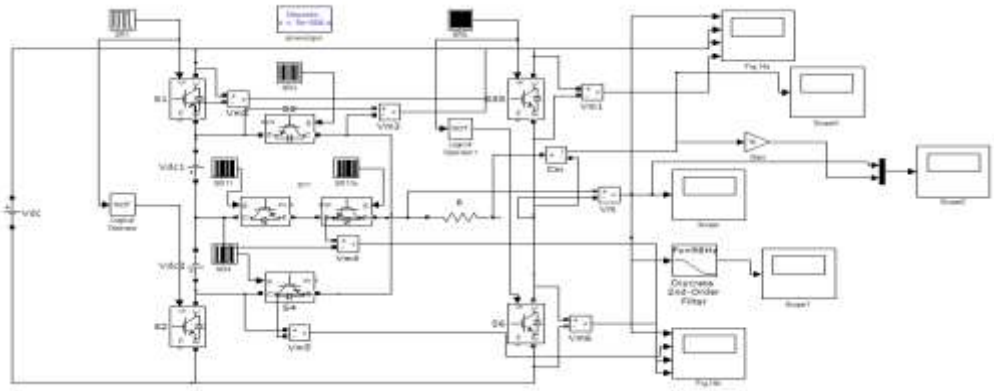
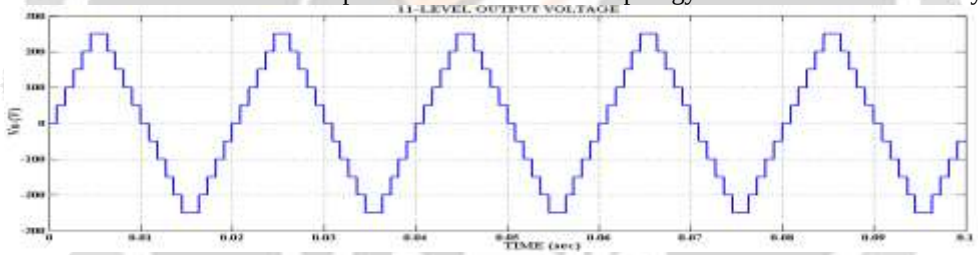
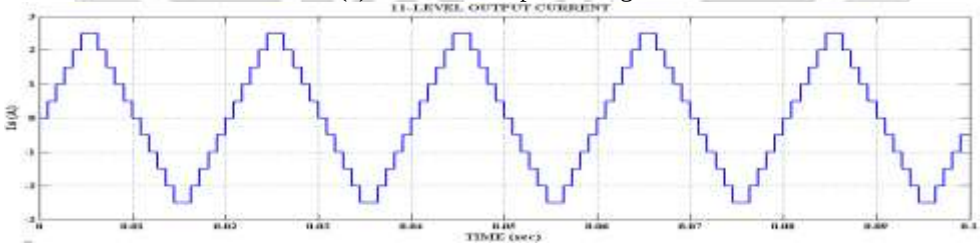


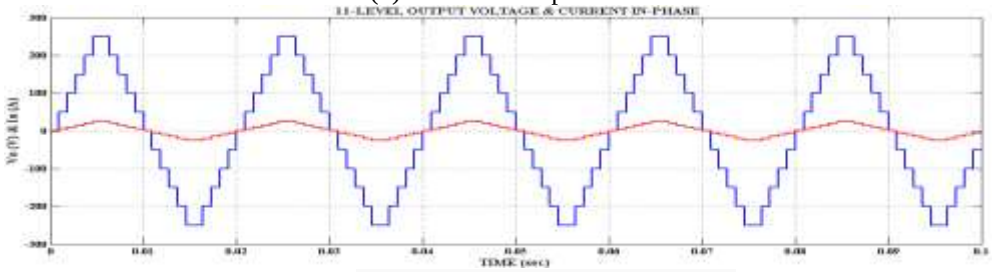
Fig.7 Matlab/Simulink Model of Proposed 11-level RSMLI Topology for Standalone R-Load System



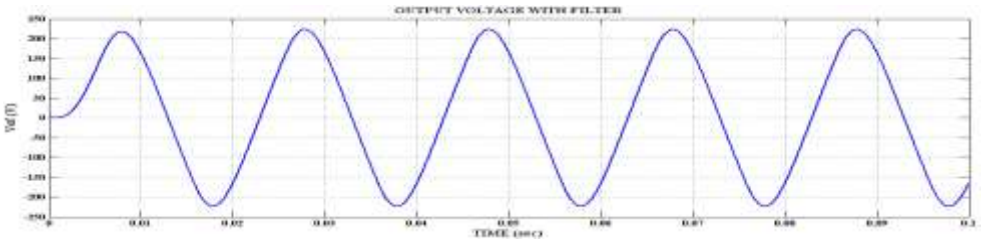
(a) 11-level Output Voltage



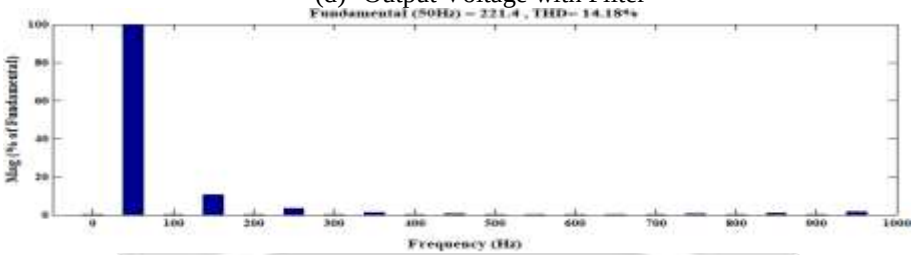
(b) 11-level Output Current



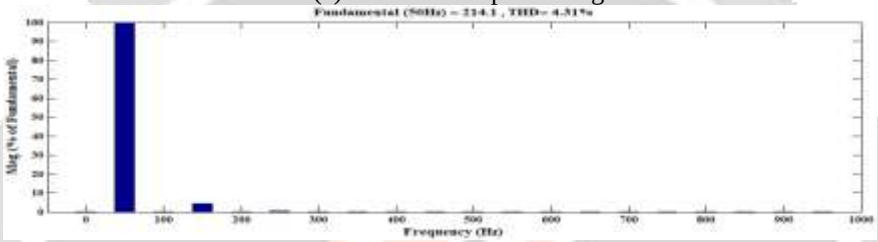
(c) Output Voltage & Current-In phase



(d) Output Voltage with Filter



(e) THD of Output Voltage

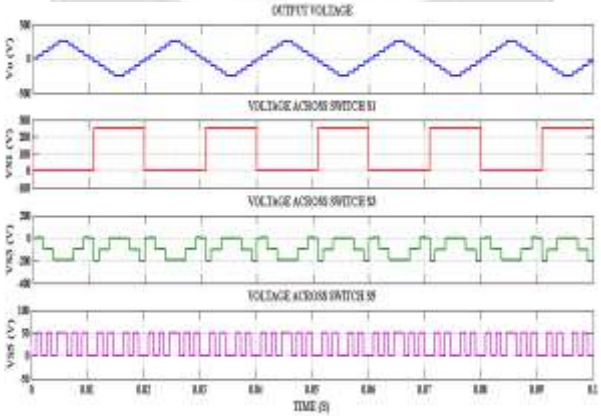


(f) THD of Output Voltage with Filter

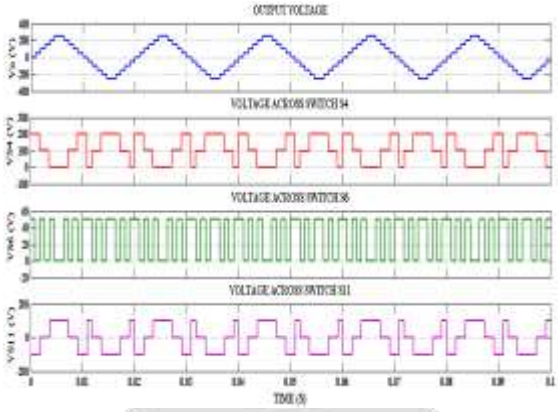
Fig.8 Simulation Results of Proposed 11-level RSMLI Topology for Standalone R-Load System

The Matlab/Simulink Model of Proposed 11-level RSMLI Topology for Standalone R-Load System is depicted in Fig.7. Simulation Results of Proposed 11-level RSMLI Topology for Standalone R-Load System is depicted in Fig.8. It Includes, (a) 11-level Output Voltage, (b) 11-level Output Current, (c) Output Voltage & Current-In phase, (d) Output Voltage with Filter, (e) THD of Output Voltage, (f) THD of Output Voltage with Filter, respectively. The output voltage and current for a basic 11-level RSMLI driven pure R-load having a load value of 100**Ω**, the output voltage is measured with a value of 250V and output current is measured with a value of 2.5A. For a pure R-load, the output current is in-phase with the output voltage represents the unity power-factor. The output voltage with filter carries a sinusoidal voltage with a value of 220V, the THD value of 11-level output voltage is 14.18% and the THD value of 11-level output voltage with filter is 4.31%, it is well within IEEE-519 standards.

Fig.9 (a)-(b) show the voltage stress of different switches of the basic unit. The voltage stress across switch S1 is the maximum with a value of 250V. The pattern of voltage stress across switch S2 is the same as that of S1 with the magnitude of 250V. The voltage stress across switches S3 and S5 is 200V and 50V, respectively, as indicated in Fig.9 (a). Fig.9 (b) shows the voltage stress variation of switches S4, S6 and bidirectional switch S11 with output voltage Vo.



(a)



(b)

Fig.9 Output voltage waveform Vo with voltage stress across switches (a) S1, S3, and V5 (b) S4, S6, and V11.

5.2 DESIGN OF PROPOSED 11-LEVEL RSMLI TOPOLOGY FOR STANDALONE RL-LOAD SYSTEM

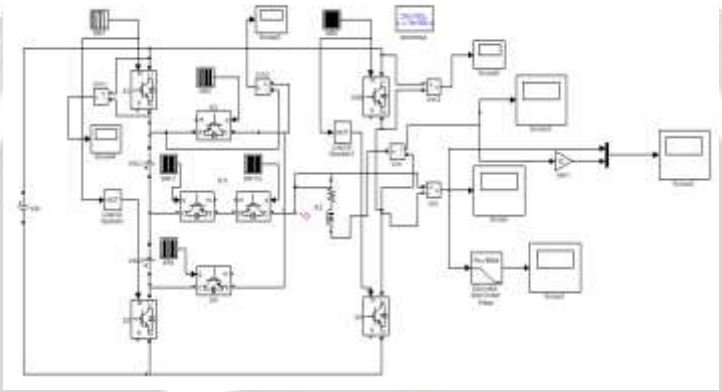
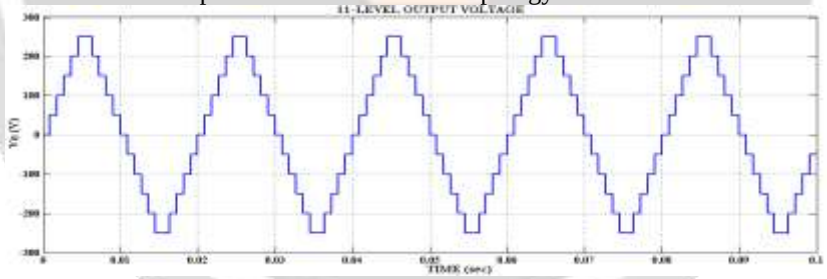
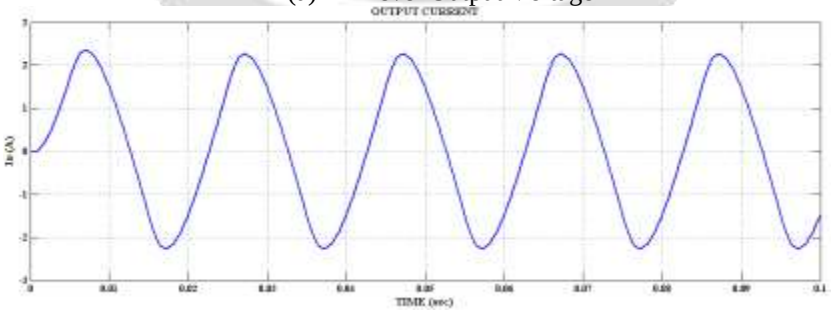


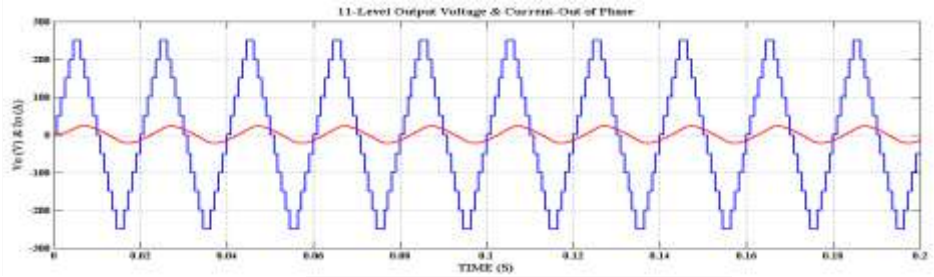
Fig.10 Matlab/Simulink Model of Proposed 11-level RSMLI Topology for Standalone RL-Load System



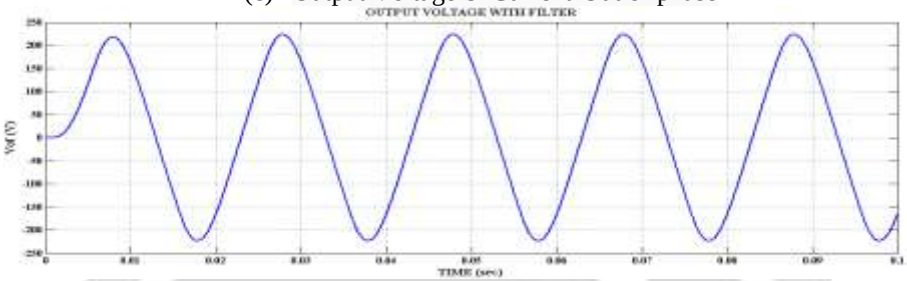
(a) 11-level Output Voltage



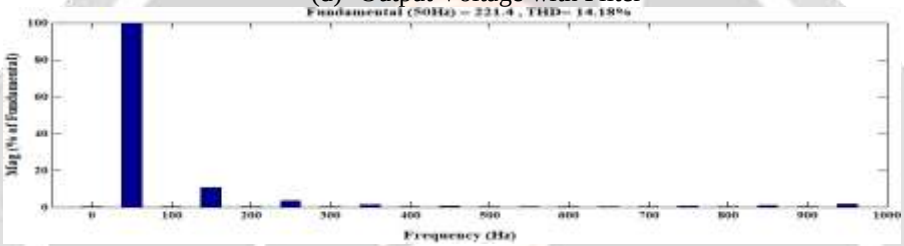
(b) Output Current



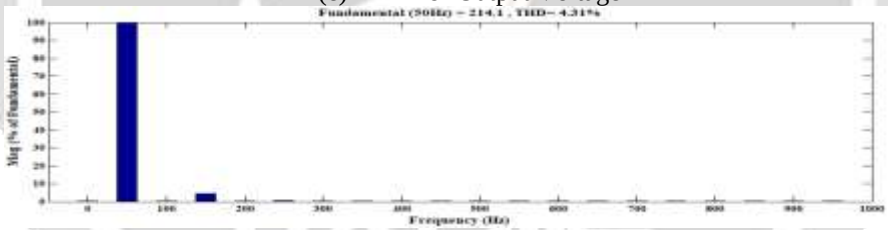
(c) Output Voltage & Current-Out of phase



(d) Output Voltage with Filter



(e) THD of Output Voltage



(f) THD of Output Voltage with Filter

Fig.11 Simulation Results of Proposed 11-level RSMLI Topology for Standalone RL-Load System

The Matlab/Simulink Model of Proposed 11-level RSMLI Topology for Standalone RL-Load System is depicted in Fig.10. Simulation Results of Proposed 11-level RSMLI Topology for Standalone RL-Load System is depicted in Fig.11. It Includes, (a) 11-level Output Voltage, (b) 11-level Output Current, (c) Output Voltage & Current-Out of phase, (d) Output Voltage with Filter, (e) THD of Output Voltage, (f) THD of Output Voltage with Filter, respectively. The output voltage and current for a basic 11-level RSMLI driven pure RL-load having a load value of 80Ω and 200mH the output voltage is measured with a value of 250V and output current is measured with a value of 2.5A. For a RL-load, the output current is out of phase with the output voltage represents the non-unity power-factor. The output voltage with filter carries a sinusoidal voltage with a value of 220V, the THD value of 11-level output voltage is 14.18% and the THD value of 11-level output voltage with filter is 4.31%, it is well within IEEE-519 standards.

5.3 DESIGN OF PROPOSED 71-LEVEL RSMLI TOPOLOGY FOR STANDALONE R-LOAD SYSTEM

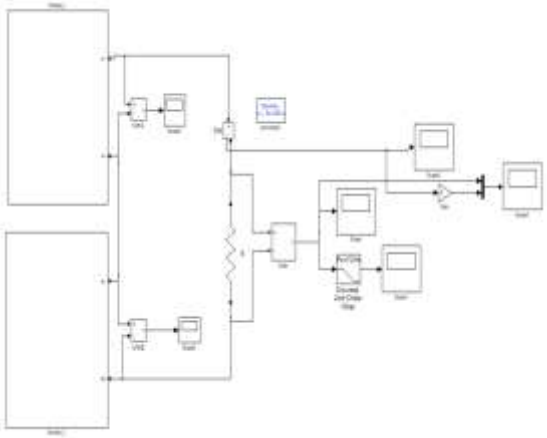
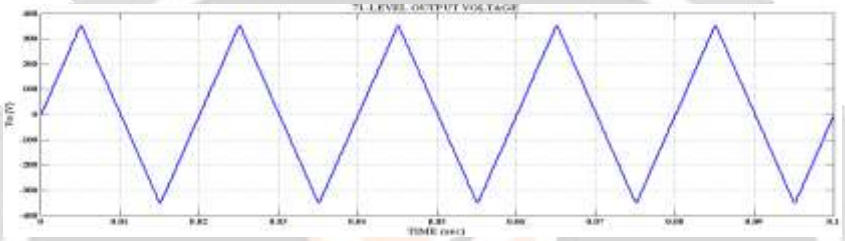
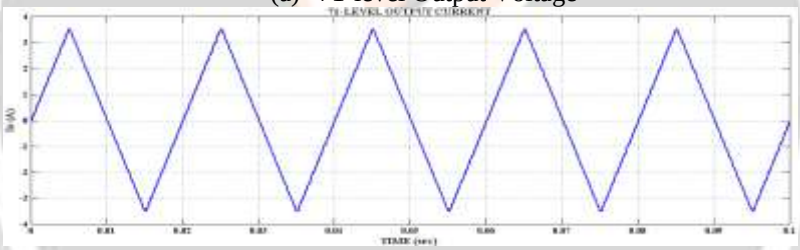


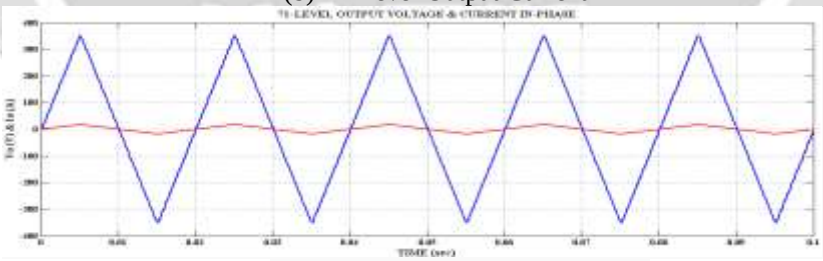
Fig.12 Matlab/Simulink Model of Proposed 71-level RSMLI Topology for Standalone R-Load System



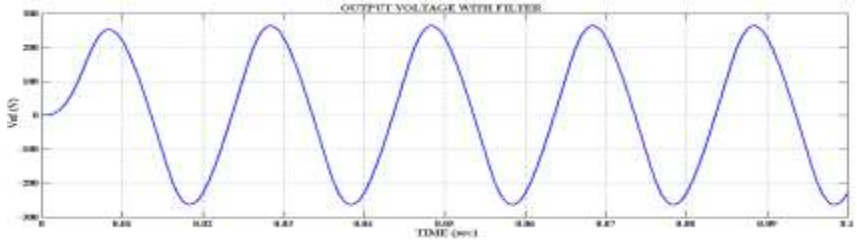
(a) 71-level Output Voltage



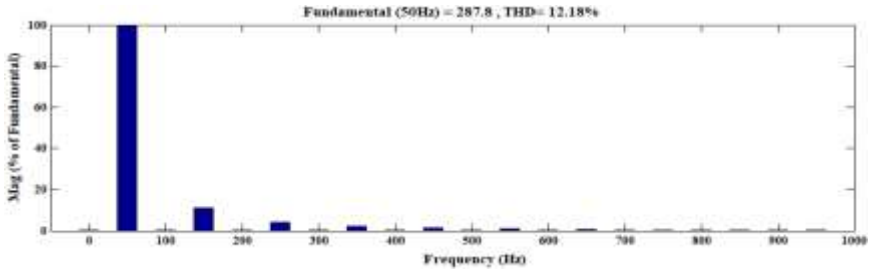
(b) 71-level Output Current



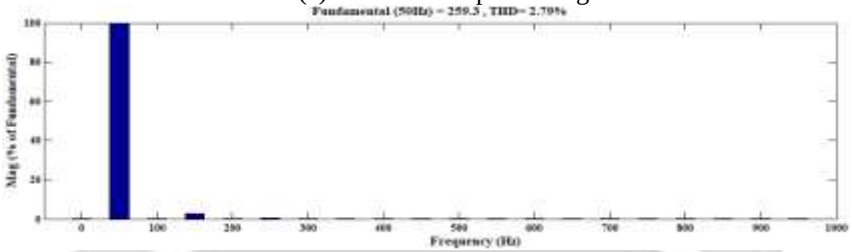
(c) Output Voltage & Current-In phase



(d) Output Voltage with Filter



(e) THD of Output Voltage



(f) THD of Output Voltage with Filter

Fig.13 Simulation Results of Proposed 71-level RSMLI Topology for Standalone R-Load System

The Matlab/Simulink Model of Proposed 71-level RSMLI Topology for Standalone R-Load System is depicted in Fig.12. Simulation Results of Proposed 71-level RSMLI Topology for Standalone R-Load System is depicted in Fig.13. It Includes, (a) 71-level Output Voltage, (b) 71-level Output Current, (c) Output Voltage & Current-In phase, (d) Output Voltage with Filter, (e) THD of Output Voltage, (f) THD of Output Voltage with Filter, respectively. The output voltage and current for a proposed cascaded 71-level RSMLI driven pure R-load having a load value of 100**Ω**, the output voltage is measured with a value of 350V and output current is measured with a value of 3.5A. For a pure R-load, the output current is in-phase with the output voltage represents the unity power-factor. The output voltage with filter carries a sinusoidal voltage with a value of 280V, the THD value of 71-level output voltage is 12.18% and the THD value of 71-level output voltage with filter is 2.79%, it is well within IEEE-519 standards.

5.4 DESIGN OF PROPOSED 71-LEVEL RSMLI TOPOLOGY FOR STANDALONE RL-LOAD SYSTEM

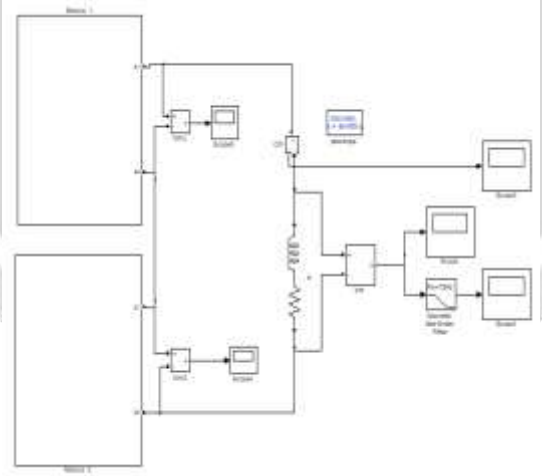
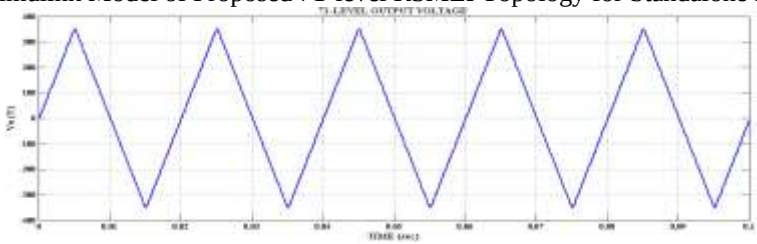
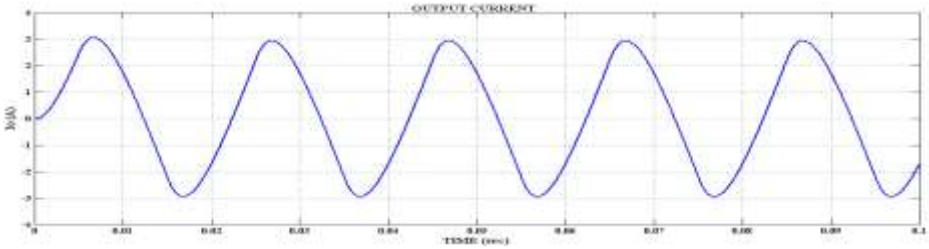


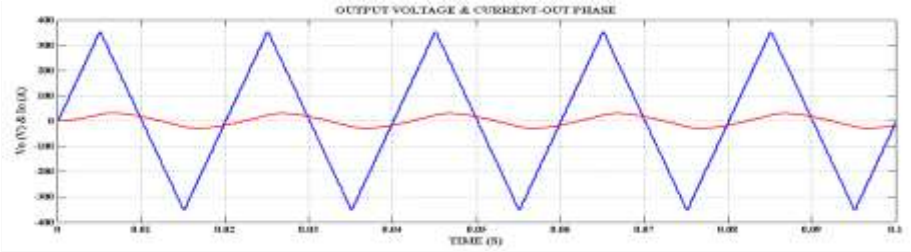
Fig.14 Matlab/Simulink Model of Proposed 71-level RSMLI Topology for Standalone RL-Load System



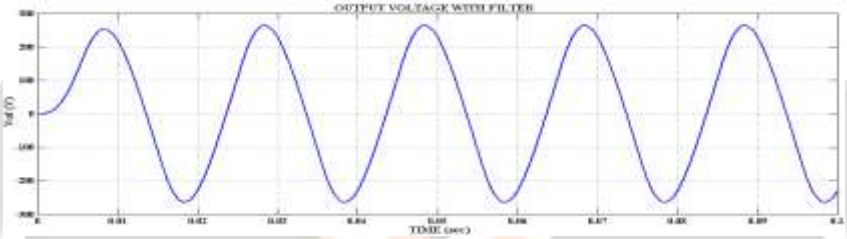
(a) 71-level Output Voltage



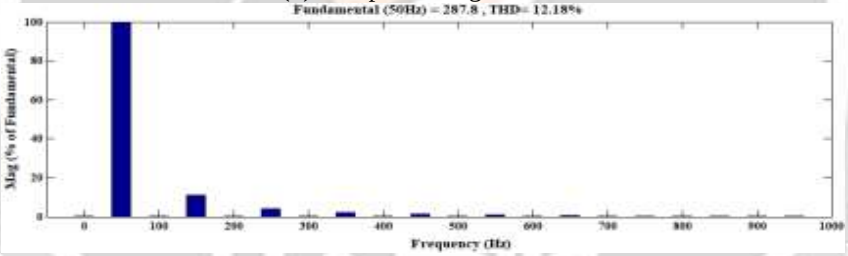
(b) Output Current



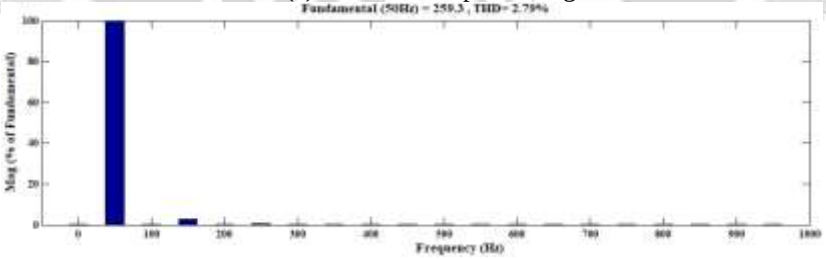
(c) Output Voltage & Current-Out of phase



(d) Output Voltage with Filter



(e) THD of Output Voltage



(f) THD of Output Voltage with Filter

Fig.15 Simulation Results of Proposed 71-level RSMLI Topology for Standalone RL-Load System

The Matlab/Simulink Model of Proposed 71-level RSMLI Topology for Standalone RL-Load System is depicted in Fig.14. Simulation Results of Proposed 71-level RSMLI Topology for Standalone RL-Load System is depicted in Fig.15. It Includes, (a) 71-level Output Voltage, (b) 71-level Output Current, (c) Output Voltage & Current-Out of phase, (d) Output Voltage with Filter, (e) THD of Output Voltage, (f) THD of Output Voltage with Filter, respectively. The output voltage and current for proposed cascaded 71-level RSMLI driven pure RL-load having a load value of 80Ω and 200mH the output voltage is measured with a value of 350V and output current is measured with a value of 3.5A. For a RL-load, the output current is out of phase with the output voltage represents the non-unity power-factor. The output voltage with filter carries a sinusoidal voltage with a value of 280V, the

THD value of 11-level output voltage is 12.18% and the THD value of 11-level output voltage with filter is 2.79%, it is well within IEEE-519 standards.

5.5 DESIGN OF PROPOSED 71-LEVEL RSMLI TOPOLOGY FOR SOLAR-PV INTEGRATED MICRO-GRID SYSTEM

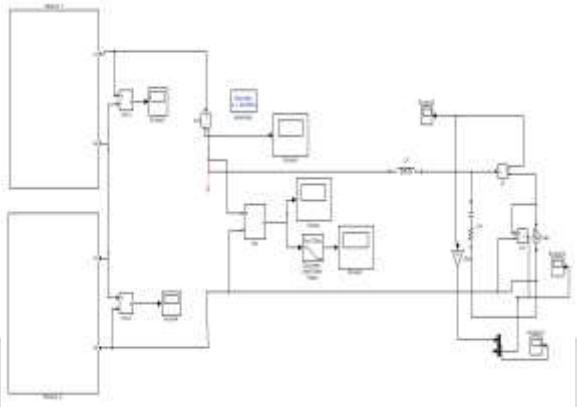
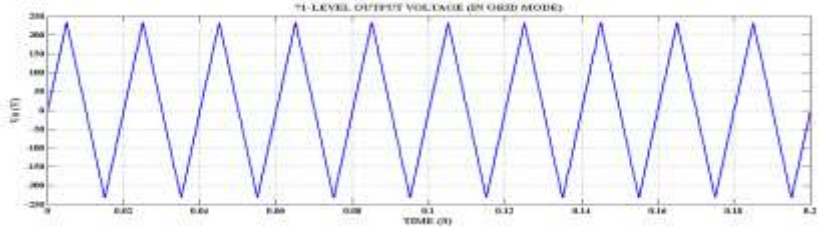
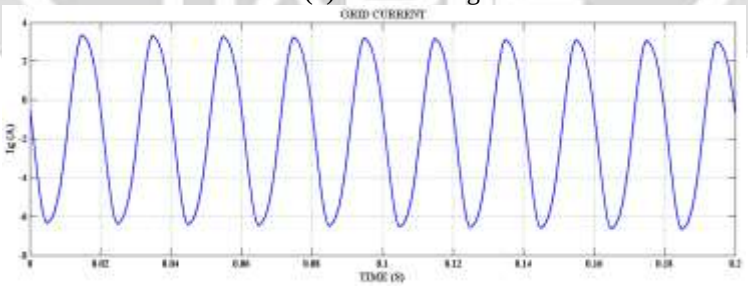


Fig.16 Matlab/Simulink Model of Proposed 71-level RSMLI Topology for Solar-PV Integrated Micro-Grid System

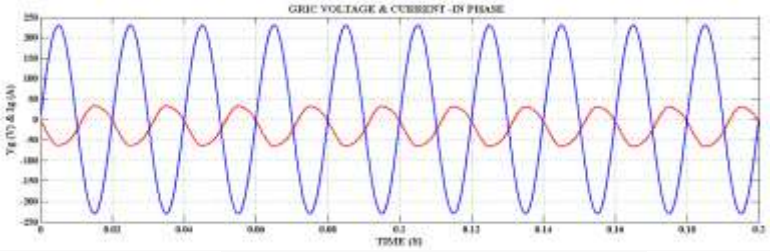


(a) 71-level Output Voltage

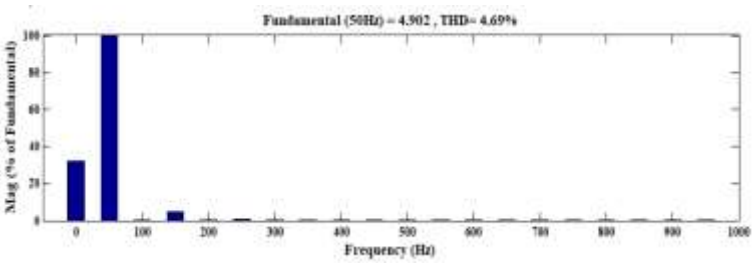
(b) Grid Voltage



(c) Grid Current



(d) Output Voltage & Current-Out of phase



(e) THD of Grid Current

Fig.17 Simulation Results of Proposed 71-level RSMLI Topology for Solar-PV Integrated Micro-Grid System

The Matlab/Simulink Model of Proposed 71-level RSMLI Topology for Solar-PV Integrated Micro-Grid System is depicted in Fig.16. Simulation Results of Proposed 71-level RSMLI Topology for Solar-PV Integrated Micro-Grid System is depicted in Fig.17. It Includes, (a) 71-level Output Voltage, (b) Grid Voltage, (c) Grid Current (c) Grid Voltage & Current-In phase, (d) THD of Grid Current, respectively. The output voltage of proposed 71-level RSMLI driven solar-PV integrated micro-grid system and the output/grid voltage is measured with a value of 230V and grid current is measured with a value of 3.5A. In grid mode, the output current is in-phase with the output voltage represents the unity power-factor and the energy receiving the grid with a reverse polarity. The THD value of grid current is 4.69%, it is well within IEEE-519 standards.

6. CONCLUSIONS

A new basic 11-level sub-module cascaded multilevel inverter topology has been proposed for standalone & micro-grid system with the advantage of having a reduced number of switching devices as well as number of dc voltage sources. The basic unit of the proposed topology generates 11 levels across the load employing eight switches with three dc voltage sources. To achieve more number of levels at the output, a detailed cascade connection of the proposed topology has been discussed. In a cascade connection, an appropriate voltage selection is carried based on requirement. Furthermore, based on merits of proposed 71-level RSMLI is integrated to micro-grid system by using solar-PV arrays. An in-depth comparison with traditional MLI topologies confirms the benefit of the proposed topology.

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