A SIMPLIFIED DESIGN OF RENEWABLE ENERGY BASED SWITCHED CAPACITOR CASCADED MULTI-LEVEL INVERTER

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ABSTRACT

In this project a cascaded multilevel inverter based on switched-capacitor for single phase Induction motor drive has proposed. The proposed topology is mainly focused on low number of switches for drive applications. A novel switched-capacitor cascaded multilevel inverter is proposed in this paper, which is designed by a switched-capacitor frontend and H-Bridge backend. Through the conversion of series and parallel connections, the switched capacitor frontend increases the number of voltage levels. The output harmonics and the component counter can be significantly mitigated by increasing number of voltage levels. However, it is difficult to obtain a high-frequency inverter with both simple circuit topology and straightforward modulation strategy. A novel switched-capacitor cascaded multilevel inverter is proposed in this paper, which is designed by a switched-capacitor frontend and H-Bridge backend. Through the conversion of series and parallel connections, the switched capacitor frontend increases the number of voltage levels. The output harmonics and the component counter can be significantly mitigated by increasing number of voltage levels. *A Solar PV has used as input to the proposed system which then converted to AC to feed IM. A new control strategy has proposed based on Multi-carrier PWM technique to control inverter switches. To analyze the proposed system is designed using MATLAB software. The Performance is analyzed interms of THD, line and phase voltages, speed and torque of the machine.*

Keyword: - *Cascaded Multilevel Inverter, Switched capacitor, THD, Solar PV*

1. INTRODUCTION

Multilevel inverter is an effective solution to increase power capacity without synchronization consideration, so the higher power capacity can be easily achieved by multilevel inverter with reduced switch stress. Non polluted sinusoidal waveform with the lower Total Harmonic Distortion is critically caused by long track distribution in HFAC PDS. The higher number of voltage levels can effectively decrease total harmonics content of staircase output, thus significantly simplifying the filter design. HF power distribution is applicable for small-scale and internal closed electrical network in Electric vehicle due to moderate size of distribution network and effective weight reduction. The consideration of operation frequency has to make compromise between the ac inductance and resistance, so multilevel inverter with the output frequency of about 20 kHz is a feasible trial to serve as power source for HF EV application. Since the input inductor of the boost converter operates in DCM, a high-frequency filter composed by an inductor *Lf* and capacitor *Cf* must be used in the preregulator input in order to reduce the input current ripple, as presented in Fig. 1.3 However, a problem presented by the boost preregulator operating in DCM is the input current distortion, presenting a third-harmonic component.

The conventional topologies of multilevel inverter fundamentally are diode-clasped and capacitor-cinched sort. The former utilizes diodes to clasp the voltage level, and the recent uses extra capacitors to clip the voltage. The higher number of voltage levels can then be acquired; on the other hand, the circuit be-comes to a great degree intricate in these two topologies. An alternate sort of multilevel inverter is fell H-Bridge built by the arrangement association of H-Bridges. The fundamental circuit is like the established H-span DC–DC converter. The fell structure expands the framework dependability due to the same circuit cell, control structure and balance. How-ever, the disservices went up against by fell structure are more switches and various inputs. With a specific end goal to expand two voltage

levels in staircase yield, a H-Bridge built by four force switches and an individual info are required. Theoretically, fell H-Bridge can get staircase yield with any number of voltage levels, yet it is improper to the applications of expense sparing and information confinement.

Various studies have been performed to expand the quantity of voltage levels. An super capacitor (SC) based multilevel circuit can adequately expand the quantity of voltage levels. Notwithstanding, the control methodology is perplexing, and EMI issue gets to be more regrettable because of the intermittent data current. A solitary stage five-level pulse width-tweaked (PWM) inverter is constituted by a full scaffold of diodes, two capacitors and a switch. Be that as it may, it just furnishes yield with five voltage levels, and higher number of voltage levels is restricted by circuit structure. A SC-based fell inverter was given SC frontend and full extension backend. Notwithstanding, both entangled control and expanded parts utmost its application . The further study was introduced utilizing arrangement/parallel transformation of SC. Then again, it is improper to the applications with HF out-put due to multicarrier PWM (MPWM). On the off chance that yield recurrence is around 20 kHz; the bearer recurrence achieves a few megahertz. To be specific, the transporter recurrence in MPWM is handfuls times of the yield recurrence. Since the bearer frequency decides the exchanging recurrence, a high exchanging misfortune is certain for the purpose of high-recurrence yield. A help multilevel inverter situated in fractional charging of SC can expand the quantity of voltage levels hypothetically. In any case, the control system is muddled to actualize incomplete charging. Along these lines, it is a testing errand to present a SC-based multi-level inverter with high-recurrence yield, low-yield harmonics, and high transformation productivity. Taking into account the study circumstance previously stated, a novel multi-level inverter and straightforward tweak methodology are displayed to serve as HF force source. Whatever is left of this paper is sorted out as takes after.

2. PROPOSED SYSTEM

2.1 circuit topology

The circuit topology of nine-level inverter (N1 =2, N2 = 2), where S1, S2, S1 1, S2 1 as the switching devices of SC circuits (SC1 and SC2) are used to convert the series or parallel connection of C1 and C2 is shown in fig 1. S1a, S1b, S1c, S1d, S2a, S2b, S2c, S2d are the switching devices of cascaded H-Bridge. Vdc1 and Vdc2 are input voltage. D1 and D2 are diode to restrict the current direction. I_{out} and v_o are the output current and the output voltage, respectively.

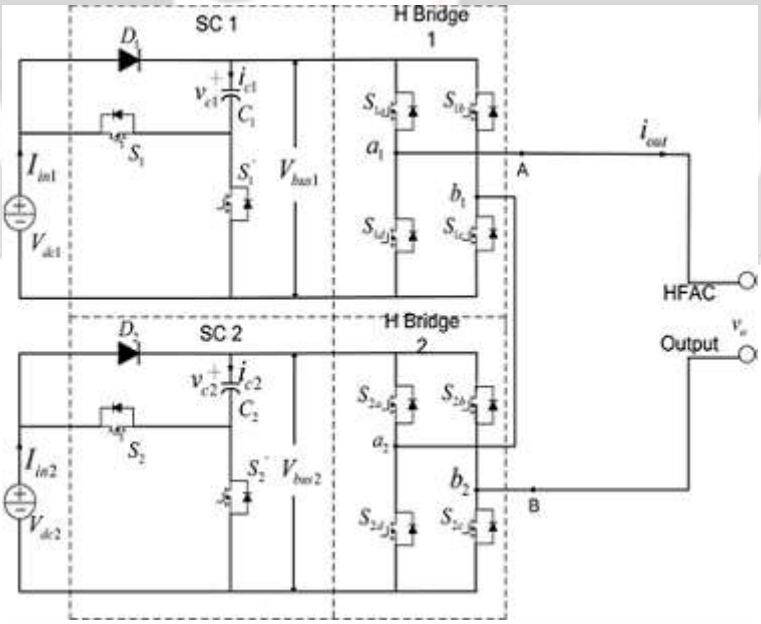


Fig-1: Proposed circuit Topology

The proposed circuit is comprised of the SC frontend and fell H-Bridge backend. In the event that the quantities of voltage levels acquired by SC frontend and fell H-Bridge backend are N1 and N2 , individually, the quantity of voltage levels is 2 × N1 ×N2 +1 in the whole operation cycle.

2.2 Symmetrical Modulation

There are numerous regulation routines to control the multilevel inverter, the prominent balances are the space vector tweak, the multicarrier PWM, and the particular symphonious disposal, sub harmonic pulse width modulation, and so forth. Notwithstanding, the greater part of them incredibly expand the bearer recurrence that is handfuls times the recurrence of yield. A symmetrical stage shift tweak (PSM) is brought into the proposed multilevel inverter. The sym-metrical PSM guarantees the yield voltage of full scaffold is sym-metrical to the transporter, so voltage levels can be superimposed symmetrically and bearer recurrence is twice as that of the out-put recurrence . The structure of symmetrical PSM is demonstrated in Fig. 2(a), and the operational waveform of symmetrical PSM is demonstrated in Fig. 2(b).

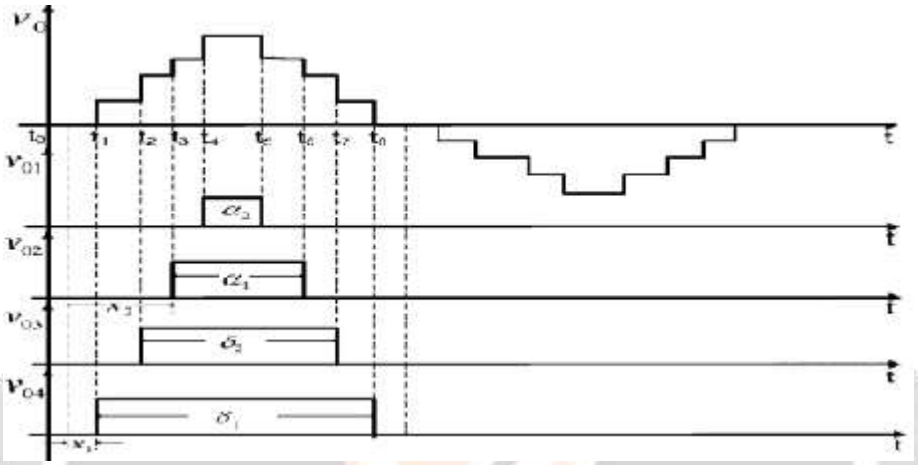


Fig-2: Output voltage decomposition for mode 1.

The logic operations of gate signals are

gate1 = *XOR{Q(RS), Q(D)}*

gate2 = *XOR{Q(RS),Q(D)}*

gate3 = *XOR{AND{Q(RS),NOT(PWM)},Q(D)}*

gate4 = *XOR{AND{Q(RS),NOT(PWM)}, Q(D)}*

A controlled PWM with pulse width δ is symmetrically generated by the comparisons of the triangle carrier V_c and modulation. Signal V_m . The rising edge matching of V_c and V_m triggers the polarity inversion of the leading bridge, while the falling edge matching of V_c and V_m triggers the polarity inversion of the lagging bridge. When V_m has a change V_m , this modulation simultaneously moves gate1 and gate3 in the opposite direction. Thus, the derived V_{ab} is symmetrical with respect to V_c .

2.3. Operation Cycles:

Fig. 3 shows the perfect waveforms of proposed inverter. Vc is the triangular transporter, and Vpp is the crest estimation of Vc . The regulation signs of triangular bearer are Vm 1c , Vm 1b , Vm 2c and Vm 2b . Vm 1b and Vm 2b are utilized to control stage movement edges of H-Bridge 1 and H-Bridge 2, individually, and δi is the span of voltage levels controlled by them. Vm 1c and are utilized to control the option operations of SC1, and SC2, separately, and αi is the length of time of voltage levels controlled by them. Therefore, the drive signs of H-Bridge switches (S1a , S1b , S1c , S1d , S2a , S2b , S2c , S2d) are stage moved heartbeat signs, while the drive signs of SC switches (S1 , S2 , S1_ , S2_) are reciprocal heartbeat signals. Two operational modes are introduced as demonstrated in Fig. Mode 1 is like mode 2 separated from the distinctive positions of tweak signs (Vm 1c , Vm 1b , Vm 2c , Vm 2b). Therefore, the spans of every voltage level are controlled by regulation flags in both mode 1 and mode 2.

Dynamic circuits of the operational mode 1 are shown in Fig. 4. Re is the equal burden. At the point when t fulfills t0 ≤ t < t1 in Fig. 3(a), the switches S1a , S1b , S2a , S2b are determined by the entryway source voltage, individually. H-Bridges 1 and 2 are in freewheeling state, and yield voltage meets 0. The voltages on Bus 1 and Bus 2 are Vin also. The current stream of this time interim is indicated in Fig. 4(a). At the point when t fulfills t1 ≤ t < t2

in Fig. 3(a), the switches S1a , S1b , S2a , S2c are determined by the entryway source voltage, respectively. H-Bridge 1 is in freewheeling state, and H-Bridge 2 is in positive leading state. Yield voltage approaches Vin . The voltages on Bus 1 and Bus 2 are Vin also. The current stream of this time interim is demonstrated in Fig. 4(b). At the point when t fulfills t2 ≤ t < t3 in Fig. 3(a), the switches S1a , S1c , S2a , S2c are determined by the door source voltage, respectively. H-Bridges 1 and 2 are in positive directing state. Yield voltage parallels 2Vin . The volt-ages on Bus 1 and Bus 2 are Vin also. The current stream of this time interim is indicated in Fig. 4(c). At the point when t fulfills t3 ≤ t < t4 in Fig. 3(a), the switches S1a , S1c, S2a, S2c are determined by the door source voltage, respectively. H-Bridges 1 and 2 are in positive directing state. Yield voltage parallels 3Vin . Since S_1 [1] and S_2 [1] are on, the capacitor C1 keeps charged to Vin (Vdc 1 = Vdc 2 = Vin), and the capacitor C2 is released. The voltages on Bus 1 and Bus 2 are Vin and 2Vin , individually. The current stream of this time interim is indicated in time.

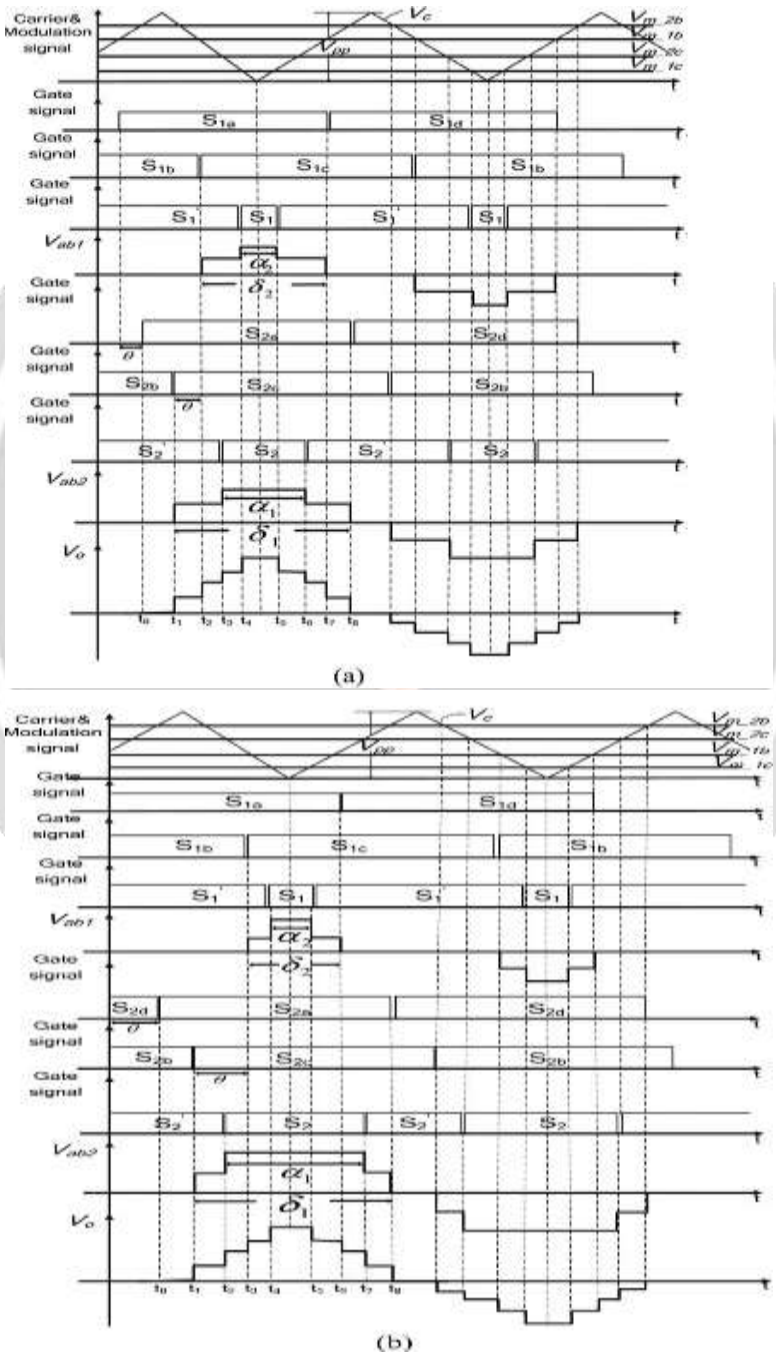


Fig-3: Operational waveforms of the proposed multilevel inverter. (a) Operational mode 1. (b) Operational mode 2

When t satisfies $t_4 \leq t < t_5$ in Fig. 3(a), the switches S_{1a} , S_{1c} , S_{2a} , S_{2c} are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in positive conducting state. Output voltage equals $4V_{\text{in}}$. Because S_1 and S_2 are on, the capacitor C_1 and C_2 are discharged. The voltages on Bus 1 and Bus 2 both are $2V_{\text{in}}$. The current flow of this time interval is shown in Fig. 4(e).

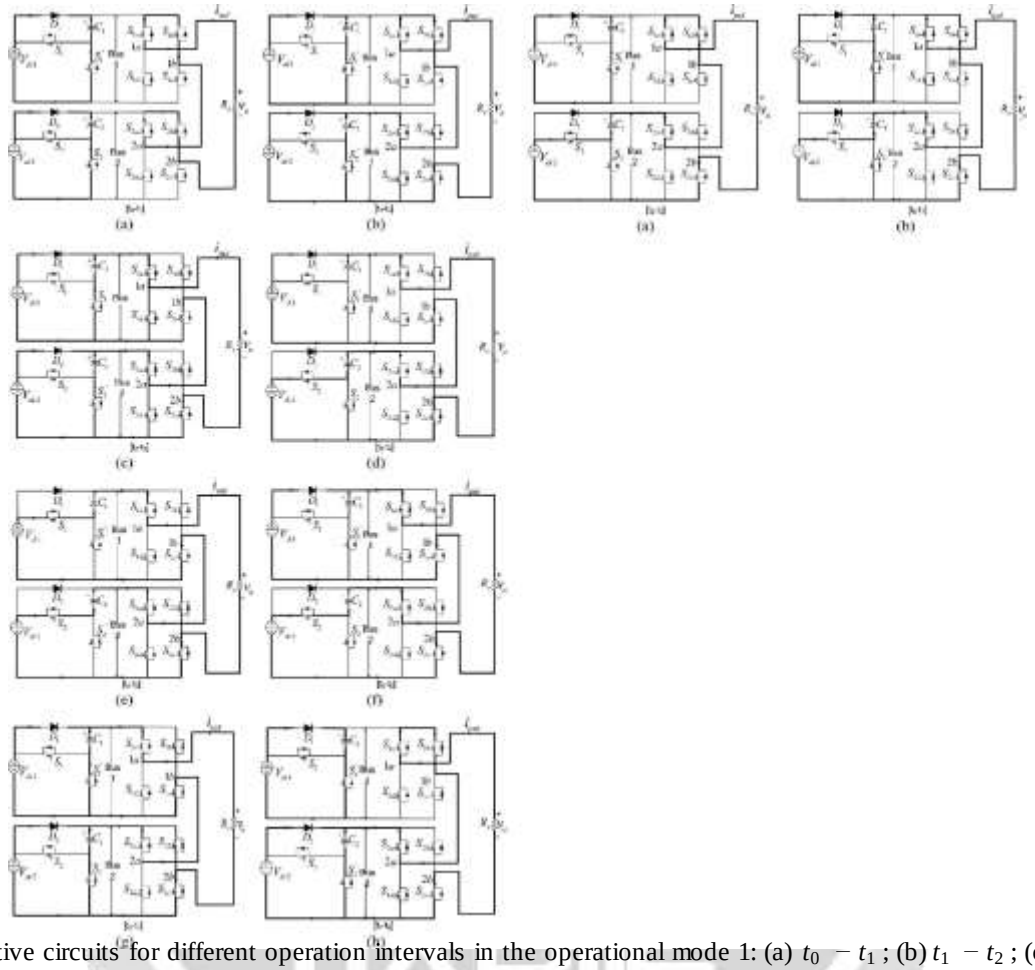


Fig-4: Active circuits for different operation intervals in the operational mode 1: (a) $t_0 - t_1$; (b) $t_1 - t_2$; (c) $t_2 - t_3$; (d) $t_3 - t_4$; (e) $t_4 - t_5$; (f) $t_5 - t_6$; (g) $t_6 - t_7$; (h) $t_7 - t_8$.

The operations in $t_5 \leq t < t_6$, $t_6 \leq t < t_7$, and $t_7 \leq t < t_8$, are the same as the operations in $t_3 \leq t < t_4$, $t_2 \leq t < t_3$, and $t_1 \leq tt_2$, respectively. The dynamic circuits are demonstrated in Fig. 4(f)–(h). Contrasting and operational mode 1, the mode 2 has the diverse dynamic circuits in two time interims. At the point when t fulfills t2 ≤ t < t3 in operational mode 2 as indicated in Fig. 3(b), the switches S1a , S1b , S2a , S2c are determined by the entryway source voltage, respectively. H-Bridge 1 is in freewheeling state, and H-Bridge 2 is in positive directing state. Yield voltage approaches 2Vin . Since S1_ and S2 are on, the capacitor C1 keeps charged to Vin and capacitor C2 is released. The voltages on Bus 1 and Bus 2 are Vin and 2Vin , separately. The current stream of this time interim is demonstrated in Fig. 5(a). Essentially, the dynamic circuit of t6 ≤ t < t7 is indicated in Fig.

The second half-cycle (from t8 on) has the comparative dynamic circuits as the first half-cycle (t1 − t8), however the current will be circled in the other way to give the negative yield voltage. The relations of on-state switches and yield voltage level are depicted in Table I, and operations of two modes are looked at nearly. At the point when the operation enters another state from a nearby state, stand out force switch changes in the middle of on and off. The gadget push in exchanging gadgets of H-scaffold circuit is higher than that in SC circuit. It can likewise be discovered that the yield voltage in Mode 1 is more steady than Mode 2 because of less releasing time of exchanging capacitor.

Alongside the up-down development of regulation signs (Vm 1c , Vm 1b , Vm 2c , Vm 2b), the yield voltage of the expert postured inverter is a controllable nine-level staircase. The duration of every voltage level is dictated by the obligation cycle of SC circuit and the stage moved point of H-Bridge circuit.

4 SIMULATION RESULTS

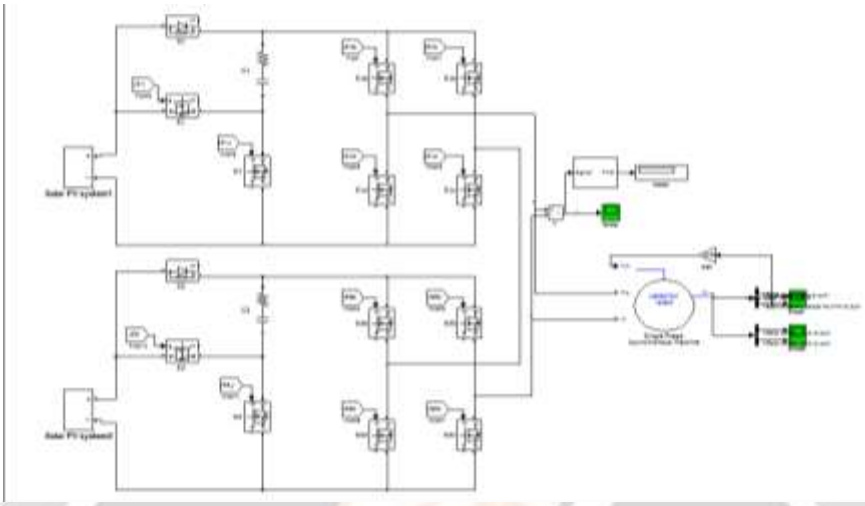


Fig-5: Simulation diagram of the proposed system

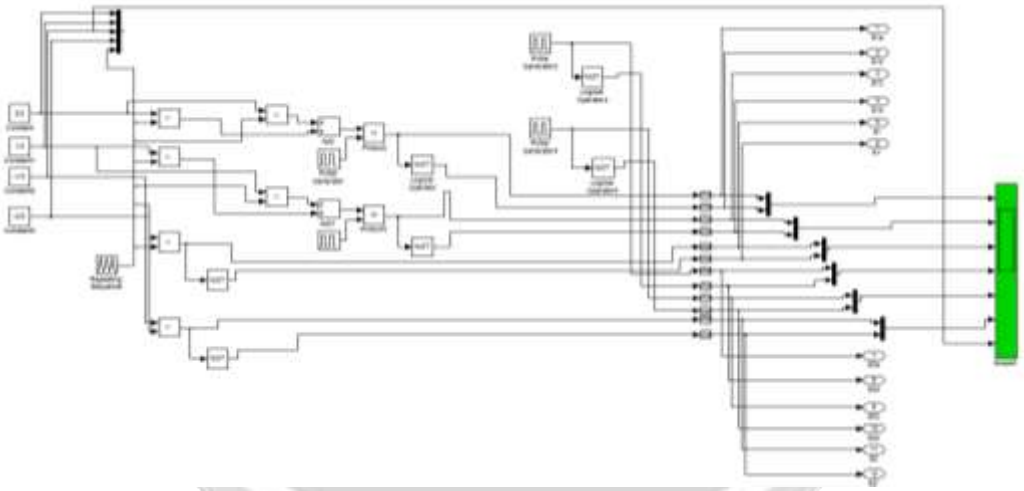


Fig-6: Proposed control strategy of pulse width modulation

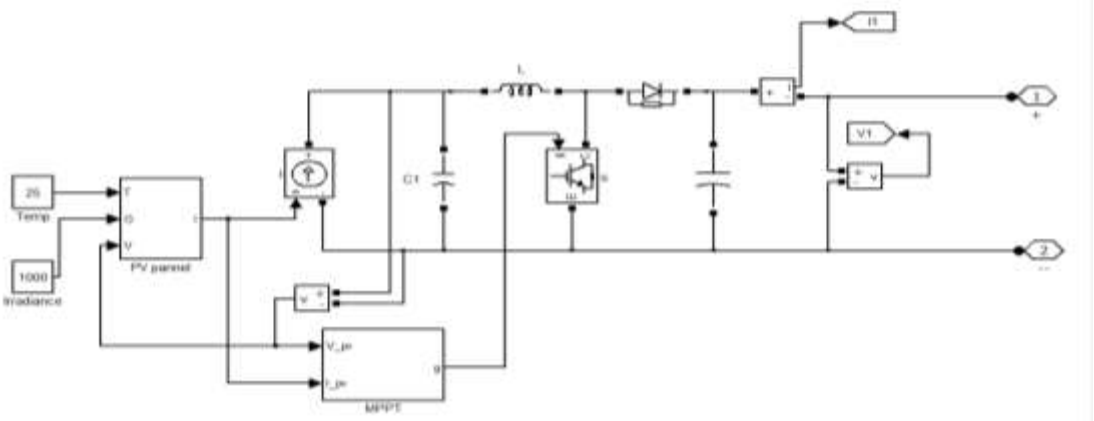


Fig-7: solar PV with MPPT control

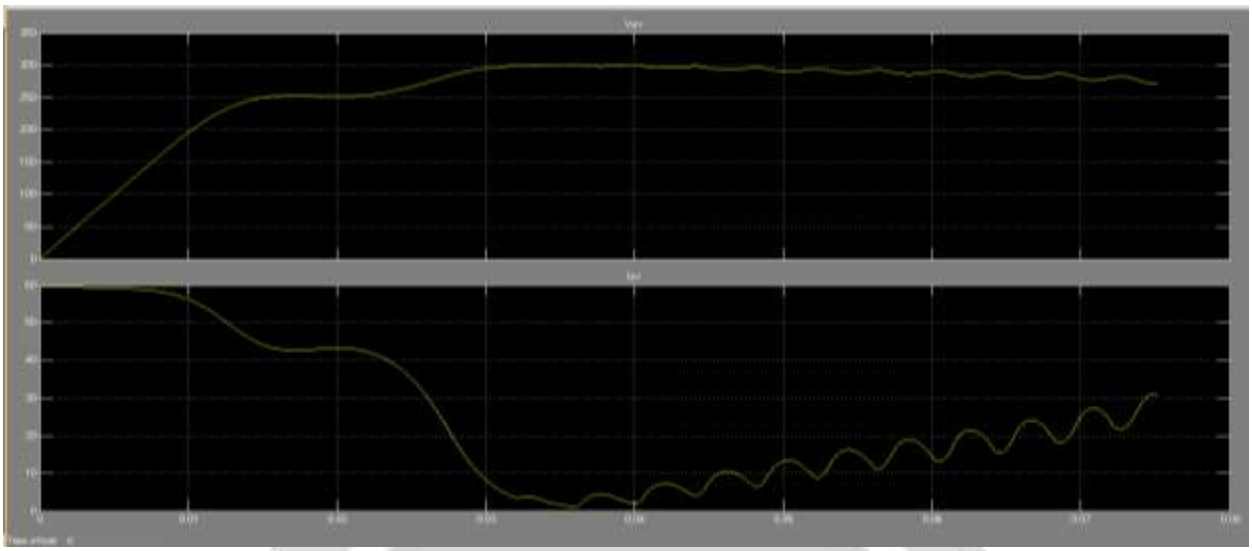


Fig-11: Vpv and Ipv of solar waveform

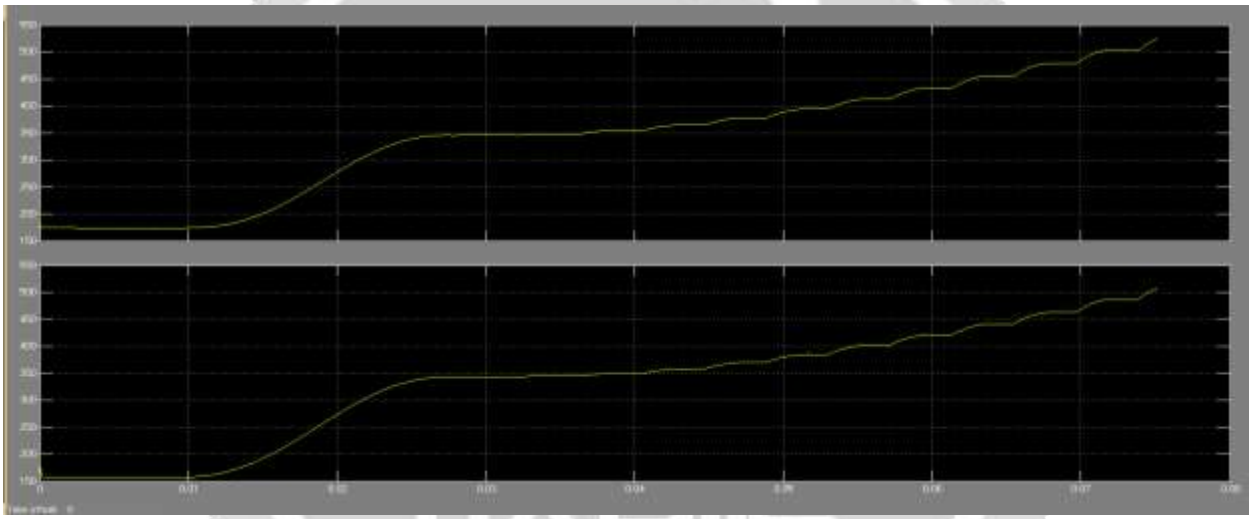


Fig-12: Boosted voltage after boost converter

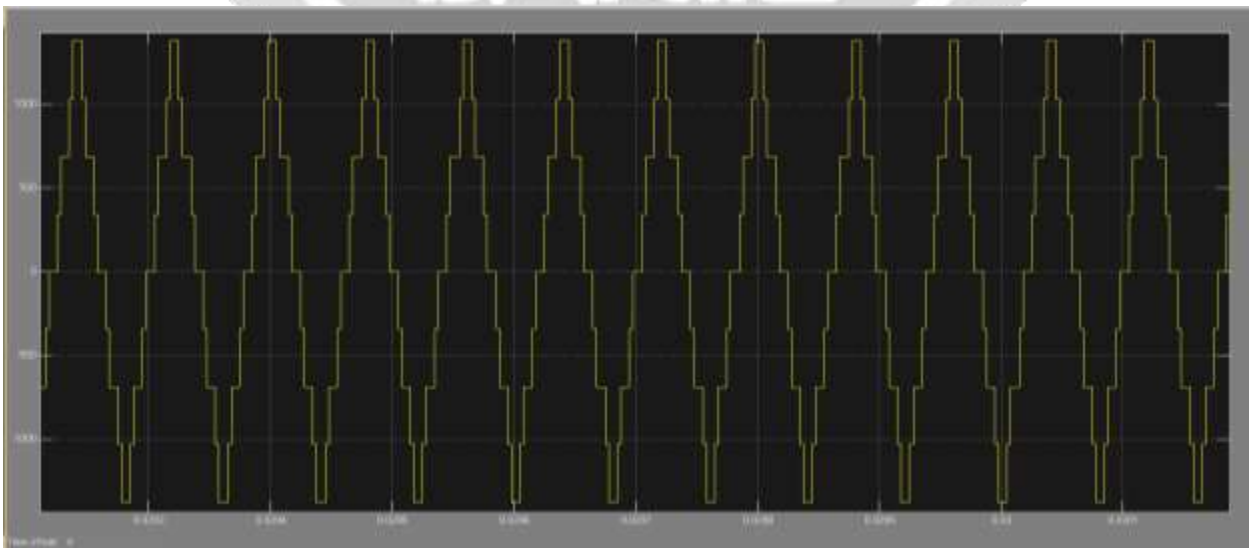


Fig-13: Nine –leveloutput of Proposed multi-level Inverter

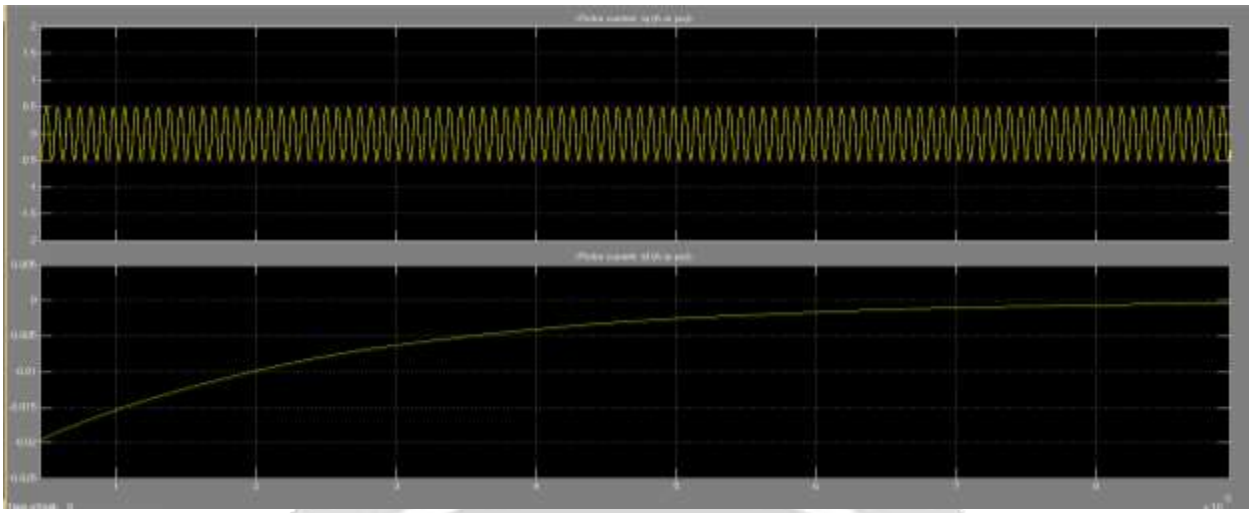
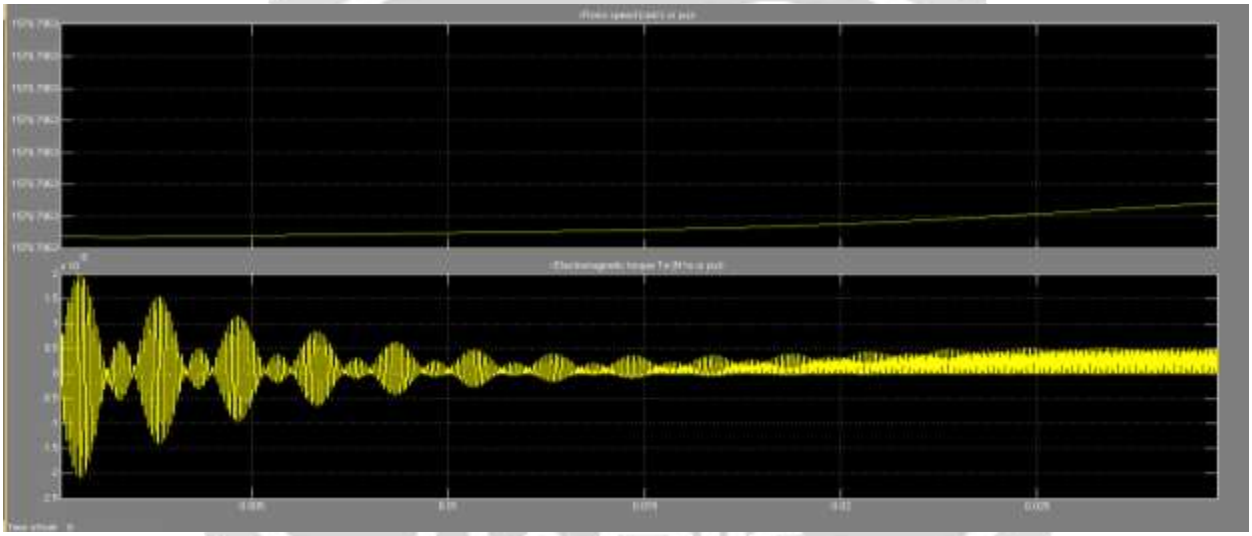


Fig-14: single phase IM machine rotor Id and Iq



.Fig-15: Speed and torque of the machine

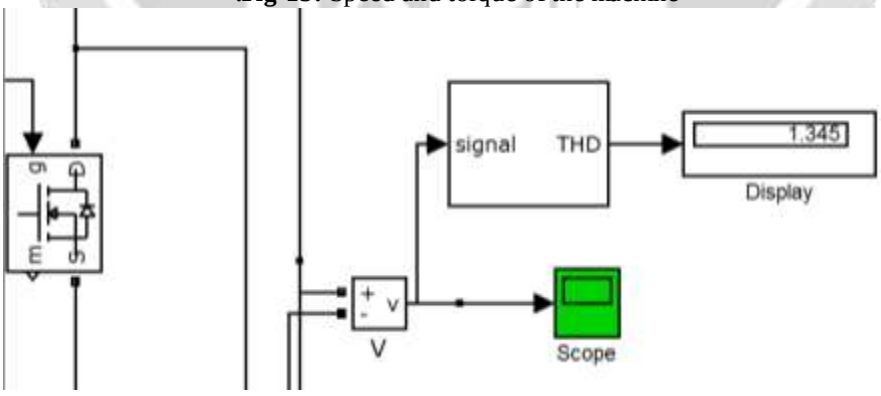


Fig-16: Total Harmonic Disrtion of the output voltage

5. CONCLUSIONS

In this paper, a SC-based cascaded multilevel inverter with nine-level circuit topology is examined in depth. Compared with conventional cascaded multilevel inverter, the proposed inverter can greatly decrease the number of switching devices. A single carrier modulation named by symmetrical PSM, was presented with the low switching frequency and simple implementation. The result of simulation gives the feasibility of proposed circuit and

modulation method. Comparing with traditional cascade H-bridge, the number of voltage levels can be further increased by SC frontend. The number of voltage levels increases twice in half cycle of 9-level circuit. With the exponential increase in the number of voltage levels, the harmonics are significantly cut down in staircase output, which is particularly remarkable due to simple and flexible circuit topology. Meanwhile, the magnitude control can be accomplished by pulse width regulation of voltage level, so the proposed multilevel inverter can serve as HF power source with controlled magnitude and reduced harmonics. The proposed inverter can be applied to grid-connected photovoltaic system and electrical network of Electric vehicles, because the multiple dc sources are available easily from solar panel, batteries, Ultra capacitors, and fuel cells.

6. REFERENCES

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