An Efficient Multilevel Inverter with Reduced Switches Using Series Connection of Sub Multilevel Inverter

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ABSTRACT

Multilevel inverter as compared to single level inverters have advantages like minimum harmonic distortion, reduced Electro Magnetic Interference (EMI/RFI) generation and can operate on several voltage levels. In this paper a new topology of cascaded multilevel inverter using reduced number of switches, resulting in higher output voltage levels is proposed. According to the basic topology, a new structure for sub-multilevel inverter is suggested. In continue, cascaded multilevel inverter is realized based on the series connection of n sub-multilevel inverters. By calculating the blocking voltage across the switches, the modulation technique is described for the proposed Structure. Work on simulation part using Matlab Simulink and also work on hardware part using power electronics. Also consider other parameters like energy efficiency, Power consumption, response time etc.

Keywords :- *Power Electronics, Multilevel Inverter*

1. INTRODUCTION:

Multilevel inverters due to many advantages such as high quality output waveform, reducing lower order harmonics, lower switching losses and better electromagnetic interference are used in different applications. The conventional topologies are divided into three main groups: the neutral point clamped (NPC) multilevel inverter, flying capacitor (FC) multilevel inverter and cascaded H-bridge (CHB) multilevel inverter. Among the multilevel inverter topologies, the cascaded multilevel inverters have attracted more attention mainly because of simple structure and easily of extending to higher voltage levels. Cascaded multilevel inverters synthesize a desired voltage output based on a series connection of power cells. In recent years, researchers have presented many various apologies of multilevel inverters for different purposes Most of the presented topologies try to reduce the number of components. One of these topologies is the modular multilevel inverter. This topology is simpler than the cascaded four-switch H-bridge-based inverter and has several advantages. However, the topology does not consider reduction in the number of components. The multilevel inverter presented in is based on symmetric topology and uses series/parallel connection of the dc voltage sources. This topology uses lower number of switches in comparison with the symmetric CHB. The topologies presented in and consider reduction in the components. These topologies are basically based on asymmetric topologies; hence, the used dc voltage sources have different values. However, the number of switching devices still remains high in these topologies. In this paper, first a new topology for basic unit for multilevel inverter is proposed which utilizes lower number of power switches and dc voltage sources. Then, series connection of the basic units is proposed as a generalized multilevel inverter. It is aimed to increase the number of output voltage levels and reduce the number of power switches, driver circuits and total cost of the inverter. In order to generate all positive and negative levels at the output, a new algorithm to determine the magnitudes of dc voltage sources are proposed. The proposed inverter is compared with several conventional cascaded multilevel inverters to investigate its advantages. Finally, the accuracy performance of the proposed inverter is reconfirmed by using simulation results on 33-level proposed inverter.

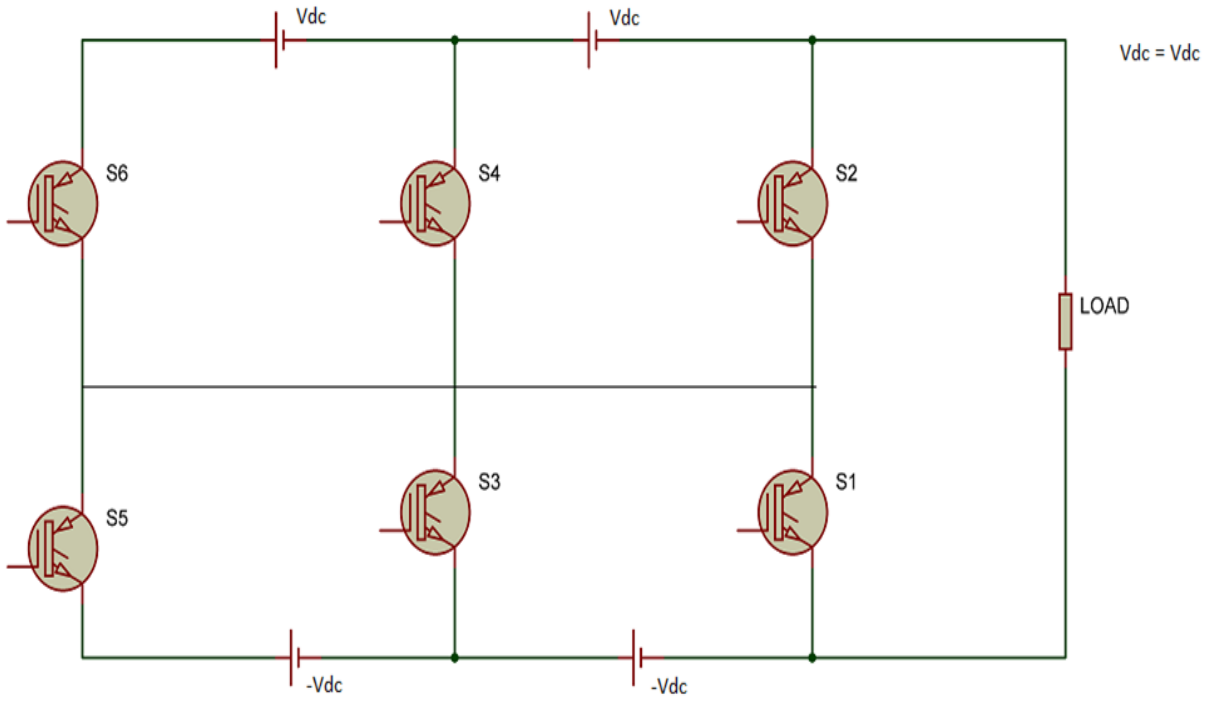

Fig. 1 Proposed Multilevel Inverter

2. LITERATURE REVIEW:

2.1 Two New Cascaded Multilevel Inverters with Less Number of Components by Using Series Sub multilevel Inverters

In [1] K.rahimi, A.salemnia, S.E.afjei. In this paper, two new cascaded inverters are proposed, by using the series connection of new Sub multilevel inverters. Each of the proposed Sub multilevel inverters consists of three batteries and eight power switches. Four algorithms are presented to determine the voltages of these batteries for each of the proposed structures. In this study the comparison between the proposed structures with conventional structures has been done. At first, the proposed algorithms of new structures are compared with each other and after that comparisons between proposed structures based on selected algorithms and the traditional structures are performed. This comparison shows that the proposed inverters can produce high number of output voltage levels due to determined number of power electronic switches. Also blocked voltage of the proposed structures is smaller than other compared structures which leads to reduce size and weight of the proposed inverters. Other advantages of these structures are reduction of s

2.2 An Efficient Topology for Multilevel Inverters: Design Specifications and Modulation Technique

In [2] Reza Choupan, Daryoush N azarpour, Sajjad Golshannavaz. This paper introduces an efficient and generalized basic topology adopted for multilevel inverters. It is shown that the proposed structure is in line with significant savings in part counts and control devices. According to the basic topology, a new structure for sub-multilevel inverter is suggested. In continue, cascaded multilevel inverter is realized based on the series connection of n sub-multilevel inverters. By calculating the blocking voltage across the switches, the modulation technique is described for the proposed structure. A comprehensive analysis is founded to compare the proposed cascaded structure with the conventional CHB topology and the recently archived structures.

2.3 A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit with Reduced Number of Power Switches.

In [3] Ebrahim Babaei, Sara Laali, Zahra Bayat. In this paper, a new single-phase cascaded multilevel inverter is proposed. This inverter is comprised of series connection of the proposed basic unit and is able to generate only positive levels at the output. Therefore, an H-bridge is added to the proposed inverter. This inverter is called developed cascaded multilevel inverter. In order to generate all voltage levels (even and odd) at the output of the developed topology, four different algorithms are proposed to determine the magnitude of dc voltage sources. Reduction in the number of power switches, driver circuits and dc voltage sources are advantages of the developed single-phase cascaded multilevel inverter. As a result, the installation space and cost of the inverter are reduced. These features are obtained by the comparison of the conventional cascaded multilevel inverters with the proposed cascaded topology. The ability of the proposed inverter in generation all voltage levels (even and odd) is reconfirmed by using the experimental results of a 15-level inverter.

2.4 A New Basic Unit for Cascaded Multilevel Inverters with Reduced Number of Power Electronic Devices.

In [4] Ebrahim Babaei, Mohammad Ali Hosseinzadeh, Maryam Sarbanzadeh, Carlo Cecati., In this paper, a new topology for asymmetrical cascaded multilevel inverter is proposed. The proposed topology consists of series connection of several basic units. Reduction of number of power switches, driver circuits, IGBTs and dc voltage sources are some advantages of the proposed topology in comparison with the conventional cascaded multilevel inverters. In order to generate all output voltage levels, a new algorithm to determine the magnitudes of dc voltage sources is proposed.

2.5 A New Multilevel Inverter Topology with Reduced Device Count and Blocking Voltage.

In [5] Piyush L. Kamani, Mahmadasraf A. Mulla, In this paper, a novel twenty-one level inverter unit is proposed. Using this, the cascaded multilevel inverter topology is suggested to achieve the higher number of output levels. The cascaded topology is constructed by the series connection of the twenty-one level basic unit. The topology is created in such a way that more levels can be added without modifying the existing circuit. The proposed topology offers advantages like reduced device count, reduced blocking voltage, and better dc source utilization compared to the conventional topologies. Various algorithms, To decide the rating of dc voltage sources, are suggested with its comparison.

2.6 A Novel Family of Three Phase Transistor Clamped H-Bridge Multilevel Inverter with Improved Energy Efficiency.

In [6] N. B. Deshmukh, R. D. Thombare, M. M. Waware, Multilevel inverter (MLI) is a proven technology used for control of electrical machines, grid integration of renewables and active power filtering. The recent trends show ingenious attempts to achieve maximum number of output voltage levels with minimum number of active device count and active device rating. This paper proposes a novel family of H Bridge MLI with transistor clamp to increase number of output levels. The proposed topology can be easily extended to any number of voltage levels facilitating significant reduction in number of circuit components, especially active switches, and thereby improving reliability of the system. The H bridge structure enables proposed topology to achieve operation at higher voltage (HV) and higher power level without increasing the device rating. The proposed topology is modified to operate at even higher voltage levels using unique series connection of unidirectional switches. This topology is controlled by carrier based Pulse Width Modulation (CBPWM) which is easy to understand, implement and hence cost efficient. This study proposes modification in the CBPWM to reduce switching losses. At higher switching frequencies and thereby improving energy efficiency of the system. Inverters can be classified by their output voltage waveform such as square wave, modified square wave, also called quasisquare wave.

3. COMPARATIVE TABLE:

Table -1: Comparative Table

Paper Title	Methods/Techniques	Advantages	Disadvantages
Two New Cascaded Multilevel Inverters with Less Number of Components by Using Series Sub multilevel Inverters	1An Efficient Cascaded Multilevel Inverter 2Less Number of Components	advantage of using tag patterns is we get an efficient multilevel inverter by using less components.so efficiency is increased.	the the quality gets reduced
An Efficient Topology for Multilevel Inverters: Design Specifications and Modulation Technique	an efficient and generalized basic topology adopted for multilevel inverters.	reducing the switching voltages across the switches. As well, the switching losses and electromagnetic interference are reduced.	Smaller in size against two level inverter.
A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit with Reduced Number of Power Switches.	1 Power Switches 2 Less Component Used	the installation space and cost of the inverter are reduced. These features are obtained by the comparison of the conventional cascaded multilevel inverters with the proposed cascaded topology.	
A New Basic Unit for Cascaded Multilevel Inverters with Reduced Number of Power Electronic Devices.	An Efficient Multilevel Inverter.	increases the Efficiency in terms of power electronics devices.	It is Costly when level is increased.
A New Multilevel Inverter Topology with Reduced Device Count and Blocking Voltage.	Reduce device count and blocking voltage.	improved harmonic profile and higher power handling competency	Costly

A Novel Family of Three Phase Transistor Clamped H-Bridge Multilevel Inverter with Improved Energy Efficiency	Novel family of 3 phase transistor.	improves the quality of multilevel inverter.	Harmonic Problem and Cost Effective.

4. CONCLUSION:

In this paper, a new asymmetric basic unit was proposed for cascaded multilevel inverters. The proposed multilevel inverter based on the basic unit is connected in series. Moreover, a new algorithm is proposed to determine the magnitude of dc voltage sources. The proposed cascaded multilevel inverter uses lower number of power electronic switches, IGBTs, power diode, driver circuit and dc voltage sources for a same number of voltage levels in comparison with the conventional multilevel inverters.

Established an efficient basic unit cell structure for multilevel inverters. Then, the proposed structure was extended to end in a sub-multilevel inverter granting a higher number of levels in the output voltage waveforms. It was shown that the cascaded connection of sub-multilevel inverters remarkably improves the operational indices required in real-world applications.

5. REFERENCES:

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