CLASSICAL DESIGN OF SOFT SWITCHED INTERLEAVED DC-DC CONVERTER FOR SUSTAINABLE ENERGY APPLICATIONS

P. Sangeetha[1], G. Ashok[2]

[1] Student, EEE Department, Jyothismathi Institute of technology & Science, Telangana, India
[2] Asst.Prof, EEE Department, Jyothismathi Institute of technology & Science, Telangana, India

ABSTRACT

In this project, the built-in transformer voltage multiplier cell is inserted into each phase of the conventional interleaved boost converter to provide additional control freedom for the voltage gain extension without extreme duty cycle. The voltage multiplier cell is only composed of the built-in transformer windings, diodes and small capacitors. And additional active switches are not required to simplify the circuit configuration. Furthermore, the switch voltage stress and the diode peak current are also minimized due to the built-in transformer voltage multiplier cells to improve the conversion efficiency. Moreover, there is no reverse-recovery problem for the clamp diodes and the reverse recovery current for the regenerative and output diodes are controlled by the leakage inductance of the built-in transformer to reduce the relative losses. In addition, the switch turn-off voltage spikes are suppressed effectively by the ingenious and inherent passive clamp scheme and zero current switch (ZCS) turn-on is realized for the switches, which can enhance the power device reliability. The presented converter is implemented in MATLAB SIMULINK and the results are presented.

Keyword: *- DC-DC Converter, soft switching, built-in transformer, PV system*

1. INTRODUCTION

Along with the declining production of the fossil fuels, the sustainable energy sources, such as the photovoltaic (PV), fuel cells, and wind energy are taken as the promising candidates for future energy supply [1], [2]. Furthermore, in order to absorb the random energy fluctuation generated by the sustainable energy sources, the back-up storage elements are required. Unfortunately, the output voltages of each PV panel and back-up battery cell are quite low, which calls for high step up and high-efficiency boost converters to lift the low voltage to a high one for the secondary grid-connected applications [3]–[5]. Generally speaking, the conventional interleaved boost converter is an excellent candidate for power factor correction (PFC) applications. However, when it is employed in the high step-up systems with nearly or over 10 times voltage gain, some insurmountable limitations are unavoidable. From its key waveforms in the high step-up conversion applications. It can be seen that the switch duty cycle is quite large and the turn-off period is extremely narrow. Consequently, the peak current on the power devices are relatively considerable and the diode reverse recovery problem is serious.

Although the three-level boost converters can double the voltage gain compared with the conventional boost converters, it cannot provide another control freedom for the voltage gain extension [6], [7]. Furthermore, the switched capacitor based converters can also achieve the large voltage gain conversion. However, they should suffer large transient current due to the switched capacitor technique, which shortens the usage life of the switched capacitors [8]–[9]. The turns ratio of the coupled inductors can be employed to provide another control freedom to lift the output voltage without extreme duty cycle and reduce the switch voltage stress. And many coupled inductor based converters are introduced in the literatures [10]–[12]. However, in these coupled inductor based converters, the input electrolytic capacitors suffer a relatively large input current ripple, which decreases the circuit reliability. Therefore, some interleaved high step-up converter with coupled inductor or winding-cross-coupled inductors are presented to achieve large voltage conversion and reduce the input current ripple at the same time [13]–[15]. However, the winding-cross-coupled inductors are a little complex and difficult to design, which increases the circuit complexity and difficulty.

The high frequency transformer, which is the essential component in the isolated dc/dc converters, can be also shifted to the non isolated converters. The interleaved high step-up converter with voltage gain extension cell is the recent achievement in this research topic. The voltage gain extension cell is made up of a three-winding transformer, two voltage regenerative diodes, and two series capacitors. The series capacitors are charged and discharged alternatively to double the voltage gain. Unfortunately, two additional active switches are necessary to absorb the energy stored in the leakage inductance, which makes the converter a little complex. Furthermore, the two interleaved phases are coupled by connecting the regenerative diodes from one phase to another phase. Its inherent influence to the circuit performance is not easy to explore.

2. PROPOSED TECHNIQUE

The use of the voltage multiplier technique applied to the classical non-isolated dc–dc converters in order to obtain high step-up static gain, reduction of the maximum switch voltage, zero current switching turn-on. The diodes reverse recovery current problem is minimized and the voltage multiplier also operates as a regenerative clamping circuit, reducing the problems with layout and the EMI generation. These characteristics allows the operation with high static again and high efficiency, making possible to design a compact circuit for applications where the isolation is not required. The operation principle, the design procedure and practical results obtained from the implemented prototypes are presented for the single-phase and multiphase dc–dc converters.

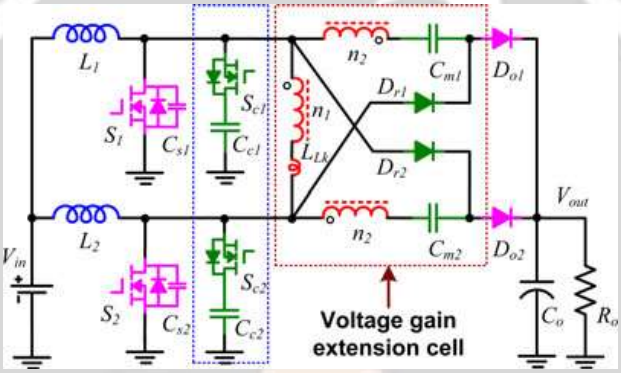

Fig-1: Interleaved high step-up converter with voltage gain extension cell

The proposed high step-up interleaved converter with built-in transformer voltage multiplier cells is plotted in Fig. 3, where *S*1 and *S*2 are the power MOSFETs, *L*1 and *L*2 are the input filter inductors, *Do*1 and *Do*2 are the output diodes, and *Co* is the output capacitor. There is a built-in transformer with three winding in the presented converter. The primary winding is *n*1 turns and the turns of the secondary and third windings are both *n*2 turns. *LLk* is the leakage summation of built-in transformer reflected to the primary winding. Each of the voltage multiplier cell is composed of the transformer winding with *n*2 turns, clamp diode *Dc*1(2) , regenerative diode *Dr*1(2) , clamp capacitor *Cc*1(2), multiplier capacitor *Cm*1(2). *V*in and *V*out are the input and output voltages, respectively. *N* is defined as the turns ratio *n*2 /*n*1 of the built-in transformer. The key steady-state waveforms of the proposed converter are shown in Fig. 4. There are 12 main operational stages in one switching period, and only six of them are analyzed in detail due to its symmetrical circuit structure. And the corresponding equivalent circuits for each operational stage are illustrated

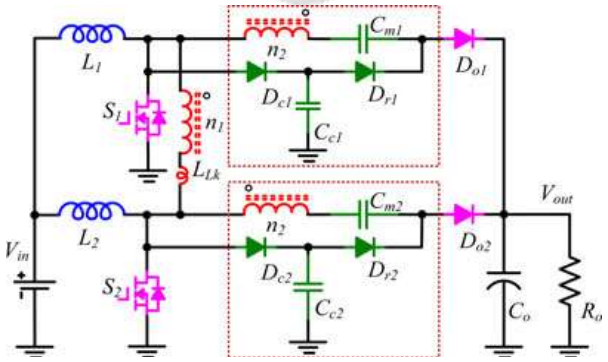

Fig-2: Proposed interleaved high step-up converter with built-in transformer voltage multiplier cells

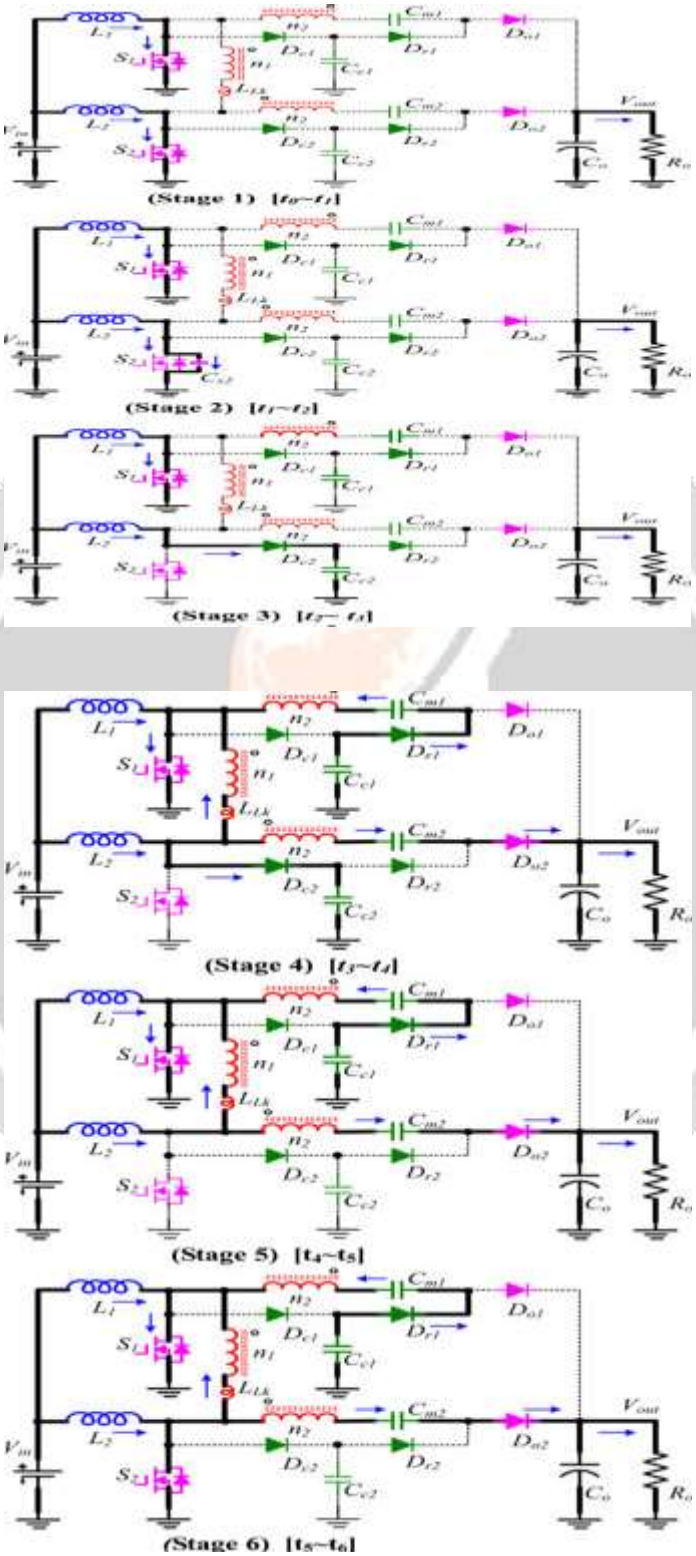

Fig-3: Operation stages of proposed converter.

2.1 OPERATING PRINCIPLE AND OPERATION MODES

1) Stage 1 [t0, t1]: Before *t*1, switches *S*1 and *S*2 are both in the turn-on state. Clamp diodes *Dc*1 and *Dc*2, regenerative diodes *Dr*1 and *Dr*2, and output diodes *Do*1 and *Do*2 are all reverse-biased. Both the two input inductors *L*1 and *L*2 are charged by the input voltage *V*in, respectively

$$i_{L1}(t) = I_{L1}(t_0) + \frac{V_{\text{in}}}{L_1} \cdot t \qquad (1)$$

$$i_{L2}(t) = I_{L2}(t_0) + \frac{V_{\text{in}}}{L_2} \cdot t. \qquad (2)$$

2) Stage 2 [t1, t2]: At *t*1 , switch *S*2 turns off, its parasitic capacitor *Cs*2 is charged by the current of the input inductor *L*2 in an approximately linear way

$$v_{ds2}(t) = \frac{I_{L2}(t_1)}{C_{s2}} t. \qquad (3)$$

3) Stage 3 [t2, t3]: At *t*2 , the drain–source voltage *vds*2 is charged and increased to make clamp diode*Dc*2 forward-biased. Then,*Dc*2 begins to conduct and clamp capacitor *Cc*2 is charged by the current of the input inductor *L*2 linearly. Switch *S*2 turns off and its drain–source voltage *vds*2 is clamped by capacitor *Cc*2

$$v_{ds2}(t) = V_{c2}(t_2) + \frac{I_{L2}(t_2)}{C_{c2}} t. \qquad (4)$$

4) Stage 4 [t3, t4]: At *t*3 , the voltage of output diode*Do*2 decreases to zero and it begins to turn on. As the current through *Do*2 increases, the current through clamp capacitor *Cc*2 decreases. The multiplier capacitors *Cm*1, *Cm*2 , the second and third windings of the built-in transformer operate as voltage sources. This is the inherent reason why the proposed converter can greatly extend the voltage gain. Meanwhile, regenerative diode *Dr*1 begins to conduct. The energy stored in clamp capacitor*Cc*1 starts to transfer tomultiplier capacitor*Cm*1 through regenerative diode *Dr*1 , second winding of built-in transformer and switch *S*1 . The current through *Cc*1 and *Cm*1 is controlled by the leakage inductance *LLk*

$$i_{S1}(t) = i_{L1}(t) + (N+1) \cdot i_{Dr1}(t) + N \cdot i_{Do2}(t) \qquad (5)$$

$$i_{L2}(t) = i_{Cc2}(t) + N \cdot i_{Dr1}(t) + (N+1) \cdot i_{Do2}(t) \qquad (6)$$

$$i_{Lk}(t) = N \cdot i_{Dr1}(t) + N \cdot i_{Do2}(t). \qquad (7)$$

5) Stage 5 [t4, t5]: At *t*4 , the current through clamp capacitor *Cc*2 decreases to zero and clamp diode *Dc*2 turns off naturally. As a result, there is no reverse-recovery problem for the clamp diodes. The energy stored in the multiplier capacitor *Cm*2 continues to transfer to the load

$$i_{L2}(t) = N \cdot i_{Dr1}(t) + (N+1) \cdot i_{Do2}(t). \qquad (8)$$

6) Stage 6 [t5, t6]: At *t*5 , switch *S*2 turns on. Due to the leakage inductance *LLk* , *S*2 turns on with zero current switch (ZCS) soft switching condition. The current falling rate through output diode *Do*2 is controlled by leakage inductance *LLk* , which alleviates the output diode reverse-recovery problem. This stage ends when output diode *Do*2 turns off

$$i_{Do2}(t) \approx I_{Do2}(t_5) - \frac{V_{\text{out}} - V_{Cm2}}{N^2 \cdot L_{Lk}} \cdot t. \qquad (9)$$

A similar operation works in the rest stages of the switching period. Due to the circuit symmetry of the proposed converter, it is reasonable to regard *L*1 = *L*2 = *L*, *Cc* 1 = *Cc*2 = *Cc* , and *Cm*1 = *Cm*2 = *Cm*. In order to simplify the detailed analysis, the leakage inductance is assumed to be zero and the voltages on the clamp capacitors and the multiplier capacitors are constant during the whole switching transition. As a result, it can be concluded that *VCc*1 = *VCc*2 = *VCc* and *VCm*1 = *VCm*2 = *VCm*. The detailed topology performance of the presented converter is analyzed as follows:

A. Voltage Gain Expression

The voltage on the clamp capacitor *Cc*1 and *Cc*2 can be easily derived by

$$V_{Cc1} = V_{Cc2} = V_{Cc} = \frac{1}{1-D} \cdot V_{\text{in}} \qquad (10)$$

where *D* is duty cycle of the switches *S*1, *S*2 .

When *S*1 turns on and *S*2 turns off, as the operation stage 4 in Fig. 4, the voltage on the second wing of the built-in transformer *Vtn*2 can be derived by

$$V_{tn2} = V_{Cm1} - V_{Cc1}. \qquad (11)$$

The output voltage can be expressed by

$$V_{\text{out}} = V_{Cm2} + V_{tn2} + V_{Cc2}. \qquad (12)$$

The voltage on the multiplier capacitors *Cm*1 and *Cm*2 is given by

$$V_{Cm} = (N+1) \cdot V_{Cc} = \frac{1}{2} \cdot V_{\text{out}}. \qquad (13)$$

The voltage on the primary wing of the built-in transformer *Vtn*1 is

$$V_{tn1} = V_{Cc2} \qquad (14)$$

$$\frac{V_{tn2}}{V_{tn1}} = N. \qquad (15)$$

From (10) to (15), the voltage gain of the proposed converter can be derived by

$$M = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{2 \cdot (N+1)}{1-D}. \qquad (16)$$

From (16), it can be concluded that a voltage multiplier is achieved to extend the voltage gain of the proposed converter compared with the conventional interleaved boost converter. The switch duty cycle and the turns ratio of the built-in transformer can be employed as two independent control variables to achieve extremely large voltage conversion ratio with optimized switch duty cycle. When the turns ratio *N* is zero, which means the built-in transformer is removed from the proposed converter. The proposed converter can be degenerated as the switched capacitor-based interleaved boost converter [8], whose voltage gain is twice of that the conventional interleaved boost converter. Compared with the switched capacitor-based interleaved boost converter, the clear advantages of the proposed converter is that the voltage gain can be easily increases by increasing the turns ratio of the built-in transformer rather than by inserting *N*-stage switched capacitor cells.

B. Voltage Stress Analysis

The voltage stress of the switches *S*1, *S*2 and the clamp diodes *Dc*1,*Dc*2 is equal to that of the clamp capacitors, which are given By

$$V_S = V_{Dc} = V_{Cc} = \frac{V_{\text{out}}}{2 \cdot (N+1)}. \qquad (17)$$

It can be concluded that seen that the voltage stress of the power MOSFETs is determined by the turns ratio of the built-in transformer and the output bus voltage. The maximum switch voltage stress is only half of the high bus voltage. As the turns ratio increases, the switch voltage stress decreases, which makes the low-voltage rated power MOSFETs with low RDS ON available to reduce the conduction losses in the high step-up and high output voltage applications.

The voltage stress of the output diodes *Do*1,*Do*2 can be derived By

$$V_{Do} = V_{\text{out}} - V_{Cc} = \frac{2 \cdot N + 1}{2 \cdot (N + 1)} \cdot V_{\text{out}}. \qquad (18)$$

The voltage stress of the regenerative diodes $Dr1$,$Dr2$ can be derived by

$$V_{Dr} = V_{\text{out}} - V_{Cc} = \frac{2 \cdot N + 1}{2 \cdot (N + 1)} \cdot V_{\text{out}}. \qquad (19)$$

From (18) and (19), it can be seen that the voltage stress of the regenerative diodes is the same as that of the output diodes. As the turns ratio of the built-in transformer increases, the voltage stress of the regenerative and output diodes increases. Fortunately, it is always lower than the output voltage.

Due to the leakage inductance of the built-in transformer, ZCS turn-on is realized for the switches $S1$ and $S2$, which reduces the switching losses. Furthermore, the clamp diode turns off naturally. Consequently, there is no reverse-recovery problem for the clamp diodes. In addition, the current falling rate of the regenerative and output diodes is controlled by the leakage inductance of the built-in transformer, which alleviates the diode reverse-recovery problem.

3 SIMULATION RESULTS

The nominal output power and input voltage equal to Vi = 127 V_{rms} are presented from Figs. 23 to 30, considering the operation with the third-harmonic reduction technique. The $L1$ and $L2$ currents are presented in Fig. 23 and its current ripple is close to the theoretical values 0.3 and 3.56 A, respectively The CS and CM capacitor voltages are presented in Fig. 24. The theoretical value of the CS and CM capacitor voltages at the peak of the input voltage, considering the capacitor voltage ripple null, is equal to 110 and 290 V, respectively The switch voltage and current are presented. The maximum switch voltage is close to 300 V for an input voltage equal 127 Vrms and output voltage equal to 400 V.

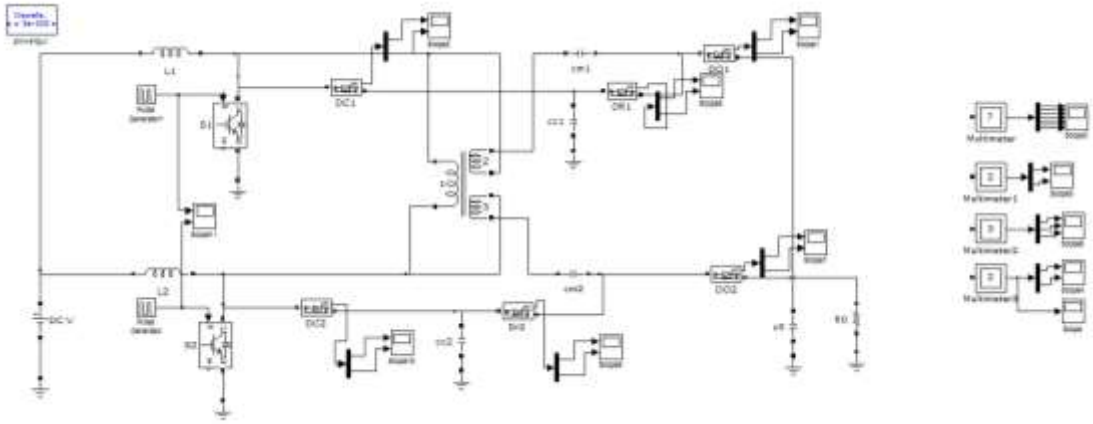

Fig-4: Simulation diagram of the proposed system

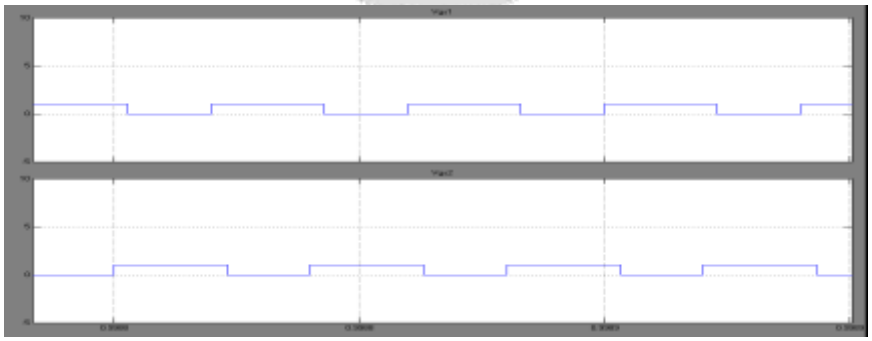

Fig-5: PWM pulses applied to proposed system

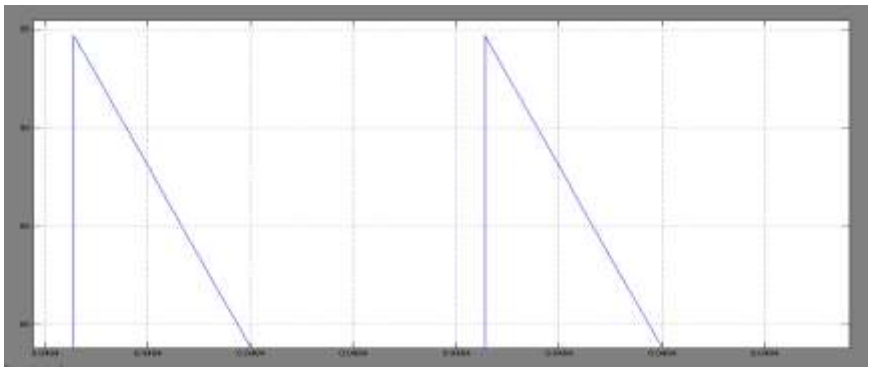

Fig-6: output current flowing through L_1

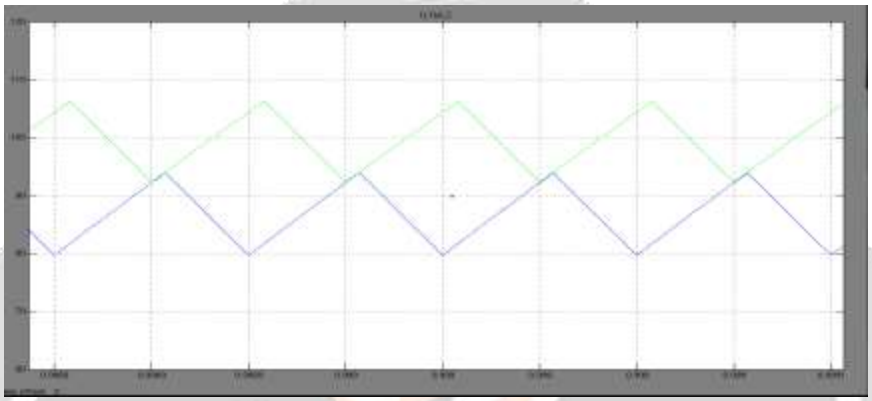

Fig-7: output current flowing through L_2

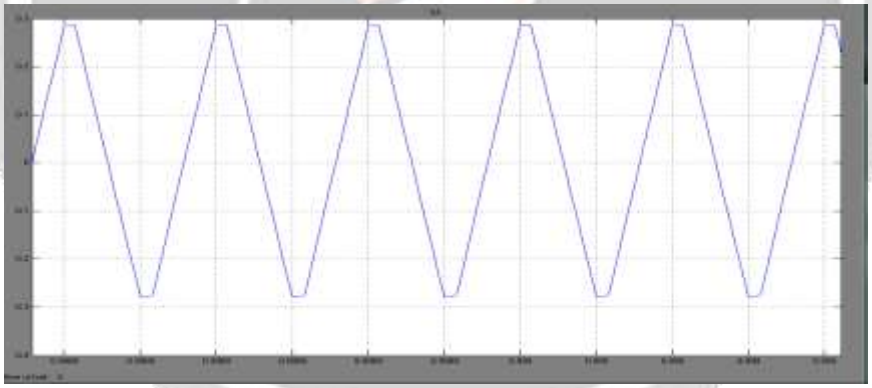

Fig-8: output current flowing through L_k

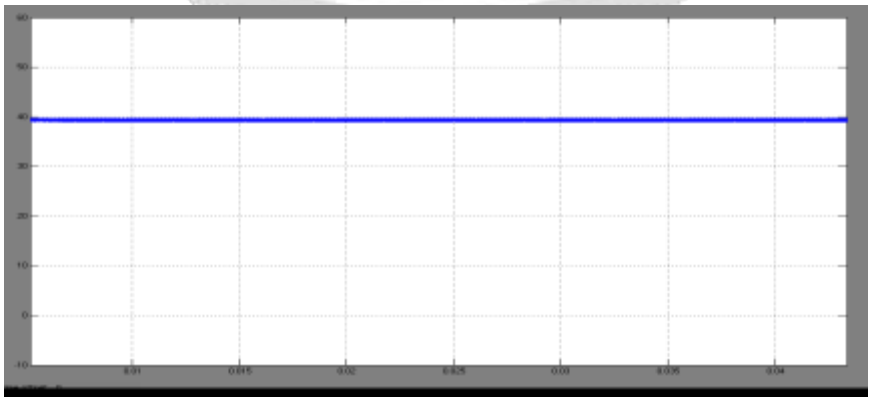

Fig-9: output voltage across capacitor Cm1

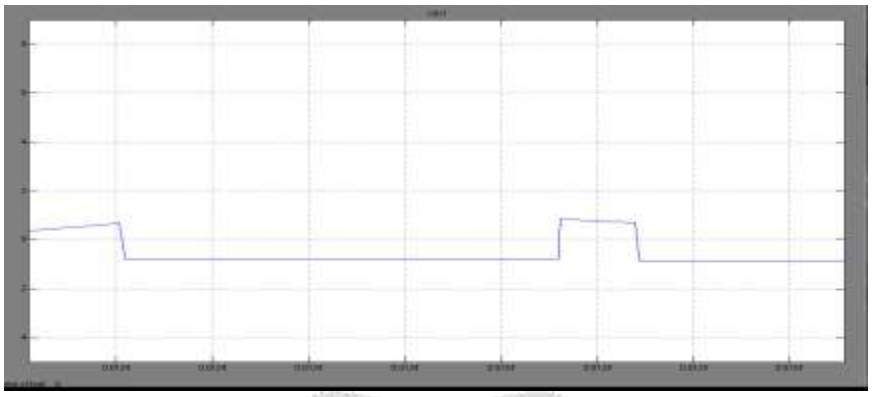

Fig-10: output voltage across diode Vdo1

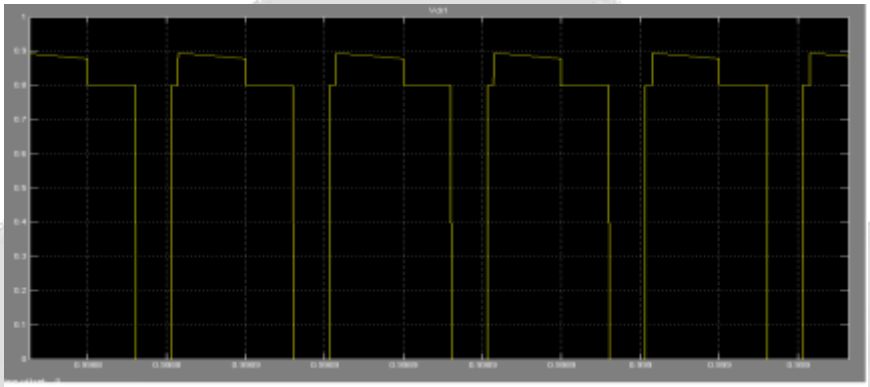

Fig-11: output voltage across diode Vdr1

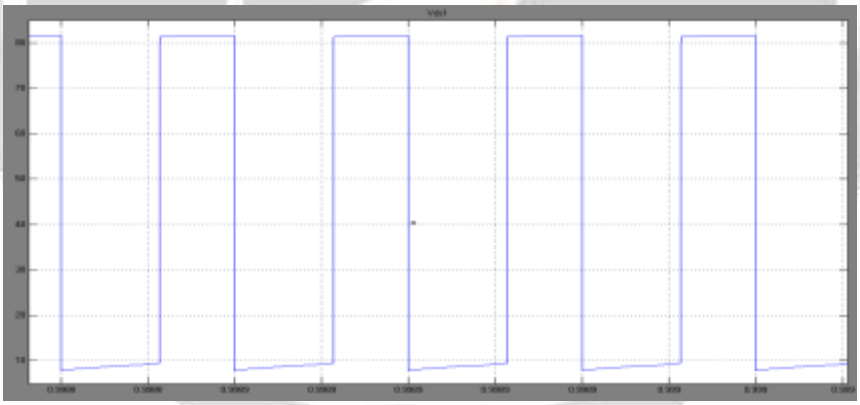

Fig-12: output voltage across diode Vds1

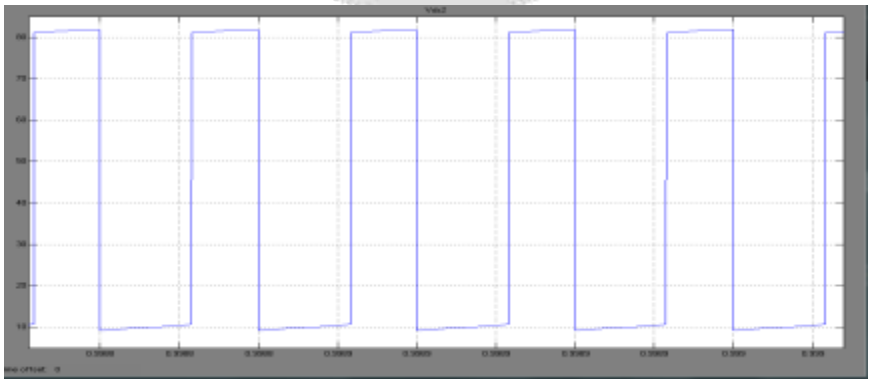

Fig-13: output voltage across diode Vds2

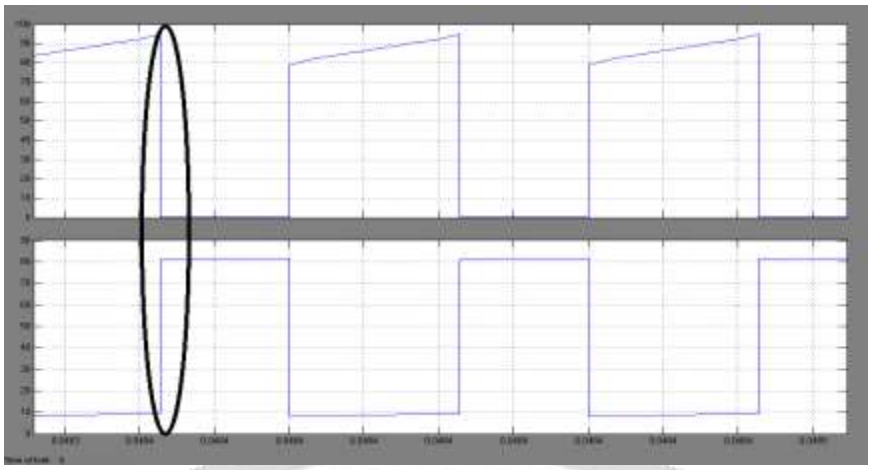

Fig-14: Results of ZCS Turn-On of *S*1

4. CONCLUSIONS

In this Paper, a interleaved high step-up converter with built-in transformer voltage multiplier cells has been proposed for the high large voltage gain conversion systems. From the detailed operational analysis, circuit performance compassion and experimental results, the presented converter has the following clear advantages: 1) an additional control freedom is provided by the built-in transformer voltage multiplier cells to achieve extremely high-voltage conversion ratio and minimize the current ripple; 2) the switch voltage stress is reduced to make the low voltage rated power device available and the conduction losses reduced; 3) ZCS is achieved for the switches and the diode reverse recovery problem is alleviated to improve the conversion efficiency. It can be concluded that the proposed converter is a suitable candidate for the high step-up and high-efficiency sustainable energy applications.

5. REFERENCES

[1] Y.Gu,W. Li,Y. Zhao, B.Yang, C. Li, and X. He, "Transformerless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 793–805, Feb. 2013.
[2] G. Spiazzi, P. Mattavelli, and A. Costabeber, "High step-up ratio flyback converter with active clamp and voltage multiplier," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3205–3214, Nov. 2011.
[3] W. Li, L. Fan, Y. Zhao, X. He, D. Xu, and B.Wu, "High step-up and high efficiency fuel cell power generation system with active clamp flyback forward converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 599–610, Jan. 2012.
[4] Y. Zhao, X. Xiang, W. Li, X. He, and C. Xia, "Advanced symmetrical voltage quadruple rectifiers for high step-up and high output-voltage
converters," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1622–1631, 2013.
[5] W. Li and X. He, "Review of non-isolated high step-up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, 2011.
[6] H.Wu and X. He, "Single phase three-level power factor correction circuit with passive lossless snubber," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 946–953, Nov. 2002.
[7] L. huber and M. M. Jovanovic, "A design approach for server power supplies for networking," in *Proc. IEEE INTELEC'00*, 2000, pp. 1163–1169.
[8] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "Voltage multiplier cells applied to non-isolated DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 871–887, Mar. 2008.
[9] F. Zhang, L. Du, F. Z. Peng, and Z. Qian, "A new design method for high-power high-efficiency switched-capacitorDC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 832–840, Mar. 2008.
[10] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switchedcapacitor/ switched-inductor structures for getting transformerless hybrid DC–DC PWM converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 2, pp. 687–696, Mar. 2008.
[11] E. H. Ismail, M. A. Al-Saffar, A. J. Sabzali, and A. A. Fardoun, "A family of single-switch PWM converters with high step-up conversion ratio,"*IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 4, pp. 1159–1171, May 2008.

[12] K. B. Park, G. W.Moon, andM. J. Youn, "Nonisolated high step-up boost converter integrated with sepic converter," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2266–2275, Sep. 2010.
[13] K. C. Tseng and T. J. Liang, "Novel high-efficiency step-up converter," in *Proc. IEE-Elect. Power Appl.*, vol. 151, no. 2, Mar. 2004, pp. 182–190.
[14] Y. Zhao,W. Li, and X. He, "Single-phase improved active clamp coupledinductor- based converter with extended voltage doubler cell," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2869–2878, Jun. 2012.
[15] L. S. Yang, T. J. Liang, H. C. Lee, and J. F. Chen, "Novel high step-up DC–DC converter with coupled-inductor and voltage-doubler circuits," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4196–4206, Sep. 2011.