DESIGN OF A MODULAR FEEDFORWARD PHASE/FREQUENCY DETECTOR FOR HIGH SPEED PLL

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ABSTRACT

Phase Frequency Detector (PFD) is convert the input analog signals into digital output by comparing both input signals in terms of phase and frequency. PFD is widely used in Phase lock loop (PLL) as a phase detector. This paper describes a fully functional modular Feedforward phase/frequency detector and to show the characteristics and behaviour of some PFD designs in order to improve some important aspects as the delay time and the power consumption in the classical model. Circuits are design using 180nm TSMC CMOS technology.

Keyword : - *PFD, PLL, Feedforward, TSMC, CMOS.*

1. INTRODUCTION

PLL is a closed-loop circuit. The main work of PLL is comparing its output phase with the phase of an incoming reference signal and adjusts itself until both are straight, i.e., the output's phase is "locked" to that of the input signal thus its known as PLL. It's composed a phase detector (PD), a low-pass filter (LPF), and a voltage controlled oscillator (VCO). The circuit compares the input signal phase and the oscillator output signal and adjusts the last one to maintain the phases matched. As it is known, the frequency is the derivate of phase. So, maintaining phases matched means maintaining matched frequencies. Block diagram of PLL shown in Fig. 1.

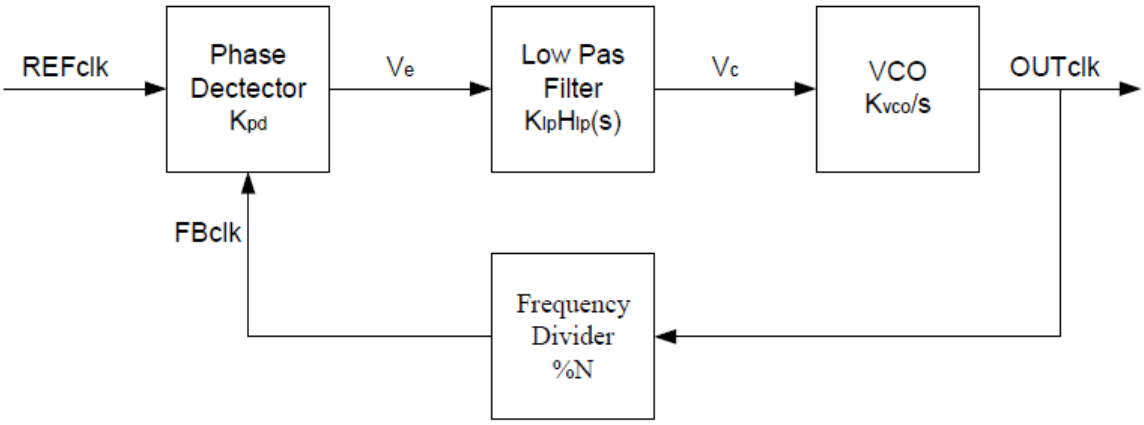

Fig- 1 Block diagram of PLL

PD gives an output signal whose dc value is directly proportional to the difference between the phases (Δϕ) of the two periodic inputs. Typically, PD generates an output pulse whose width is equal to the time difference between the consecutive zero crossing of the two inputs. Since the two inputs are not equal, the phase difference exhibits a "beat" behavior with an average value of zero. PDs are allowed to detect both phase and frequency difference proves

extremely useful because it significantly increases the acquisition range and lock speed of PLLs [1]. PFD depicts in Fig. 2.

Fig- 2 Block diagram of PFD

2. PREVIOUS WORK

An architecture of PLL used a PFD for detect clock phase and frequency. Dynamic PFD maintains the stability of the circuit when operate at both high frequency and low frequency [2]. Gated phase frequency detector (GPLL) operate in two mode, first mode it tracks the HF input signal in another mode GPLL adjust the last frequency used for oscillation of oscillator [3]. Maximum difference between the phase of two input analog signals cannot detect by the PFD is called dead zone. 8- Transistor PFD removed the reset the path and solves the problem of dead zone [4]. Phase frequency detector decreases the locking time and an output signal frequency with little clock jitter [5].
Symmetry PFD achieve the fast locking with low noise or low jitter clock signal. Symmetry PFD used only two XOR gates and generates lead and lag signal to voltage to current converter and filter [6]. Pass transistor based PFD using the two inverters to decreases the clock skew thereby result in dead zone reduction [7].

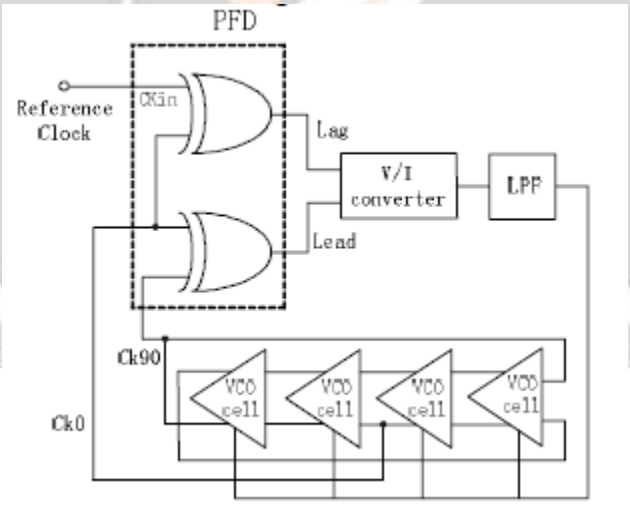

Fig- 3 PLL architecture [6]

3. FEEDFORWARD-RESET PFD

This feedforward-reset PFD model is to avoid de bad effect of the D-FF in the PFD behaviour and, so, to use it in more exigent applications. Its improvement consists of removing the dependence that the reset signal has with the D-FF. That way, the D-FF delay will not affect the width and the delay of this signal and a higher operation speed will be achieved. Feedforward-reset PFD shown in Fig. 4.

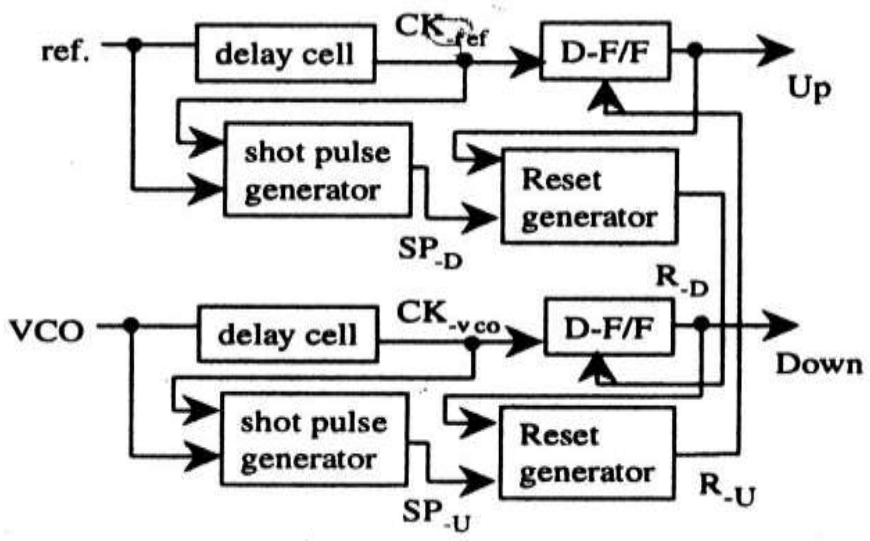

Fig- 4 Block diagram of feedforward-reset PFD

3.1 Delay Cell

Delay cell takes the input signal and gives it a delay. Its output is called "CK-ref" or "CK-vco", respectively. It could be implemented by some inverters (even number for not invert the signal), as in the conventional one. This way, the delayed input signals are obtained and they will be in D-FF input, respectively. Delay cell shown in Fig. 5.

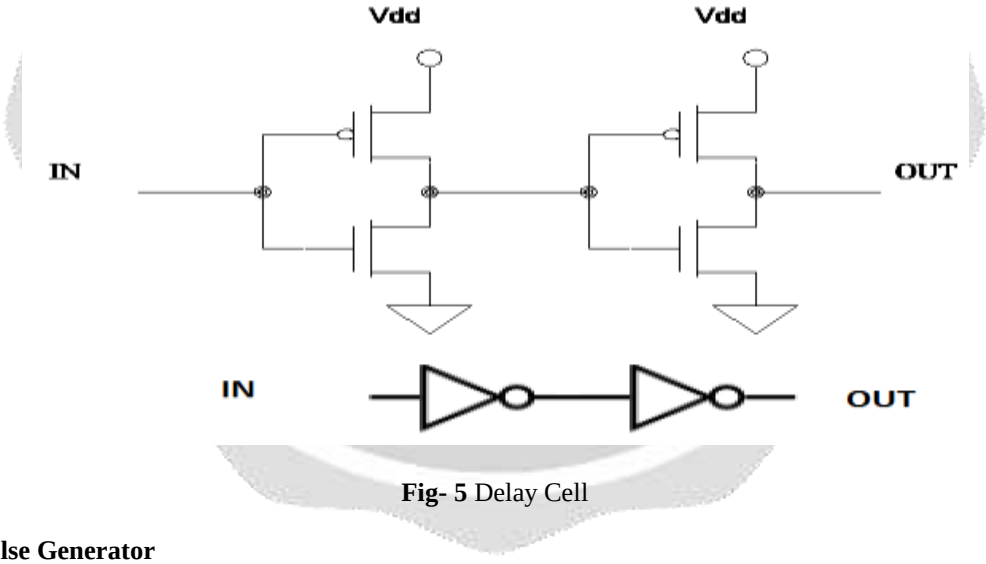

Fig- 5 Delay Cell

3.2 Shot Pulse Generator

It generates a pulse that will activate the "reset generator". It has two input signals: the original input signal (ref and VCO in each branch) and the delayed by the delay cell input signal. It will produce a pulse at the same time as the one of its inputs will be active first, so, the ref or the VCO signal, respectively. The second input, the delayed ref or VCO signal, determinates de width of the pulse.

3.3 Reset generator

It is implemented as an OR gate whose inputs are the D-FF output signal and the "shot pulse generator" output. So, at the output of this item we will have the reset signal that will reset the other input signal D-FF output. This signal will start at the same time as the ref or VCO signal because of the OR gate operation.

3.4 D-Flip Flop (D-FF)

As it is known, it conserves the value of the D input in its Q output while the clock signal is active. In the design of this new PFD it is only described with one input, so, the delayed PFD input signal will act as the clock signal (CLK) of the D-FF. And D input in the D-FF will be a constant "1" signal.
That way, at the output of it, Up and Down signals will be CKref and CKvco, respectively, according to the reset signal described before.
This reset signal, when it will be active, will deactivate D-FF signal, resetting the D-FF dispositive. Then, the outputs will be active again until a new up (or down, depending on the D-FF) rising edge in the input will active the output again.
Besides, the fact that one reset signal is introduced in the other D-FF, allows a kind of synchronism between the two PFD outputs: Up and Down. Fig. 6 depicts the operation of D-FF.

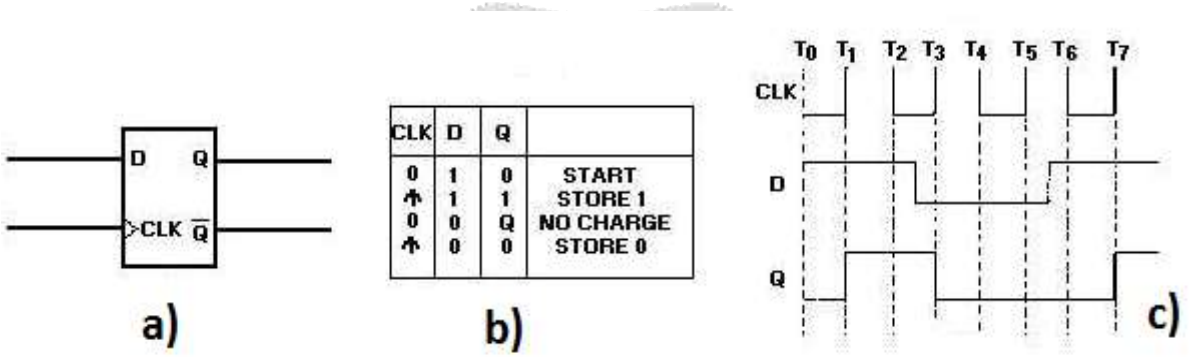

Fig- 6 a) D-FF standard symbol. b) Truth table c) Timing diagram

3.5 Feedforward-Reset PFD

Finally feedforward-reset PFD design using delay cell, shot pulse generator, reset generator and D-FF. Feedforward reset PFD reduced a reset time thereby result in decreases dead zone. Fig. 7 depicts the schematic of feedforward-reset PFD.

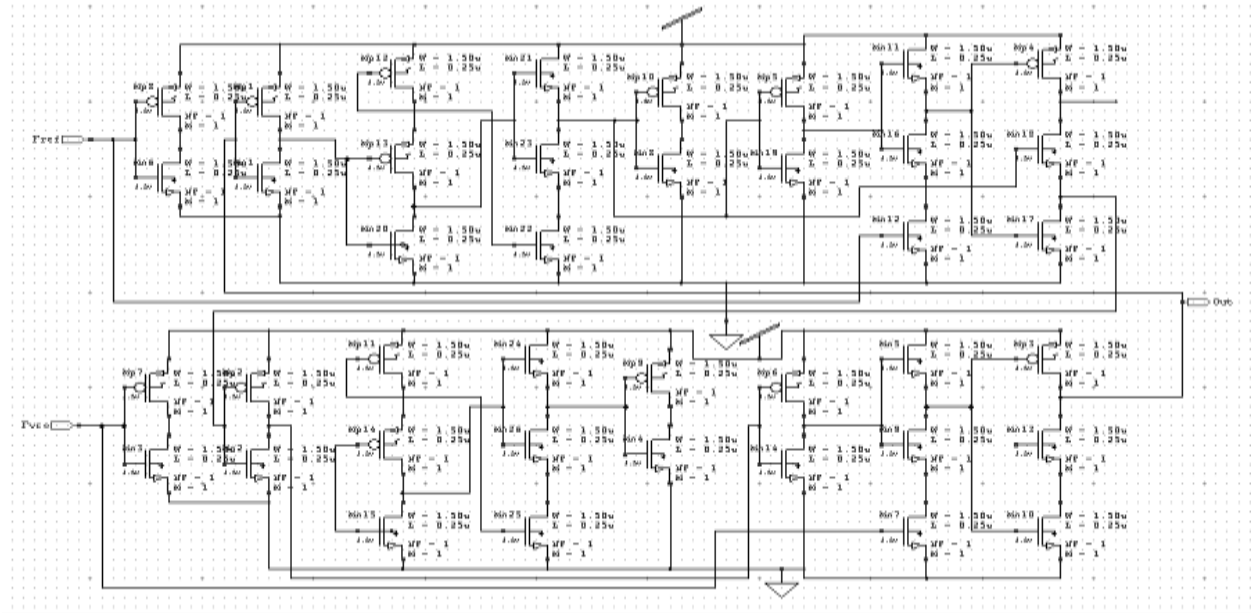

Fig- 7 Feedforward-Reset PFD

4. SIMULATION RESULT

After the theorist study of each design, it is necessary to verify the properties of which boast. The parameters that will be analyzed are the ones that describe the operation of this kind of circuits: transient response, periodic noise, the delay time/reset time and the power consumption. For the simulations in TANNER the used technology is TSMC_180µm CMOS.

The delay between Fref and CKref or Fvco and CKvco is so tiny that the reset generator does not work as it should do. So, the alternatives is to put more inverter circuits in these cell to increase the delay between the original input signals and the D-FFs inputs which increases the number of transistors and make the schematic more complicated. Table 1 shows the two input signals are two pulse ones with the following parameters.

Table 1 Transient simulation profile

	Period	PW	Td	Tf	Tr	Low logic	High Logic
Fref	2µ	1µ	0p	100p	100p	0V	1.8V
Fvco	1.8 µ	0.9µ	80n	100p	100p	0V	1.8

Alternatively, the following simulations will be done with some external sources with the same frequency of Fref and Fvco, respectively; but adding to their delay, other extra one. It is a practical way to face the problem acting as the delay cell should do. Simulation result of feedforward-reset PFD shown in Fig. 8.

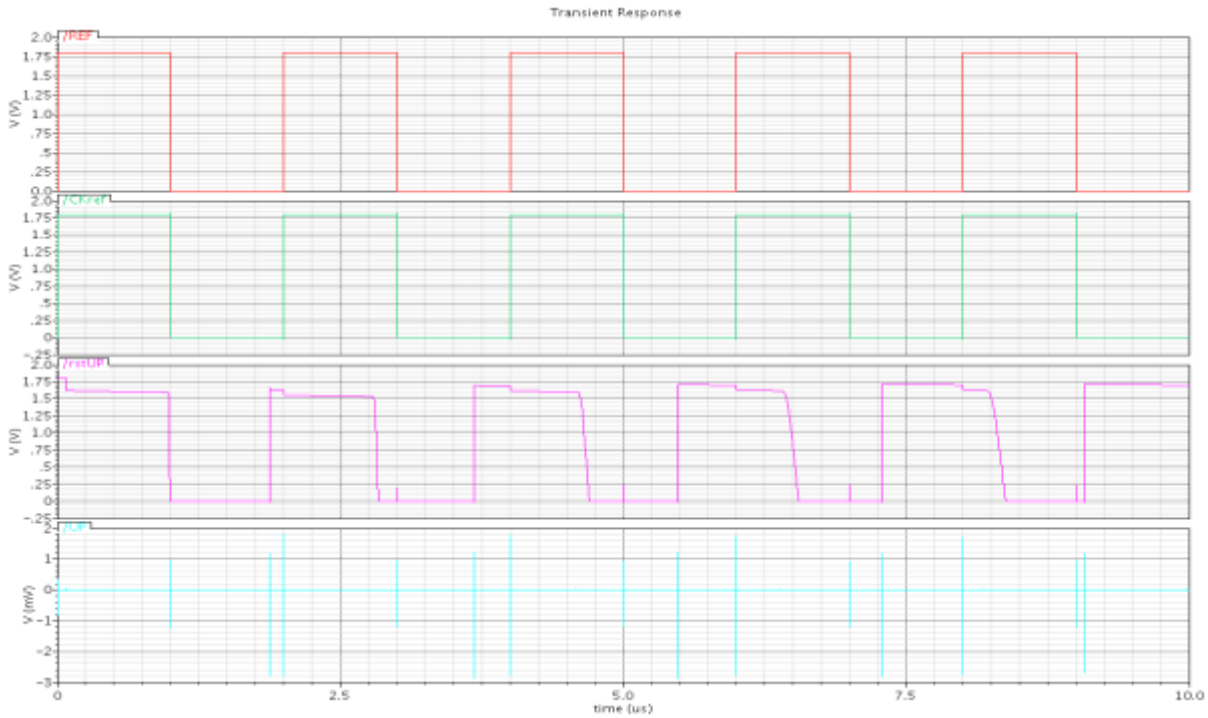

Fig- 8 Feedforward reset PFD transient response

5. CONCLUSIONS

All the results that were detailed before are summarized in the following table. As it can be seen in it, the main advantage of the Feedforward reset PFD design is the independence of its reset generation, who does not depend on the DFF delay. Apart from that, the design is much more complicated than the basic one. It includes 40 transistors that increase the noise, the current and the power consumption, and so, its price. As it is said in previous chapters, this disadvantage can be solved partially by using dynamic CMOS logic instead of the static one**.**

6. REFERENCES

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