DESIGN OF A PUSH–PULL DC-DC PHASE SHIFTED RESONANT CONVERTER

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ABSTRACT

This paper presents analysis and design of push/pull converter with ZVS and ZCS control. The proposed converter has the following features: 1) zero-current commutation (ZCC) and natural voltage clamping (NVC) eliminate the need for active-clamp circuits or passive snubbers required to absorb surge voltage in conventional current-fed topologies. 2) Switching losses are reduced significantly owing to zero-current switching of primary-side devices and zero-voltage switching of secondary-side devices. Turn-on switching transition loss of primary devices is also negligible. 3) Soft switching and NVC are inherent and load independent. 4) The voltage across primary-side device is independent of duty cycle with varying input voltage and output power and clamped at rather low reflected output voltage enabling the use of low-voltage semiconductor devices. These merits make the converter good candidate for interfacing low-voltage dc bus with high-voltage dc bus for higher current applications. Steady state analysis, and simulation results are presented using MATLAB software.

Keyword: - *DC-DC Converter, Push-Pull Converter, Mosfet, ZVS, ZCS*

1. INTRODUCTION

Battery-based electric vehicles (EVs) and fuel cell vehicles (FCVs) are emerging as viable solutions for transportation electrification with lower emission, better vehicle performance, and higher fuel economy. Compared with pure battery-based EVs, FCVs are quite appealing with the merits of zero-emission, satisfied driving range, short refueling time, high efficiency, and high reliability. A diagram of a typical FCV propulsion system is shown in Fig. 1. Bidirectional and unidirectional dc/dc converters are utilized to develop high-voltage bus for the inverter. The energy storage system (ESS) is used to overcome the limitations of lacking energy storage capability and fast power transient of FCVs.

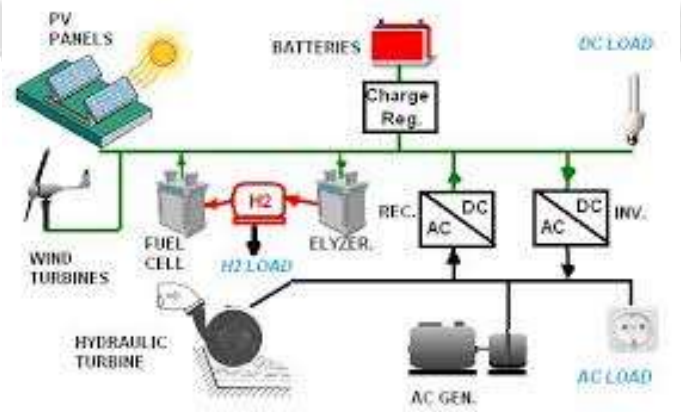

Fig-1: Diagram of a FCV propulsion system.

Bidirectional converter with high boost ratio and high efficiency is required to connect the low-voltage ESS and high- voltage dc-link bus. Compared with non isolated topologies, high-frequency (HF) transformer isolated converters are preferred with merits of high step up ratio, galvanic isolation, and flexibility of system configuration [6]. HF transformer isolated converters could be either voltage-fed [7]–[9] or current fed [10]–[20]. Advantages and

disadvantages of both types are compared in [21]–[23]. The voltage-fed converters have low switch voltage ratings enabling the use of switches with low ON-state resistance. This can significantly reduce conduction loss of primary-side switches. However, voltage-fed converters suffer from several limitations, i.e., high pulsating current at input, limited soft-switching range, rectifier diode ringing, duty cycle loss (if inductive output filter), high circulating current through devices and magnetic, and relatively low efficiency for high-voltage amplification and high-input current applications.

Compared with voltage-fed converters, current-fed converters exhibit smaller input current ripple, lower diode voltage rating, lower transformer turns-ratio, negligible diode ringing, no duty cycle loss, and easier current control ability. Besides, current-fed converters can precisely control the charging and discharging current of ESS, which helps achieving higher charging/discharging efficiency. Thus, current-fed converter is more feasible for the application of ESS in FCVs.

Three topologies of isolated current-fed dc/dc converters, i.e., full-bridge [10]–[12], L-type half-bridge [13]–[15], and push–pull [16], [17] have been researched. One drawback of current fed converters is the high turn-off voltage spike across the devices. Normally, active-clamp circuits [14-25] RCD passive snubbers [11], or energy recovery snubber [6] is employed to absorb the surge voltage and assist soft-switching. In RCD snubbers, energy absorbed by the clamping capacitor is dissipated in the resistor resulting in low efficiency. Active clamp suffers from high current stress (peak) and higher circulating current at light load.

The leakage inductance and parasitic capacitance of the HF transformer were utilized to achieve zero-current switching (ZCS) in [17]–[19]. However, resonant current is much higher than input current that increases the current stress of devices and magnetic requiring higher VA rating components. Besides, the variable frequency modulation makes the control implementation difficult and complex [20]. External auxiliary circuits are utilized to achieve ZCS and reduce the circulating current in [26]–[28] but complex. Although the trapped energy can be recycled, the auxiliary circuits still contribute to a significant amount of loss. In current-fed bidirectional converter, active soft commutation technique [11], [29], [30] is proposed to divert the switch current to another switch through transformer to achieve natural or zero-current commutation (ZCC) thus reducing or eliminating the need of snubber.

2. PROPOSED TECHNIQUE

To study the operation and explain the analysis of the converter:1) Boost inductor *L* is large enough to maintain constant current through it. 2) All the components are ideal. 3) Series inductors *Llk*1 and *Llk*2 include the leakage inductances of the transformer. The total value of *Llk*1 and *Llk*2 is represented as *Llk T* . *Llk* represents the equivalent series inductor reflected to the high-voltage side. 4) Magnetizing inductance of the transformer is infinitely large.

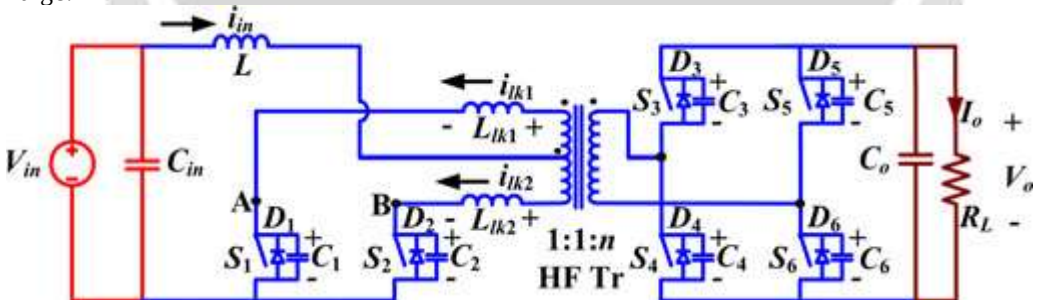

Fig-2: Proposed ZCS current-fed push–pull dc/dc converter.

2.1. Boost Mode (Discharging Mode) Operation

In this part, the steady-state operation and analysis with ZCC and NVC concept has been explained. Before turning OFF one of primary-side switches (say *S*1), the other switch (say *S*2) is turned-on. Reflected output voltage 2*Vo*/*n* appears across the transformer primary. It diverts the current from one switch to the other one through transformer causing current through just triggered switch to rise and the current through conducting switch to fall to zero naturally resulting in ZCC. Later, the body diode across switch starts conducting and its gating signal is removed leading to ZCS turn-off of the device. Commutated device capacitance starts charging with NVC.

The steady-state operating waveforms of boost mode are shown in Fig. 4.2. The primary switches *S*1 and *S*2 are operated with identical gating signals phase-shifted with each other by 180◦ with an overlap. The overlap varies with the duty cycle, and the duty cycle should be kept above 50%. The steady-state operation of the converter during

different intervals in a one half HF cycle is explained using the equivalent circuits shown in Fig. 4.3. For the rest half cycle, the intervals are repeated in the same sequence with other symmetrical devices conducting to complete the full HF cycle.

Interval 1 (Fig. 4(a); *to* < *t* < *t*1): In this interval, primary side switches *S*2 and anti parallel body diodes *D*3 and *D*6 of secondary-side H-bridge switches are conducting. Power is transferred to the load through HF transformer.

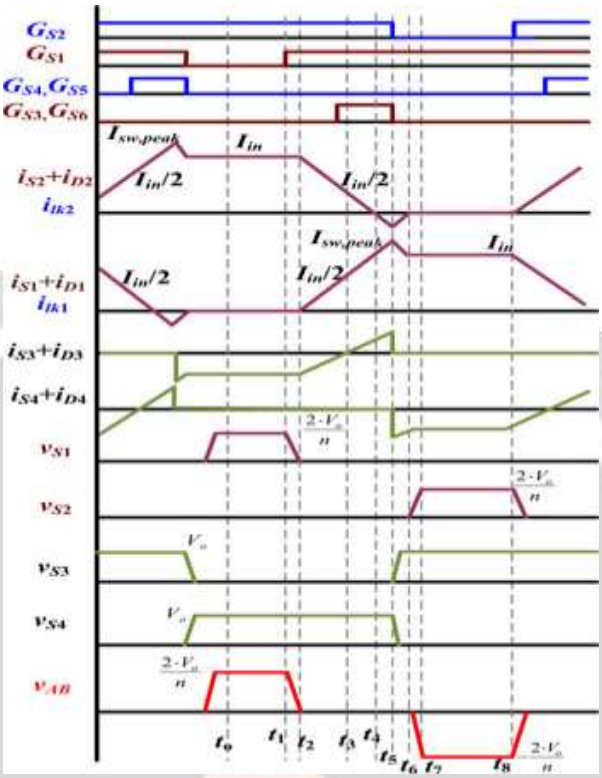

Fig-3: Operating waveforms of proposed ZCS current-fed push–pull converter in the boost mode.

The non-conducting secondary devices *S*4 and *S*5 are blocking output voltage *Vo* and the no conducting primary devices *S*1 are blocking reflected output voltage 2*Vo*/*n*. The values of current through various components are

$$iS1 = 0,\ iS2 = I\text{in},\ ilk1 = 0,\ ilk2 = I\text{in},\ iD3 = iD6 = I\text{in}/n.$$

Voltage across the switch *S*1:*VS*1= 2*Vo*/*n*.
Voltage across the switches *S*4 and *S*5:*VS*4 = *VS*5 = *V o*.

Interval 2 (Fig. 4(b); *t*1 < *t* < *t*2): At *t* = *t*1, primary switch *S*1 is turned-on. The corresponding snubber capacitor *C*1 discharges in a very short period of time.

Interval 3 (Fig. 4(c); *t*2 < *t* < *t*3): All two primary switches are conducting. Reflected output voltages appear across inductors *Llk*1 and *Llk*2, diverting/transferring the current through switch *S*2 to *S*1. It causes current through previously conducting device *S*2 to reduce linearly. It also results in conduction of switch *S*1 with zero current which helps reducing associated turn-on loss. The currents through various components are given by

$$i_{lk1} = i_{S1} = \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_2)$$

$$i_{lk2} = i_{S2} = I_{\text{in}} - \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_2)$$

$$i_{D3} = i_{D6} = \frac{I_{\text{in}}}{n} - \frac{4 \cdot V_o}{n^2 \cdot L_{lk\_T}} \cdot (t - t_2) \quad \text{.....(1)}$$

where $L_{lk\_T} = Llk1 + Llk2$. At the end of this interval $t = t3$, the anti parallel body diode $D3$ and $D6$ are conducting. Therefore, $S3$ and $S6$ can be gated on for ZVS turn-on. At the end of this interval, $D3$ and $D6$ commutates naturally. Current through all primary devices reaches Iin/2. Final values are:

$$ilk1 = ilk2 = I\text{in}/2,\ iS1 = iS2 = I\text{in}/2,\ iD3 = iD6 = 0.$$

Interval 4 (Fig. 4(d); $t3 < t < t4$): In this interval, secondary H-bridge devices $S3$ and $S6$ are turned-on with ZVS. Currents through all the switching devices continue increasing or decreasing with the same slope as interval 3. At the end of this interval, the primary device $S2$ commutates naturally with ZCC and the respective current $iS2$ reaches zero obtaining ZCS. The full current, i.e., input current is taken over by other device $S1$. Final values are:

$$ilk1 = iS1 = I\text{in},\ ilk2 = iS2 = 0,\ iS3 = iS6 = I_{\text{in}}/n.$$

Interval 5 (Fig. 4(e); $t4 < t < t5$): In this interval, the leakage inductance current $ilk1$ increases further with the same slope and anti parallel body diode $D2$ starts conducting causing extended zero voltage to appear across commutated switch $S2$ to ensure ZCS turn-off. Now, the secondary devices $S3$ and $S6$ are turned off. At the end of this interval, current through switch $S1$ reaches its peak value. This interval should be very short to limit the peak current though the transformer and switch reducing the current stress and kVA ratings. The currents through operating components are given by

$$i_{S1} = i_{lk1} = I_{\text{in}} + \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_4)$$

$$i_{D2} = -i_{lk2} = \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_4)$$

$$i_{S3} = i_{S6} = \frac{I_{\text{in}}}{n} + \frac{4 \cdot V_o}{n^2 \cdot L_{lk\_T}} \cdot (t - t_4). \quad \text{..... (2)}$$

Interval 6 (Fig. 4(f); $t5 < t < t6$): During this interval, secondary switches $S3$ and $S6$ are turned-off. Anti parallel body diodes of switches $S4$ and $S5$ take over the current immediately. Therefore, the voltage across the transformer primary reverses polarity. The current through the switch $S1$ and body diodes $D2$ also start decreasing. The currents through operating components are given by

$$i_{S1} = i_{lk1} = I_{sw,\text{peak}} - \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_5)$$

$$i_{D2} = -i_{lk2} = I_{D2,\text{peak}} - \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_5)$$

$$i_{D4} = i_{D5} = \frac{I_{lk,\text{peak}}}{n} - \frac{4 \cdot V_o}{n^2 \cdot L_{lk\_T}} \cdot (t - t_5). \quad \text{..... (3)}$$

At the end of this interval, current through $D2$ reduces to zero and is commutated naturally. Current through $S1$ reaches Iin . Final values: $ilk1 = iS1 = I\text{in},\ ilk2 = iD2 = 0,\ iD4 = iD5 = I\text{in}/n$.

Interval 7 (Fig. 4(g); $t6 < t < t7$): In this interval, snubber capacitor $C2$ charges to $2Vo/n$ in a short period of time. Switch $S2$ is in forward blocking mode now.

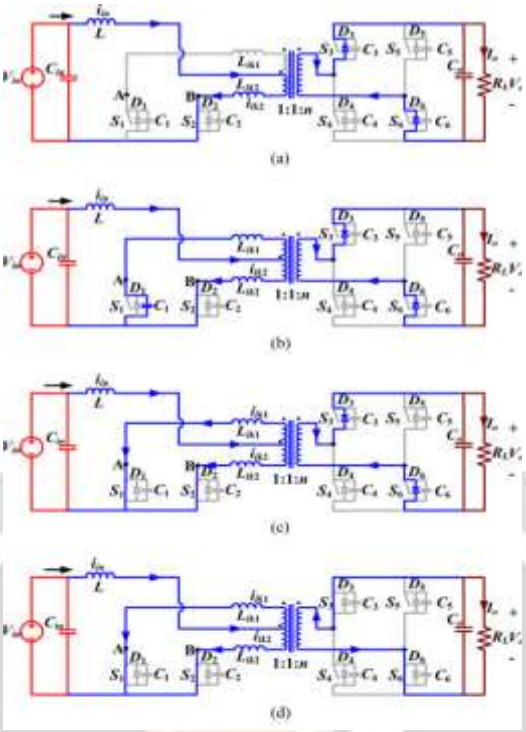

Fig-4: Equivalent circuits during different intervals of the boost mode operation.

Interval 8 (Fig. 4(h); $t7 < t < t8$): In this interval, currents through $S1$ and transformer are constant at input current Iin. Current through anti-parallel body diodes of the secondary switches $D4$ and $D5$ is at Iin$/n$.
The final values are: $ilk1 = iS1 = I$in, $ilk2 = iS2 = 0$, $iD4 = iD5 = I$in$/n$.
Voltage across the switch $S2 VS2 = 2Vo/n$.
In this half HF cycle, current has transferred from switch $S2$ to $S1$, and the transformer current has reversed its polarity.

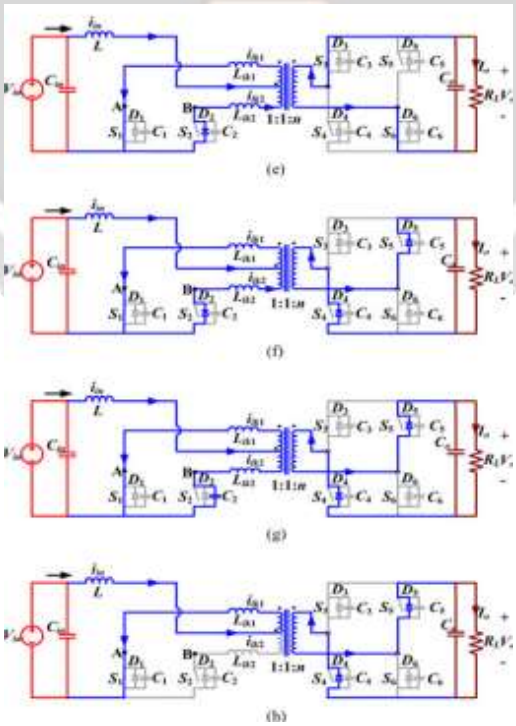

Fig-5: Equivalent circuits during different intervals of the boost mode operation.

4 SIMULATION RESULTS

A simulation design open loop system as shown in **Fig.6** is implemented in MATLAB SIMULINK with the help of coupled inductor, switches and diodes we get desired output voltage level

4.1 Boost mode

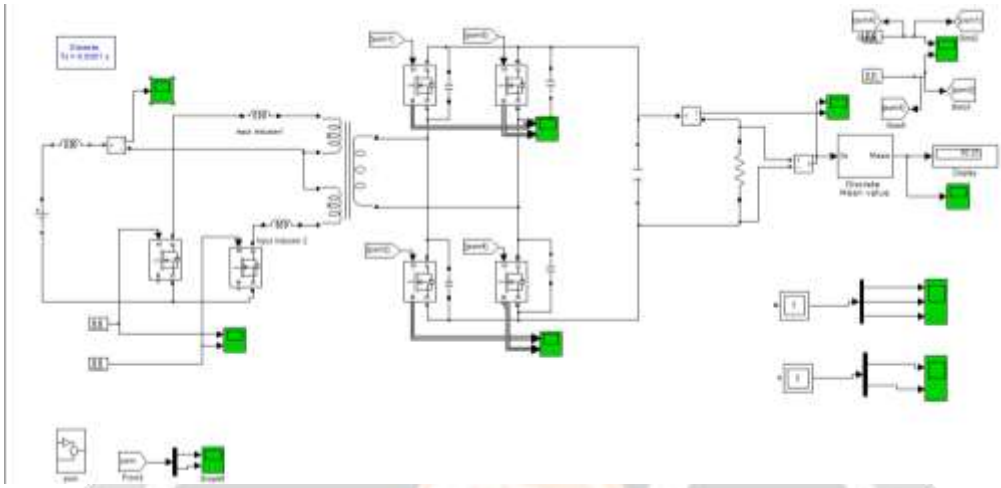

Fig-6: simulation of proposed circuit

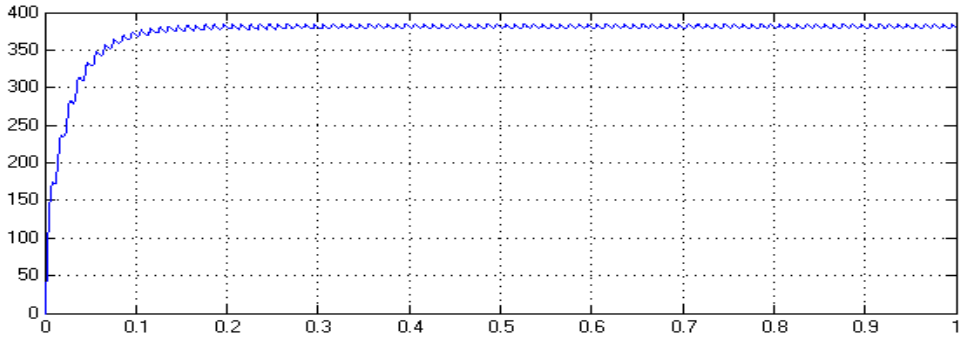

Fig-7: output voltage 380V (DC)

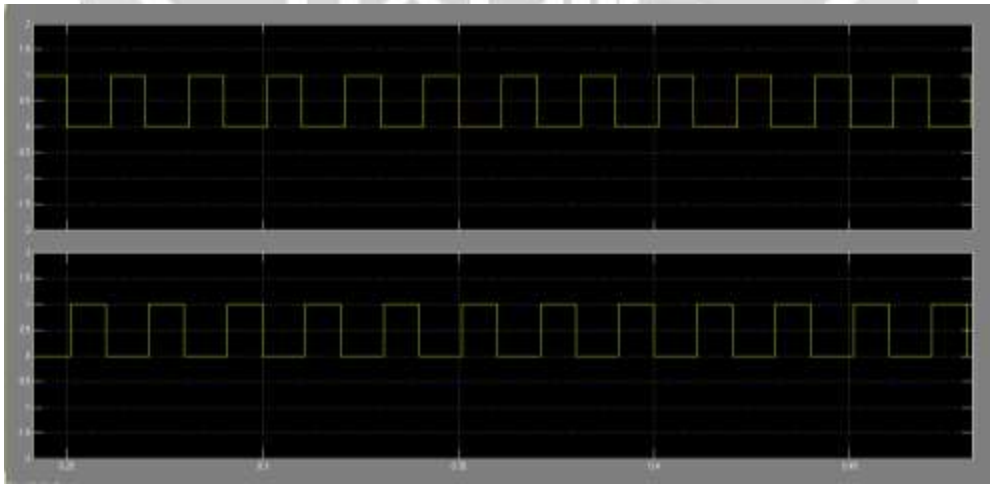

Fig-8: pwm pulses

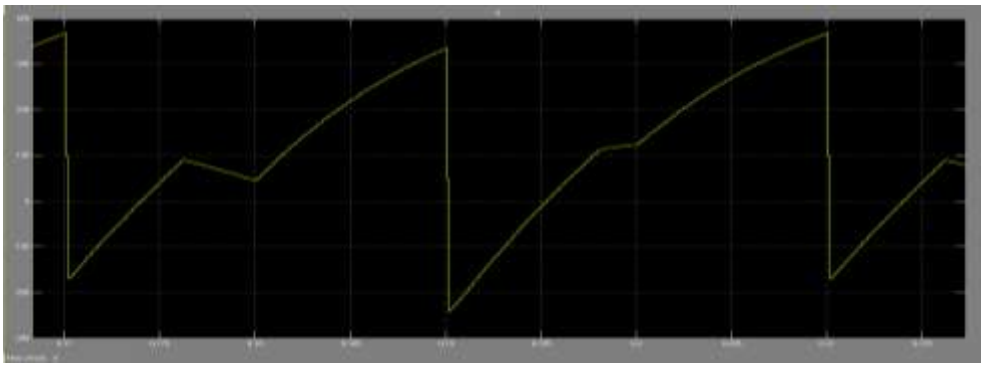

Fig-9: input inductor current

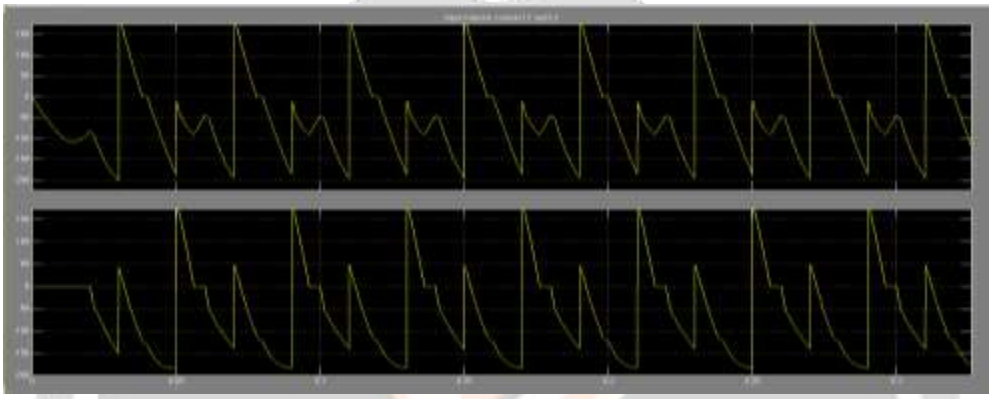

Fig-10: current through two series inductors

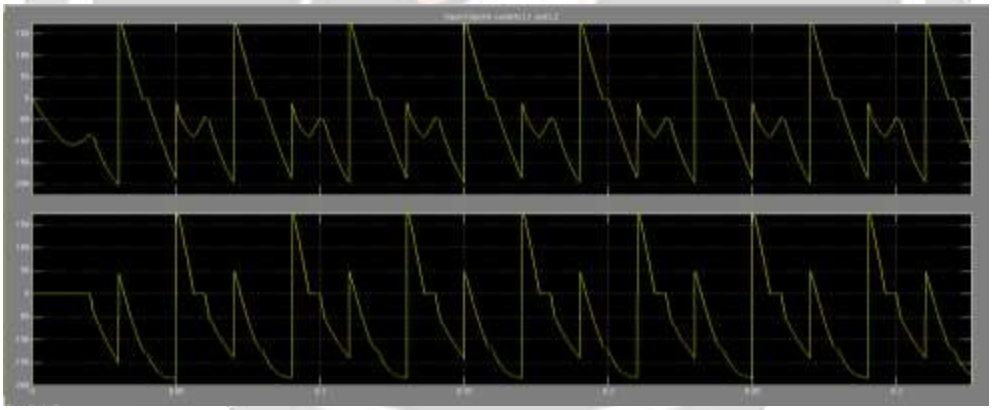

Fig-11: output voltage and current

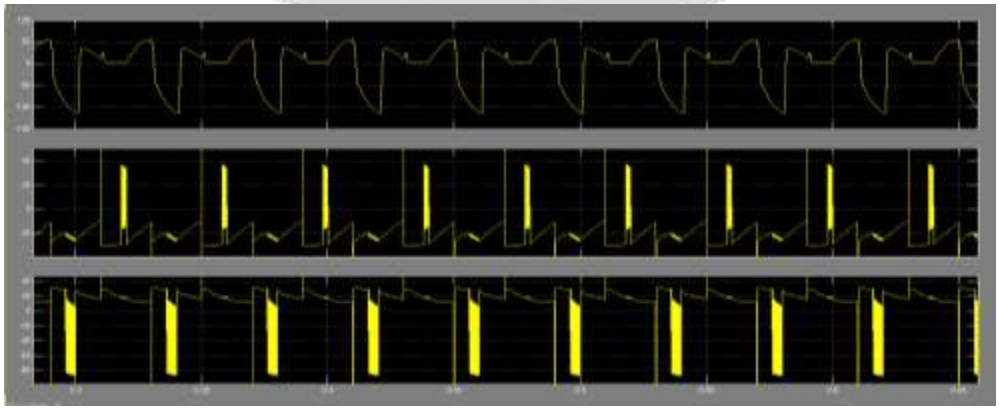

Fig-12: transformer winding voltages

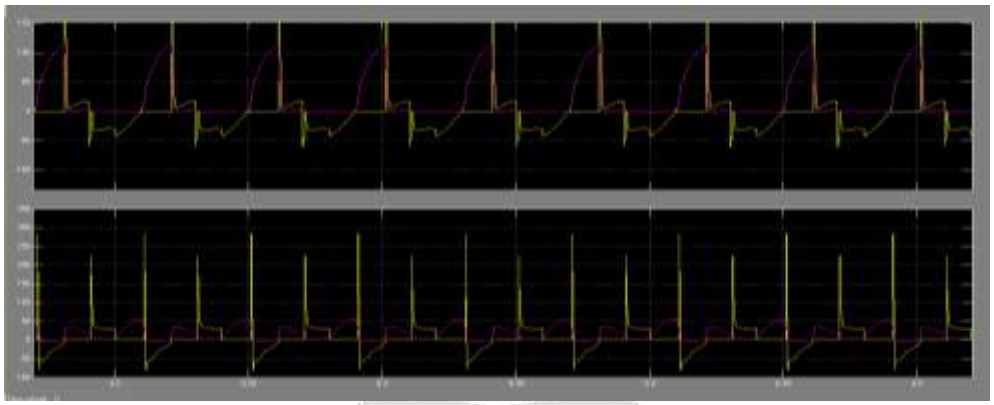

Fig-13: switch voltages and currents

4.2 Buck mode

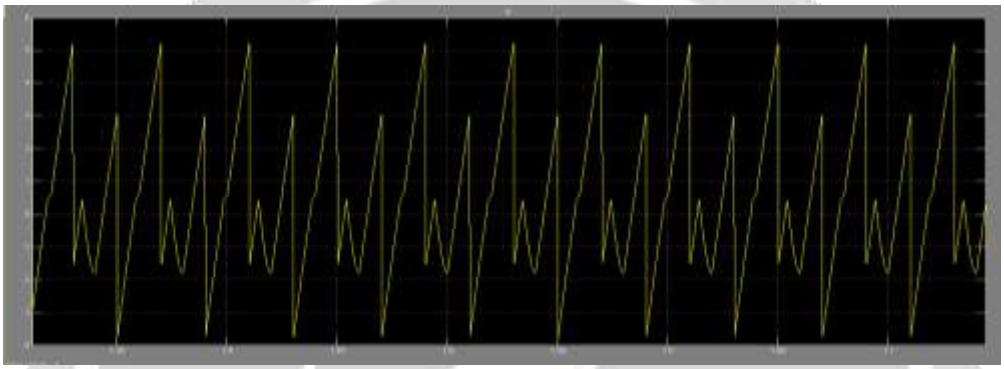

Fig-14: Current through input inductor

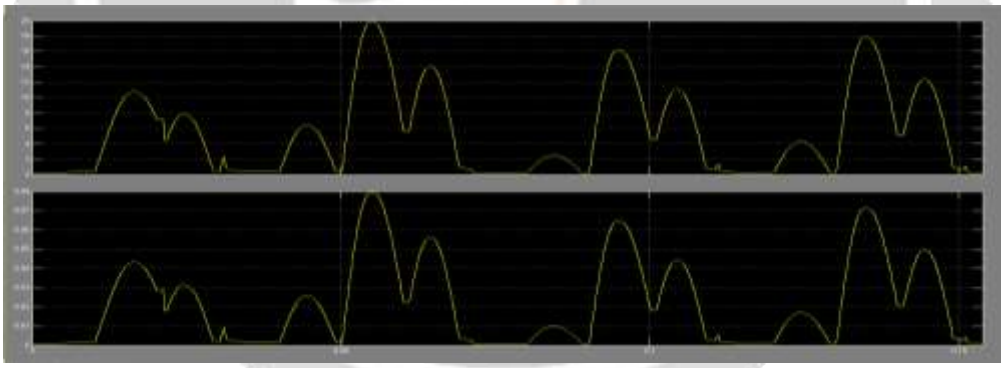

Fig-15: output voltage and current

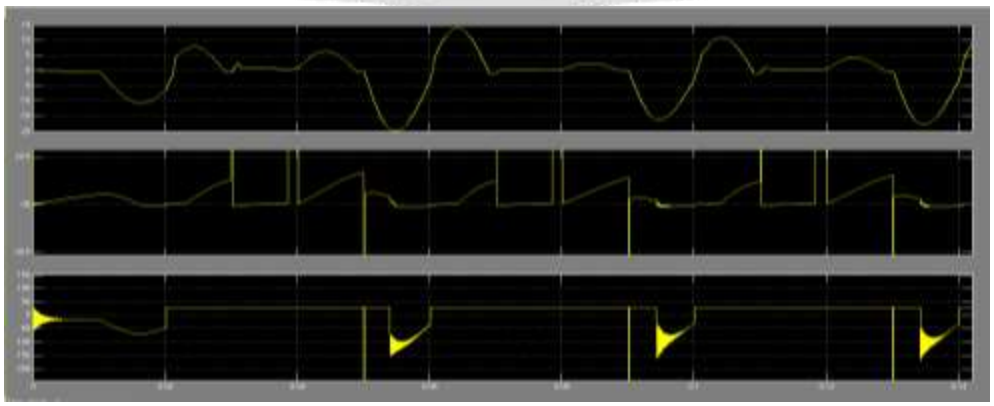

Fig-16: transformer voltages

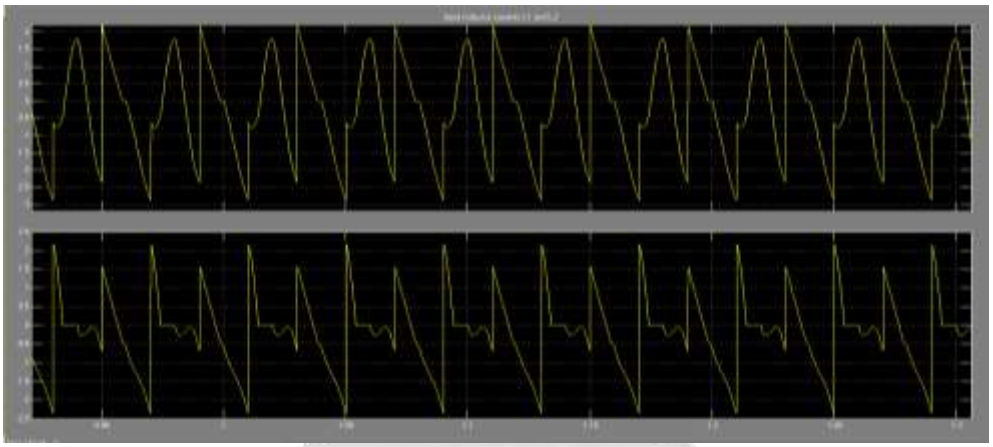

Fig-17: current through parallel inductors

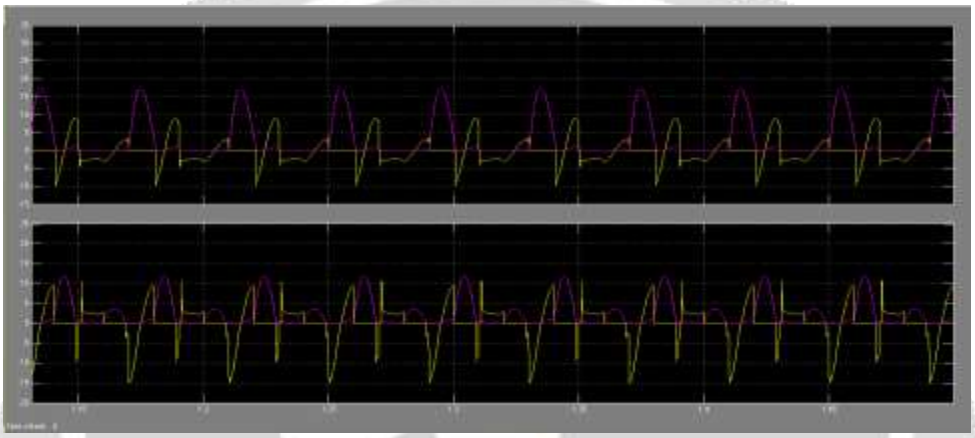

Fig-18: voltage and current through the switch S1 and S2 of rectifier

5. CONCLUSIONS

A soft-switching snubberless bidirectional current-fed isolated push–pull dc/dc converter for application of the ESS in FCVs. A novel secondary-side modulation method is proposed to eliminate the problem of voltage spike across the semiconductor devices at turn-off. The above claimed ZCC and NVC of primary devices without any snubber are demonstrated and confirmed by the simulation and experimental results. ZCS of primary-side devices and ZVS of secondary-side devices are achieved, which reduces the switching losses significantly. Soft-switching is inherent and is maintained independent of load. Once ZCC, NVC, and soft switching are designed to be obtained at rated power, it is guaranteed to happen at reduced load unlike voltage-fed converters. Turn-on switching transition loss of primary devices is also shown to be negligible. Hence, maintaining soft switching of all devices substantially reduces the switching loss and allows higher switching frequency operation for the converter to achieve a more compact and higher power density system. Proposed secondary modulation achieves natural commutation of primary devices and clamps the voltage across them at low voltage (reflected output voltage) independent of the duty cycle. It, therefore, eliminates requirement of active-clamp or passive snubber.

6. REFERENCES

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