DESIGN & ANALYSIS OF A 920-MHz LOW POWER OPTIMIZED LOW NOISE AMPLIFIER FOR RFID APPLICATIONS

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ABSTRACT

An optimized 920-MHz UHF band power optimized LNA is presented here, which can be used for RFID application works on UHF bands. Here main parameters of amplifier are analyzed which can be used for designing any transceiver system. Described LNA is simulated using NGSPICE simulator with BSIM 4.7.0 CMOS technology file, and the size of used MOS is 20nm which is very small compared to other works nowadays. This LNA achieves forward gain (S_{21}) ≈ 21.5db and an input power reflection (@920MHz) of ≈ -34db.It is power optimized LNA which works on 0.7V voltage supply. It has low pass band noise factor of around 1.10dB.

Keyword: *-LNA, Impedance Matching, Noise Figure, Tank Circuit, Transconductance.*

1. INTRODUCTION

RADIO-FREQUENCY IDENTIFICATION (RFID) is a growing intelligent wireless tracking system for information on goods, animals and even humans in transit [1]. An RFID application needs two main part for working, A reader and A transponder [2] which is called tag. Generally the front end required a LNA which is works on narrow band and particularly if it is working on UHF band then it can be used with larger tracking distance area as UHF bandwidth is large compared to high radio frequency. Despite wider application scope and more advanced functionality, the development of RFID is still restricted by its high fabrication cost and weak process compatibility [3] Though In recent years many research is done in this area so nowadays it's been cost-effective system. LNA designed for UWB frequency from 2-10 GHz has been reported by author [4], [5] and also for UHF band work is done by authors [1], [6], [7]. UHF RFID reader front ends in the 860 to 960 MHz range was addressed in [1]. So designing for particular band is challenging task. There are main three parameters which have to consider for design process which are noise, impedance matching and power dissipation. Major difficult part is to simultaneously consider all of this three parameters which works simultaneously and efficiently. For that there are many technology is used for designing which are simultaneous noise and impedance matching (SNIM) [8], power-constrained noise optimization [9], and power-constrained simultaneous noise and input matching (PCSNIM) [1]. The above approaches lacked mutual consistency. Hence, the authors in [1], [16], [17], provided an integrated analysis of the above narrow-band LNA optimization techniques based on a consistent set of noise and matching expressions. However work done by author [1] is satisfied but as new advanced technology files are available this paper improves authors work and with some advanced modification gives good LNA which works on 920-MHz frequency band, which is approved for RFID application in many countries. So by this re-evaluation of author [1] work is improved though here we neglected the channel transconductance g_{ds} which can be evaluated by future work.

2. OPTIMIZED RFID LNA DESIGN

Here telescopic inductive source degeneration topology is used for designing a 920-MHz UHF band LNA. This is because the telescopic cascode is inherently a current reuse structure and consumes less bias current than the folded cascade [1]. Below in fig. 1 illustrated a proposed LNA design. Here M1 is main CMOS as it is first part of LNA and noise mostly depends on first stage of system, for proposed LNA M1 is input source degenerated amplifier device which generates noise free resistive component looking into the gate, Which is used for resistance matching from source for maximum power transfer to the system. Ce is external capacitor for facilitate low power matching.

Lg is external inductor at gate terminal facilitate complex conjugate for input reactance matching. Also Ld, Cd and Rd at the output terminal of M2 are creating a tank circuit which is carefully tuned at particular 920-MHz frequency. Also the value of Cd and Ld is carefully chosen to prevent detuning by parasitic components of M2 CMOS. Two capacitors at input and output are ac-coupling capacitors and Cb is ac grounding capacitor at gate of M2 CMOS. Here M3 CMOS is mainly used for supplying current to the LNA which is basically work as current mirror of M1. Large resistance Rref at the drain of M3 CMOS controls the bias current to the telescopic LNA while large resistor Rb decoupled any noise or ac component produced at the M3 to its current mirror M1 CMOS.

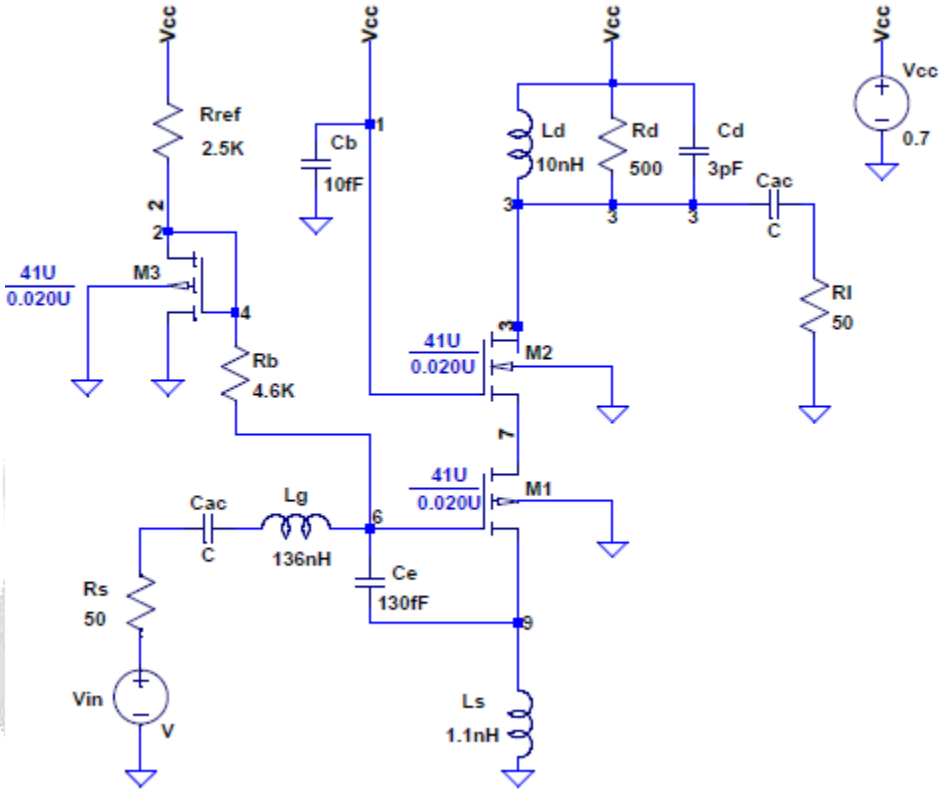

Fig-1: Proposed low power constrained 920-MHz UHF band LNA

Also, Fig. 2 shows the noise inserted circuit diagram of the RFID LNA front end which accounts for the major noise components contributing to the short circuit output noise current at the drain of M1.Thermal noise of resistances, Drain current noise and induced gate noise are the different noise sources of LNA components from which Drain current noise and induced gate noise are the significant noise components in the LNA circuit[1].The power spectral densities of each individual source are as follows: In all the noise expressions, K is the Boltzman constant, and T is the ambient temperature in Kelvin.
The induced gate noise is given by,

$$\overline{I^2_{nG,m1(f)}} = 4KT\delta_1 g_{g1}$$

Where g_{g1} can be expressed as

$$g_{g1} = \frac{\omega^2 C^2_{gs1}}{5g_{d01}} = \frac{\omega^2 \alpha_1 C^2_{gs1}}{5g_{m1}}$$

Where, $\delta 1$ and $\alpha 1$ depend on the channel length of the device M1.

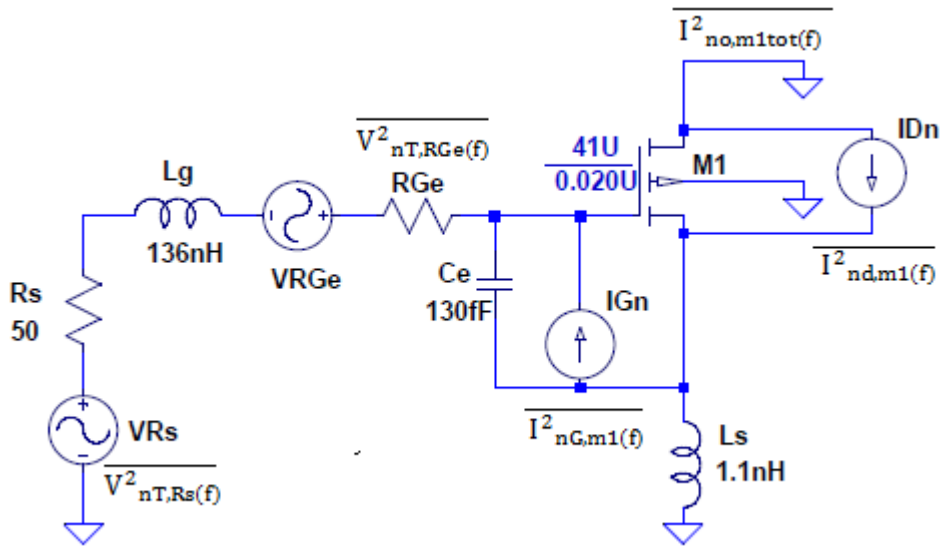

Fig-2: Proposed LNA Noise equivalent circuit of first stage

The drain current noise is given by,

$$\overline{I^2_{nd,m1(f)}} = 4KT\gamma_1 g_{go1} = 4KT\frac{\gamma_1}{\alpha_1} g_{m1}$$

Where, the noise parameter γ_1 also depends on the channel length of M1.

Also, the parameter α_1 is given by,

$$\alpha_1 = \frac{g_{m1}}{g_{go1}}$$

With g_{go1} being the zero-bias drain-to-source (channel) conductance for M1 [1]

The correlation factor, $c1$ between the induced gate noise and the drain current noise for M1 is given by,

$$c_1 = \frac{\overline{I_{ng,m1(f)} I^*_{nd,m1(f)}}}{\sqrt{\overline{I^2_{ng,m1(f)}} \overline{I^2_{nd,m1(f)}}}}.$$

The other noise sources include the thermal noise of the source resistance, which is given by,

$$\overline{V^2_{nT,Rs(f)}} = 4KTR_s \;\&\; \overline{V^2_{nT,RGe(f)}} = 4KTR_{Ge}$$

Noise figure (NF) is the ratio of the total output noise power to the output noise power due to the input source (the noise factor) expressed in dB [10].

3. Design methodology

Here, Power constrained simultaneous Noise & Impedance matching technique is used for designing of LNA. In which both main parameters are considered at a time. As we are using very small CMOS with highly supply voltage, big external capacitor Ce is used to achieve minimum NF Fmin & impedance matching under low power dissipation. One advantage derived as a byproduct of this capacitive device size compensation is the capacitive transformation [11] of the poly gate resistance of M1 CMOS to a lower value resulting in lower line drop in the input circuit, which shown by fig.3.

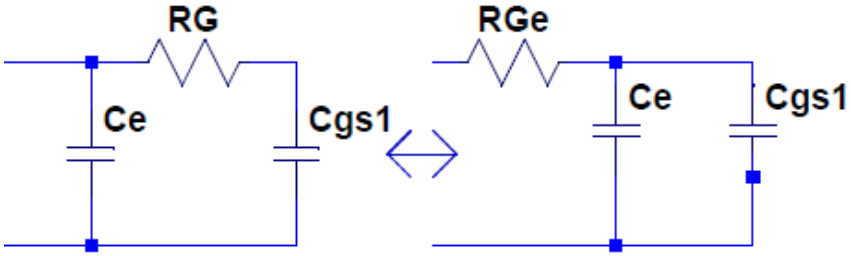

Fig-3: Capacitive transformation of *R*G due to the addition of Ce across M1 [1]

Simplification of gate resistance Rg to RGe given by,

$$RG_e = R_G \frac{C^2_{gs1}}{(C_{gs1}+C_e)^2}$$

Where Cgs is gate to source capacitances of M1. By rewriting induced gate noise expression,

$$\overline{I^2_{nG,m1(f)}} = 4KT\delta_{mod}\frac{\omega^2\alpha_1 C^2_{gs1}}{5g_{m1}}$$

$$\text{Where, } \delta_{mod} = \delta_1\frac{C^2_{gs1}}{C^2_t} \quad \& \quad C_t = C_{gs1} + C_e$$

Now, the theoretical Fmin given by [12],

$$F_{min} \cong 1 + \frac{2}{\sqrt{5}}\frac{\omega C_{gs1}}{g_{m1}}\sqrt{\delta_1\gamma_1(1-|C_1|^2)}$$

Requires the optimal impedance (Zopt) for noise match, with this low-power constraint, to be approximately given by [12], [13]

$$Z_{opt} = \frac{\alpha_1\sqrt{\frac{\delta_1}{5\gamma_1}(1-|C_1|^2)} + j\left(\frac{C_t}{C_{gs1}} + \alpha_1|C_1|\sqrt{\frac{\delta_1}{5\gamma_1}}\right)}{\omega C_{gs1}\left\{\frac{\alpha_1\delta_1}{5\gamma_1}(1-|C_1|^2) + \left(\frac{C_t}{C_{gs1}} + \alpha_1|C_1|\sqrt{\frac{\delta_1}{5\gamma_1}}\right)^2\right\}}.$$

The input impedance of the LNA (ignoring finite output impedance) can be derived as,

$$Z_{in} \cong sL_s + \frac{1}{sC_t} + \frac{g_{m1}}{C_t} * L_s$$

If we consider finite output impedance at resonant than Re(Z_{in}) typically changed 6-12% [1]. Here $C_e(C_t - C_{gs1})$ & L_s facilitate to choose appropriate values for input impedance matching. Also above equations are valid for small value of L_s.

Now to achieve impedance matching source resistance & the matching reactance near the source (L_g) must transform the impedance at the source to Z_{opt}.

Hence by [1],

$$R_s \cong \frac{\alpha_1\sqrt{\frac{\delta_1}{5\gamma_1}(1-|C_1|^2)}}{\omega C_{gs1}\left\{\frac{\alpha_1\delta_1}{5\gamma_1}(1-|C_1|^2)+\left(\frac{C_t}{C_{gs1}}+\alpha_1|C_1|\sqrt{\frac{\delta_1}{5\gamma_1}}\right)^2\right\}} \quad \& \quad sL_g \cong \frac{j\left(\frac{C_t}{C_{gs1}}+\alpha_1|C_1|\sqrt{\frac{\delta_1}{5\gamma_1}}\right)}{sC_{gs1}\left\{\frac{\alpha_1\delta_1}{5\gamma_1}(1-|C_1|^2)+\left(\frac{C_t}{C_{gs1}}+\alpha_1|C_1|\sqrt{\frac{\delta_1}{5\gamma_1}}\right)^2\right\}} - sL_s.$$

At deep Nano metric channel lengths, the value of $\frac{\delta_1}{\gamma_1} \approx 2$, $\alpha_1 < 0.9$ & $|C_1| < 0.395$ as drain & gate noise correlation reduces with deep nano-metric scaling.
So by simplification of above equations we got,

$$R_s \approx \frac{\alpha_1 \sqrt{\frac{\delta_1}{5\gamma_1}(1-|C_1|^2)}}{\omega \frac{C^2_t}{C_{gs1}}} \qquad ..(A)$$

$$sL_g \approx -\frac{1}{sC_t} - sL_s \qquad ..(B)$$

Now for SNIM, the source impedance must be the complex conjugate of Zin. So that the real & Imaginary parts in have equivalences, so

$$\frac{g_{m1}}{C_t} * L_s = R_s \qquad ..(C)$$

$$sL_s + \frac{1}{sC_t} = -sL_g \qquad ..(D)$$

For PCSNIM, eq. (A)–(D) must be satisfied, in which we have ignored finite output impedance of CMOS M1.Here the described LNA design, the steps followed are, first we select Ls as low as possible with particular supply DC voltage. The DC voltage is selected in the way that power constraint PC (=I_{bias} * Vdd) will be minimum from that we have to optimized value of g_{m1}, w_1, & C_{gs1} & checked for particular frequency at the output. Also equation [A]-[D] must be satisfied with values of different component used. With this particular S-parameters specially S21(forward gain), S11(input power reflection) & Fmin must be checked. The tank circuit must be tuned with the selected frequency. For this all values are chosen here is Ls = 1.1nH while Ce = 130fF. Ld, Cd & Rd for tank circuit are chosen 10nH, 3pF & 500Ω respectively so circuit is tuned at particularly 920-MHz frequency. If we consider the finite channel transconductance g_{ds} than Ce value will be lower by approximately 10% of its regular value.

4. Simulation results & Comparisons :-

Here we are using NGSPICE simulator for simulation of optimized LNA with using BSIM 4.7.0 technology file available by Berkeley. BSIM CMOS technology file we used is supported from 10nm to 100nm length CMOS. Here we simulate our LNA with 0.7V dc voltage and using 20nm CMOS. The s-parameter simulation results are as follows:

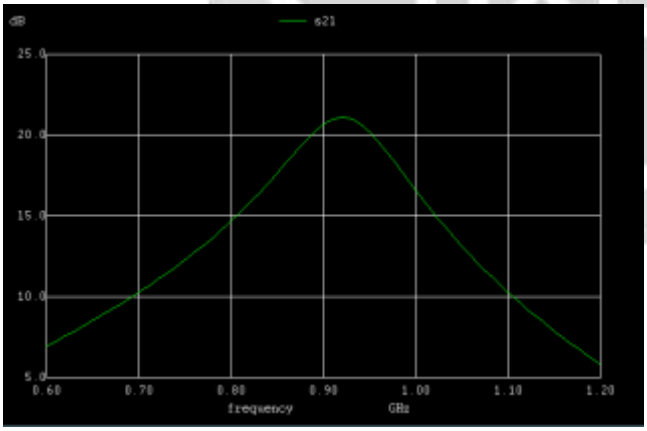

Fig-4: S21 (Forward Gain) simulation of Proposed LNA

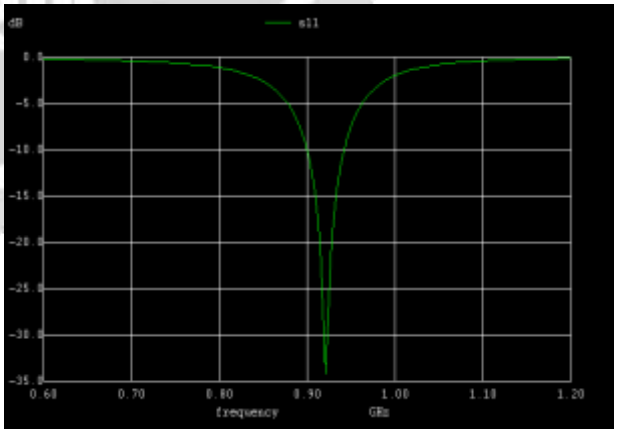

Fig-5: S11 (input power reflection) simulation of Proposed LNA

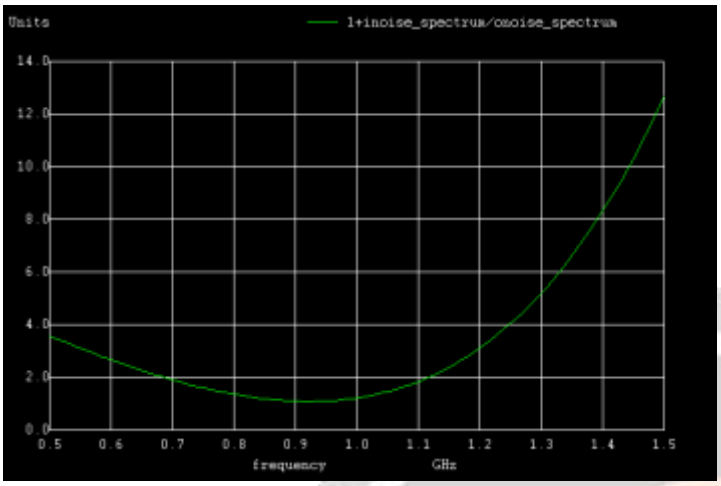

Fig-6: Noise Figure simulation of Proposed LNA

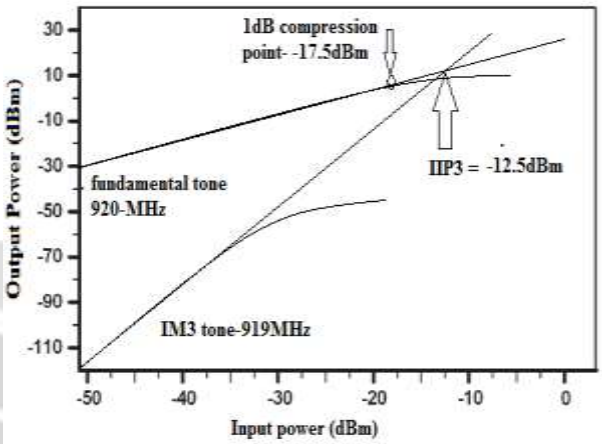

Fig-7: IIP3 & P1db Compression point simulation of Proposed LNA

	CMOS process technology (nm)	S11 (dB)	S21 (dB)	S12 (dB)	Noise Figure (dB)	IIP3 (dBm)	P1dB (dBm)	DC supply (Volt)	Center frequency (f_o-MHz)
This work	020	-34	21.5	-32	1.10	-12.5	-17.5	0.7	920
ISDTC[1]	130	-30	17	-34	2.2	-11.5	-16.1	0.7	866
FCT[14]	250	-18	12	N/A	1.35	-4	-15	1.25	900
CGT[15]	350	-11	13.4	N/A	3.2	10.8	1.4	3	900
DT[08]	180	N/A	15	N/A	2.9	N/A	-15	1.8	900

TABLE-1: Summary of the 920-MHz UHF RFID LNA performance & comparisons with previous papers

4. CONCLUSIONS

This paper presents power optimized low noise amplifier which works on 920-MHz center frequency with 0.7V dc voltage source. This LNA can be used for RFID application. Though many research is required in this research as CMOS used here is of 20nm size only, So this required many more research. Also this design may be reconsidered with using finite gate transconductance which gives better accurate result.

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