

# Design and implementation of enhanced LECTOR technique for low power consumption in CMOS VLSI circuit: A Review

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## ABSTRACT

*With shrinking technology, power management is becoming an important factor for almost every design and application. The key challenges in deep sub micrometer technology are reducing the power consumption and overall power management on the chip. At the very early stage power management needs to be considered. Also, at every design stage low-power technique should to be employed, from RTL to GDSII. This paper describes various techniques for low power VLSI circuits. Future challenges that must be met with designers is to design low power high performance circuits.*

**Keywords:** CMOS, Lector, Sleep, Stack, Sleepy Stack, nMOS, pMOS, Dual Stack, Low power consumption, delay

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## 1.INTRODUCTION

These days, due to the advancement of handheld and battery-based devices with limited power capabilities, the major requirement are power efficiency and power-delay product. These two factors are of greater importance to the electronics designer. In the VLSI circuit design, power consumption of the circuit is of major concern. Development of mobile application alone has not lead to the demand for low power devices. The problem of power consumption is a major issue due to the evolution of mobile era. To overcome the problem of power dissipation, numerous techniques and procedures has been developed by researchers. But there is no standard technique or approach to address this problem. The designer needs to select the most appropriate technique taking into consideration the application requirements and product.

## 2.Literature Survey

Literature survey is an important part of the project. It enables assimilation of knowledge required for the project right from the problem definition, finding a solution for the same and its execution. The following section summarizes the literature survey carried out for the project.

**2.1.Firdous *et al* [1]** have proposed lector-based stack approach for power consumption minimization. Less delay compared to forced stacking during overcome this sleep transistor need control circuit. In proposed design circuit the main concept is charge sharing and recovering of stored charges between output capacitor and capacitance nodes.

**2.2.Saini and Mehra** [2] proposed designs have low delay, good performance, and these techniques are also more area efficient than the existing techniques and are having small leakage current. The proposed technique variable body biasing with bypass is power efficient as well as it is providing more maximum current than base.

**2.3.Barua** [3] in this paper has proposed Common Vdd and Gnd technique compared with well-known low leakage techniques. Hence, this paper explores the experimental results for general logic circuits and then for SRAM cell design. Moreover, Common Vdd and Gnd Technique compares in terms of power, delay and area.

**2.4.Hari** [4] in this paper a novel low-power design technique is proposed to minimize the standby leakage power in cmos VLSI systems by generating the adaptive optimal reverse body-bias voltage. In order to minimize the leakage power dissipation, several circuit techniques have been proposed, such as multi-threshold voltage cmos and variable threshold voltage cmos using variable substrate bias voltage.

**2.5.Anjana and Somkuwar** [5] proposed a technique for minimizing sub threshold leakage current using stacked sleep technique in microwind eda tool was used for the layout and the simulation of two input NAND gate.

**2.6.Sivakumar et al** [6] has proposed Recent Trends in Low Power VLSI Design though there are different types of power consumption, the major types that affect CMOS circuits are dynamic power and leakage power. . The two most common traditional, mainstream techniques are clock gating and multi  $V_{th}$  optimization.

**2.7.Hanchate et al** [7] the lector technique was implemented and tested on MCNC'91benchmark circuits. First, theMCNC'91benchmark netlists were converted to BLIF using a script.

**2.8.Park et al** [8] in Sleepy Stack Reduction of Leakage Power has compared five design approaches in terms of power consumption (dynamic and static), delay and area. To show that the sleepy stack approach is applicable to general logic design, chosen three generic circuits: (i) a chain of 3 inverters, (ii) a 4-input multiplexer and (iii) a 4-bit adder.

### 3.PREVIOUS WORK

#### 3.1 SLEEP

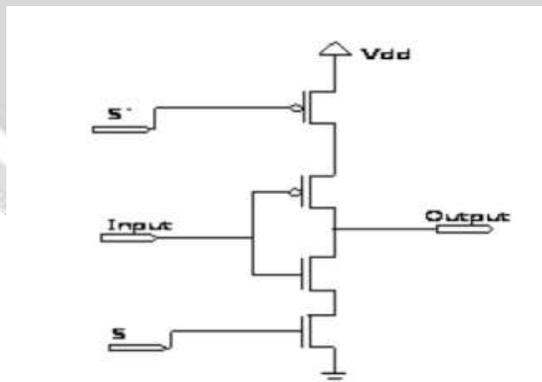


Figure 1

Sleep technique is one of the traditional approaches for sub threshold leakage power reduction. In sleep approach 2 additional transistors are added between V<sub>DD</sub> and V<sub>SS</sub>. Sleep transistor can either be pmos or nmos. A pmos sleep transistor is placed between V<sub>DD</sub> and pull up circuit and a nmos sleep transistor between pull down and ground. This type of circuit is called as gated V<sub>DD</sub> and gated gnd. The sleep transistors are turned off when the circuits are not in use. They turn off the circuit by cutting off the power rails. During the sleep mode, it dramatically reduces the leakage power, but the additional sleep transistor increases the area and delay. During the active mode the circuit provides very low resistance in the conduction path and these additional transistors have no effect on the

performance of the circuit. In standby mode the transistors will be made to turn off, thus reducing the leakage power in the circuit. Thus, leakage power can be reduced effectively by switching off the power source. Furthermore, the pull-up and pull-down circuit will have floating values and thus will lose their state during sleep mode. These values significantly impact the wake-up time and energy of the sleep technique due to the requirement to recharge the transistors which lose their state during the sleep mode.

### 3.2. DUAL SLEEP

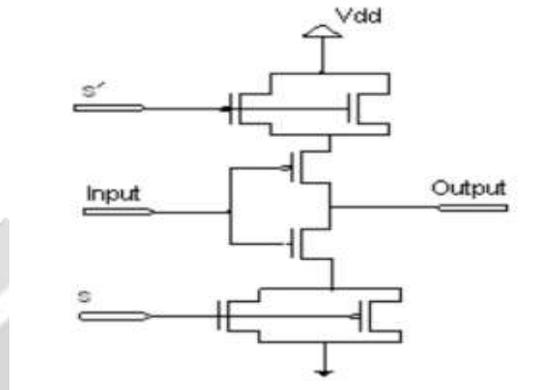


Figure 2

In dual sleep approach it uses two extra pull up and two extra pull-down transistors in sleep mode either in off state or in ON state, here one of the sleep transistors is used to turn on in ON state and the other one is used to turn on the OFF state. In both active and inactive mode, the 2 sleep transistors are always ON in both pull-up and pull-down network. Thus, there is a connectivity to the with the gnd and VDD. This technique has an excellent trade-off between power, delay and area. The dual sleep circuit can be made common to all the logic circuits; thus, a smaller number of transistors are needed to apply a certain logic circuit. When  $S=1$  the pull down NMOS transistor is ON and the pull-up PMOS transistor is ON since  $s'=0$ . So, in OFF state a PMOS is in series with an NMOS both in pull-up and pull-down circuit which then reduces power.

### 3.3. SLEEPY STACK

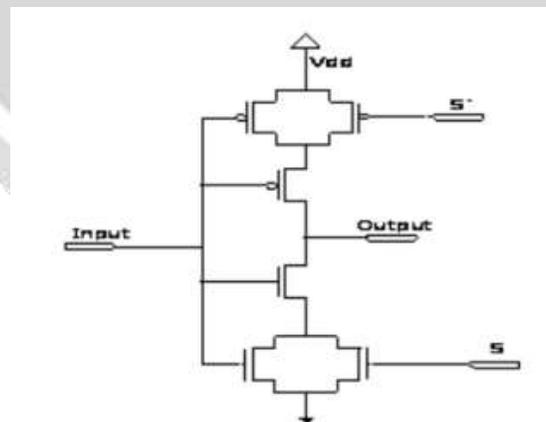


Figure 3

The figure 3 shows, sleepy stack technique applied to CMOS inverter. The Sleepy stack technique combines the sleep transistor in active mode with the stack affect during sleep mode. In this technique, existing transistors is divides into two transistors of equal width (i.e.,  $W1 = W2/2$ ). Then sleep transistor is connected in parallel to one of the transistors in each set of two stacked transistors. All sleep transistors are turned on during active mode when  $S=0$  and  $S=1$ . Due to the added sleep transistor, the resistance through the active path decreases, which in turn decreases

the propagation delay. When in sleep mode,  $S=1$  and  $S=0$  are asserted, and both of the sleep transistors are turned off. Leakage current is suppressed by the stacked transistors in the sleepy stack technique.

### 3.4. FORCED STACK

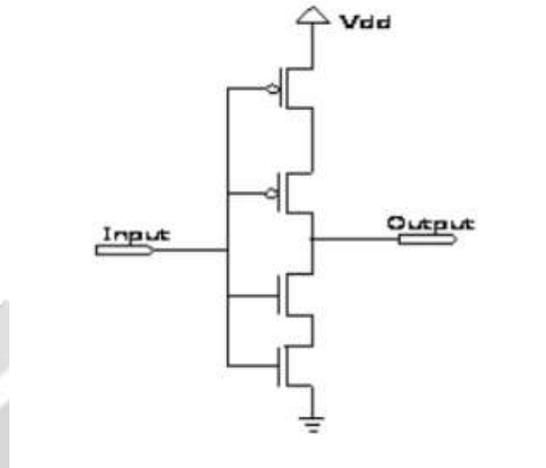


Figure 4

Forced stack technique exploits the stack effect of transistors and reduces the leakage. This happens due to the reduction of the gate to source voltage and reduction of DIBL coefficient due to lower drain to source potential thereby further reducing leakage. Forced stack technique fails in saving power consumption in standby mode. Finally, MTSC Stack technique is a combination of MTCMOS, SCCMOS and Forced Stack techniques. In MTSC Stack technique power consumption is reduced in active mode and retains the exact logic state in sleep mode. Operation of MTSC Stack technique is similar to the MTCMOS technique where the sleep transistors are turned on during active mode and turned off during sleep mode.

### 3.5. SLEEPY KEEPER

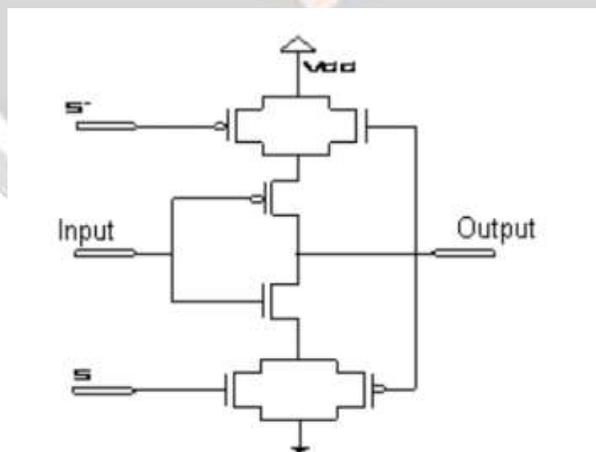


Figure 5

The figure 5 shows, Sleepy keeper technique applied on two input CMOS circuit. In the schematic of traditional CMOS nand gate, the transistors are used only in the most efficient way possible. NMOS transistors are connected to Gnd and PMOS transistors are connected to  $V_{dd}$ , this is where the basic problem lies. As we know that Gnd or logic 0's are not efficiently passed by PMOS transistors; similarly,  $V_{dd}$  or logic 1's is not efficiently passed by NMOS transistors. However, given that the value '1' is already been calculated to maintain a value '1' in sleep mode.

The sleepy keeper approach uses this output value '1' and an NMOS transistor that is connected to the  $V_{dd}$ , to maintain the output value which is equal to '1' when in sleep mode. As shown in the Figure, an additional NMOS transistor is placed in parallel to the sleep transistor in pull-up circuit which connects to the  $V_{dd}$ . When in sleep mode, this NMOS transistor becomes the only source of  $V_{dd}$  to the pull-up network since the sleep transistor is in the off state. Similarly, given that the value '0' is already been calculated to maintain a value '0' in sleep mode. The sleepy keeper approach uses this output value '0' and a PMOS transistor connected to  $Gnd$  to maintain the output value equal to '0' when in sleep mode. As shown in Figure (), an additional PMOS transistor is placed in parallel to the sleep transistor in pull-down circuit which connects to the  $Gnd$ . Now this additional PMOS transistor becomes the only source of  $Gnd$  to the pull-down network, which is the dual case of the output '1' case explained above

### 3.6. SLEEPY STACK WITH LECTOR

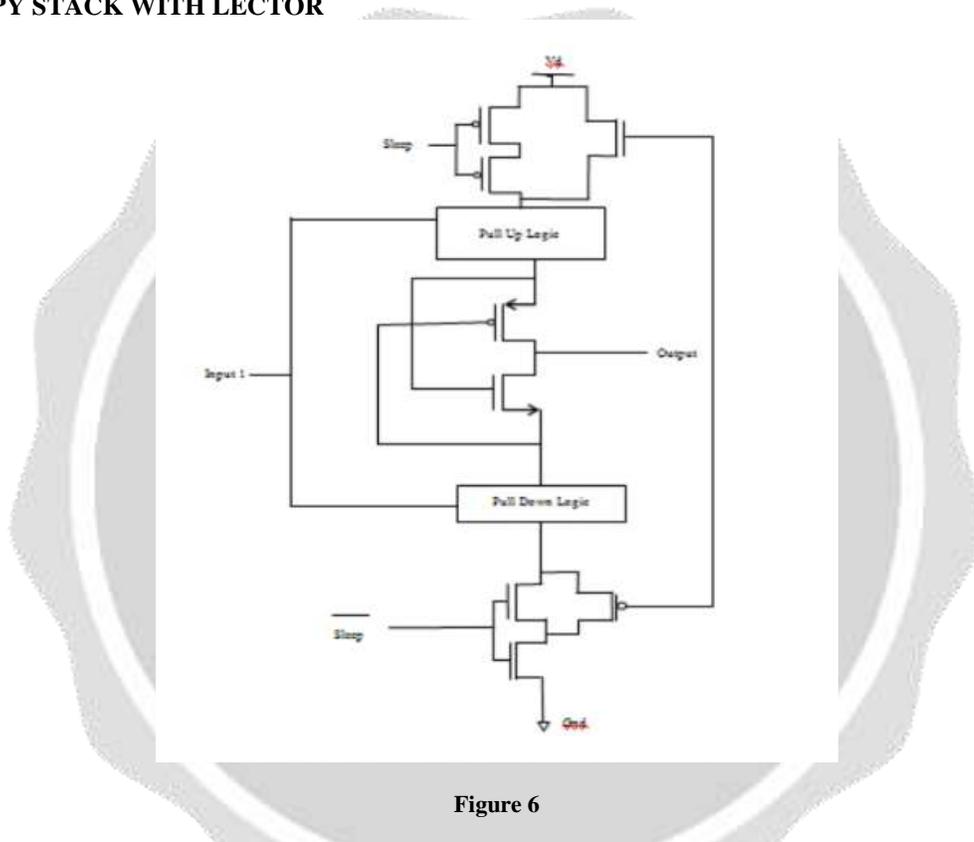


Figure 6

It consists of a pull up and pull-down circuit which is separated by a pmos and a nmos transistor. The circuit diagram is shown in figure.2. The aspect ratio of  $W/L=2$  in case of PMOS circuit transistor and in NMOS transistor the aspect ratio is of  $W/L = 1$ . Through the minimal aspect ratio the circuit sub-threshold value reduces. In this technique, the sleep transistors are used for differentiation of power supply and ground, and the remaining transistor is connected to the gate terminal. It depends on the input vector and the switching of the sleep transistors, that consumes power in both the active state and idle states. Further, the two transistors are added in logic circuit based on the Pull-up and pull-down design network circuit. This design will provide a path resistance for ground to supply connection. This resistance will provide a minimum leakage current in the circuit. The designed circuit performs effectively for both active and standby mode of the circuit design. Furthermore, increase the resistance in the path from source to ground. The system array is designed using transistors  $VCC$  and  $GND$  terminals, hence it is also called as self-controlled voltage technique.

#### 4. SIMULATION AND RESULTS

Sl.No	Techniques	Power (nW)	Delay (nS)	Power delay product
1	Sleep	693	4.2	2.91
2	Dual Sleep	1716	4.02	6.89
3	Sleepy Stack	1057	2.105	2.22
4	Forced Stack	872.5	0.131	11.4
5	Sleepy Keeper	928.4	2.19	2.03
6	Sleepy Stack with lector	609.8	4.136	2.522

**Table 1**

In this work, different designs of nand gate are implemented in CMOS process with 180nm technology. The average powers are compared with and without the power reduction techniques. The simulation results of nand gate with and without power reduction technique are given in Table.1

#### 5. CONCLUSION

We have demonstrated a new approach to low power optimization of digital static CMOS circuits. The assignment is performed in such a way that subsequent optimization for low power operation yields a significant reduction in the total power consumption of the circuit. It is demonstrated that with technology scaling the contribution of gate leakage and subthreshold leakage relative to the total leakage in an “off” transistor varies. It is observed that as the gate leakage becomes a significant component of total leakage, the traditional stacking technique to reduce subthreshold leakage fails to minimize the overall leakage in a circuit. A methodology of input vector selection based on the ratio of gate-leakage to the subthreshold leakage is proposed for reducing the overall leakage of a circuit in the standby-mode of operation. In nanometer scale CMOS technology, subthreshold leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques based upon technology and design criteria. Our novel enhanced sleepy stack with lector which combines the sleep and the stack approaches, is proposed as a new choice for logic designers. Furthermore, the enhanced sleepy stack with lector is applicable to single and multiple threshold voltages. In conclusion, the enhanced sleepy stack with lector combines some of the advantages of sleep transistors – most notably the effective use of dual- $V^{\text{th}}$  technology – with some of the advantages of the stack approach – most notably the ability to save state and some of the advantage of the lector approach- to reduce the power leakage by increasing the number of off transistors

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