Driving of Three-Phase Systems Using Switching Current Of Rectifiers.

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ABSTRACT

This paper proposes a driving of three phase system composed of parallel single-phase rectifiers, here we use a three-phase AC motor and inverter. The proposed topology permits to reduce the switch currents of rectifier, the harmonic distortion at the input on the converter side, and presents improvements on the fault tolerance characteristics. If we increase in the total number of switches, the total energy loss of the proposed system may be lower than that of a conventional one. The proposed model of the system is derived, and it is shown that the reduction of circulating current is an important objectives in the system proposed design. A suitable control strategy, including the pulse width modulation(PWM) technique, is developed. Experimental results are presented as well.

1.INTRODUCTION:

Several solutions have been proposed when the objective is to supply three-phase motors from a single-phase ac main. It is quite common to have only a single phase power grid in residential, commercial, manufacturing, and mainly in rural areas, while the adjustable speed drives may request a three-phase power grid. Single-phase to three-phase ac–dc–ac conversion usually employs a full-bridge topology, which implies in ten power switches. This converter is denoted here as conventional topology.

Parallel converters have been used to improve the power capability, reliability, efficiency, and redundancy. Parallel converter techniques can be employed to improve the performance of active power filters, uninterruptible power supplies (UPS), fault tolerance of doubly fed induction generators, and three-phase drives. Usually the operation of converters in parallel requires a transformer for isolation. However, weight, size, and cost associated with the transformer may make such a solution undesirable. When an isolation transformer is not used, the reduction of circulating currents among different converter stages is an important objective in the system design.

In this paper, a single-phase to three-phase drive system composed of two parallel single-phase rectifiers and a three-phase inverter is proposed. The proposed system is conceived to operate where the single-phase utility grid is the unique option available. Compared to the conventional topology, the proposed system permits: to reduce

the rectifier switch currents; the total harmonic distortion (THD) of the grid current with same switching frequency or the switching frequency with same THD of the grid current; and to increase the fault tolerance characteristics. In addition, the losses of the proposed system may be lower than that of the conventional counterpart. The aforementioned benefits justify the initial investment of the proposed system, due to the increase of number of switches.
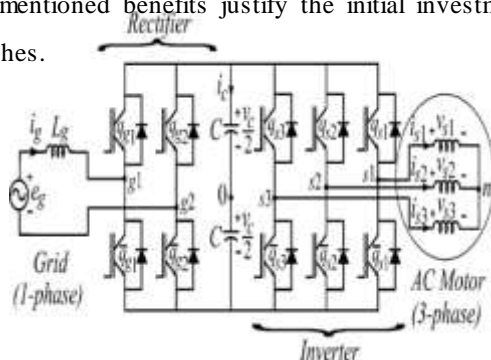

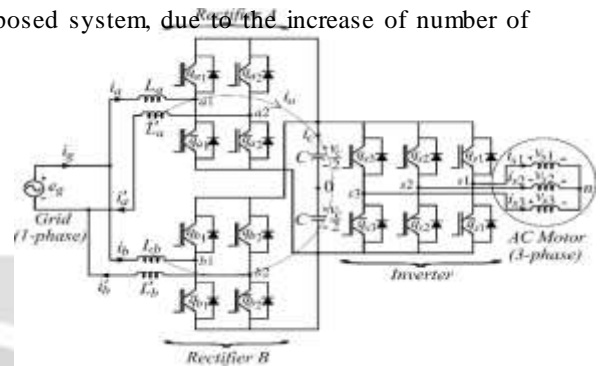Fig. 1.Conventional single-phase to three-phase drive system   Fig. 2.Proposed single-phase to three-phase drive system.

II. SYSTEM MODEL:

The system is composed of grid, input inductors (L_a, L^a, L_b, and L^b), rectifiers (A and B), and capacitor bank at the dc-link, inverter, and induction machine. Rectifiers A and B are constituted of switches q_{a1}, q_{a1}, q_{a2}, and q_{a2}, and q_{b1}, q_{b1}, q_{b2}, and q_{b2}, respectively. The inverter is constituted of switches q_{s1}, q_{s1}, q_{s2}, q_{s2}, q_{s3}, and q_{s3}. The conduction state of the switches is represented by variable s_{qa1} to s_{qs3}, where sq=1 indicates a closed switch while $s_q = 0$ an open one.

From Fig. 2, the following equations can be derived for the front-end rectifier

$$v_{a10} - v_{a20} = e_g - (r_a + l_a p)i_a - (r^a + l^a p)i^a \qquad (1)$$

$$v_{b10} - v_{b20} = e_g - (r_b + l_b p)i_b - (r^b + l^b p)i^b \qquad (2)$$

$$v_{a10} - v_{b10} = (r_b + l_b p)i_b - (r_a + l_a p)i_a \qquad (3)$$

$$v_{a20} - v_{b20} = (r^a + l^a p)i^a - (r^b + l^b p)i^b \qquad (4)$$

$$i_g = i_a + i_b = i^a + i^b \qquad (5)$$

where $p = d/dt$ and symbols like r and l represent the resistances and inductances of the input inductors L_a, L^a, L_b, and L^b.

The circulating current i_o can be defined from i_a and i^a or i_b and i^b, i.e.,

$$i_o = i_a - i^a = -i_b + i^b . \qquad (6)$$

Introducing i_o and adding (3) and (4), relations (1)-(4) become

$$v_a = e_g - [r_a + r^a + (l_a + l^a)p]i_a + (r^a + l^a p)i_o \qquad (7)$$
$$v_b = e_g - [r_b + r^b + (l_b + l^b)p]i_b - (r^b + l^b p)i_o \qquad (8)$$

$$v_o = -[r^a + r^b + (l^a + l^b)p]i_o - [r_a - r^a + (l_a - l^a)p]i_a$$
$$+ [r_b - r^b + (l_b - l^b)p]i_b \qquad (9)$$

where

$$v_a = v_{a10} - v_{a20} \qquad (10)$$

$$v_b = v_{b10} - v_{b20} \qquad (11)$$

$$v_o = v_{a10} + v_{a20} - v_{b10} - v_{b20}. \qquad (12)$$

In order to both facilitate the control and share equally current, voltage, and power between the rectifiers, the four inductors should be equal, i.e., $r^g = r_a = r^a = r_b = r^b$ and $l^g = l_a = l^a = l_b = l^b$. In this case, the model (7)-(9) can be simplified to the model given by

$$v_a + \frac{v_o}{2} = e_g - 2(r_g + l_g p)i_a \qquad (13)$$

$$v_b - \frac{v_o}{2} = e_g - 2(r_g + l_g p)i_b \qquad (14)$$

$$v_o = -2(r^g + l^g p)i_o. \qquad (15)$$

Additionally, the equations for i_g, i^a, and i^b can be written as

$$v_{ab} = \underline{v^a + v^b} = e_g - (r^g + l^g p)i_g \qquad (16)$$

$$v_a - \frac{v_o}{2} = e_g - 2(r_g + l_g p)i_a \qquad (17)$$

$$\frac{v_b + v_o}{2} = e_g - 2(r_g + l_g p)i_b. \qquad (18)$$

In this ideal case (four identical inductors), the circulating current can be reduced to zero imposing

$$v_o = v_{a10} + v_{a20} - v_{b10} - v_{b20} = 0. \qquad (19)$$

When $i_o = 0$ ($i_a = i^a$, $i_b = i^b$) the system model (7)-(9) is reduced to

$$v_a = e_g - 2(r^g + l^g p)i_a \qquad (20)$$

$$v_b = e_g - 2(r^g + l^g p)i_b. \qquad (21)$$

Then, the model of the proposed system becomes similar to that of a system composed of two conventional independent rectifiers.

III. PWM STRATEGY:

The inverter can be commanded by using an adequate pulse width modulation (PWM) strategy for three-phase voltage source inverter (VSI) [19], so that it will not be discussed here. In this section, the PWM strategy for the rectifier will be presented.

The rectifier pole voltages v_{a10}, v_{a20}, v_{b10}, and v_{b20} depend on the conduction states of the power switches, i.e., $v_{j0} = (2s_{qj} - 1)\underline{v_c}$ for $j = a1$ to $b2$ (22)

$$v^a = v^{a10} - v^{a20} \qquad (23)$$

$$v^b = v^{b10} - v^{b20} \qquad (24)$$

$$v^o = v^{a10} + v^{a20} - v^{b10} - v^{b20}. \qquad (25)$$

$$v^{a10} = v^a + v^x \qquad (26)$$

$$v^{a20} = v^x \qquad (27)$$

$$v^x = \mu v^{xmax} + (1 - \mu)v^{xmin}. \qquad (28)$$

When $\mu = 0$, $\mu = 0.5$, and $\mu = 1$ the auxiliary variable v^x has the following values $v^x = v^{xmin}$, $v^x = v^{xave} = (v^{xmin} + v^{xmax})/2$, and $v^x = v^{xmax}$, respectively. When $v^x = v^{xmin}$ or $v^x = v^{xmax}$ a converter leg operates with zero switching frequency.

IV. CONTROL STRATEGY:

Fig. 3 presents the control block diagram of the system in Fig. 2, highlighting the control of the rectifier. The rectifier circuit of the proposed system has the same objectives of that in Fig. 1, i.e., to control the dc-link voltage and to guarantee the grid power factor close to one. Additionally, the circulating current i_o in the rectifier of the proposed system needs to be controlled In this way, the dc-link voltage v_c is adjusted to its reference

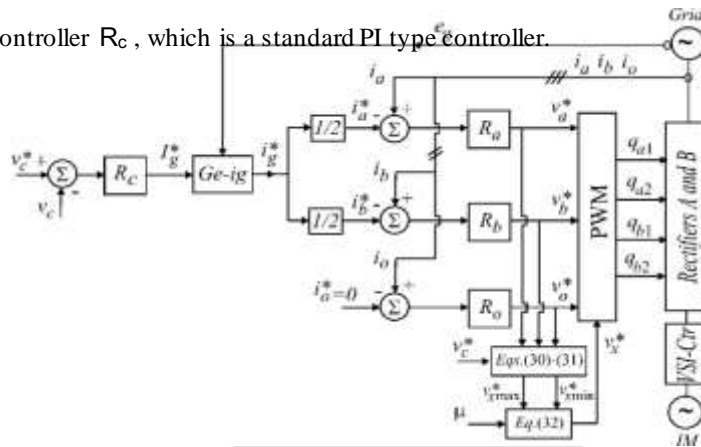value v^c using the controller R_c , which is a standard PI type controller.

Fig. 3.   Control block diagram.

The homopolar current is measured (i_o) and compared to its reference ($i^o = 0$). The error is the input of PI controller R_o , that determines the voltage v^o. The calculation of voltage v^x is given from (30) to (32) as a function of μ, selected as shown in the Section V. The motor there-phase voltages are supplied from the inverter (VSI). Block VSI-Ctr indicates the inverter and its control. The control system is composed of the PWM command and a torque/flux control strategy (e.g., field-oriented control or volts/hertz control).

V. HARMONIC DISTORTION:

The harmonic distortion of the converter voltages has been evaluated by using the weighted *THD* (*WTHD*). where a_1 is the amplitude of the fundamental voltage, a_i is the amplitude of ith harmonic and p is the number of harmonics taken into consideration.

Fig. 4 shows the WTHD of voltages generated by rectifiers [$v_{ab} = (v_a + v_b)/2$ for the proposed configuration and $v_g = v_{g10} - v_{g20}$ for the conventional one] at rated grid voltage as a function of μ.
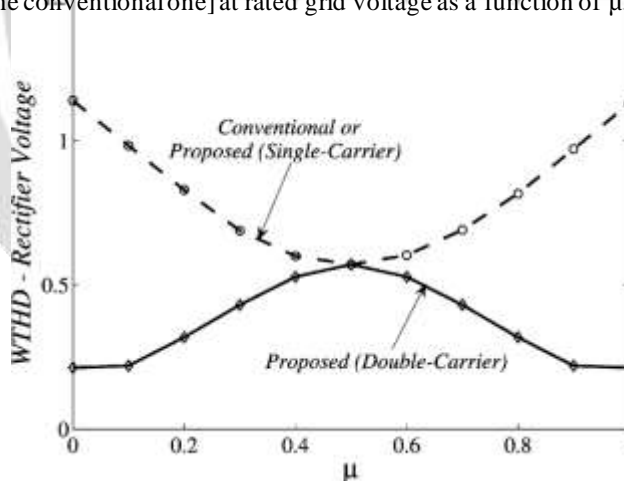

Fig. 4.   *WTHD* of rectifier voltage (v_{ab} for proposed configuration and v_g for standard configuration) as a function of μ.

When the single-carrier PWM is used, the behavior of *WTHD* of the proposed system is similar to that of conventional one for all μ, as observed in Fig. 4. When the double-carrier PWM is used with $\mu = 0.5$, the *WTHD* is also the same for both configurations. However, for the other values of μ the *WTHD* of the proposed system is lower than that of the

conventional one. The *WTHD* of the proposed topology (double-carrier with $\mu = 0$ or $\mu = 1$) is close to 63% of that of
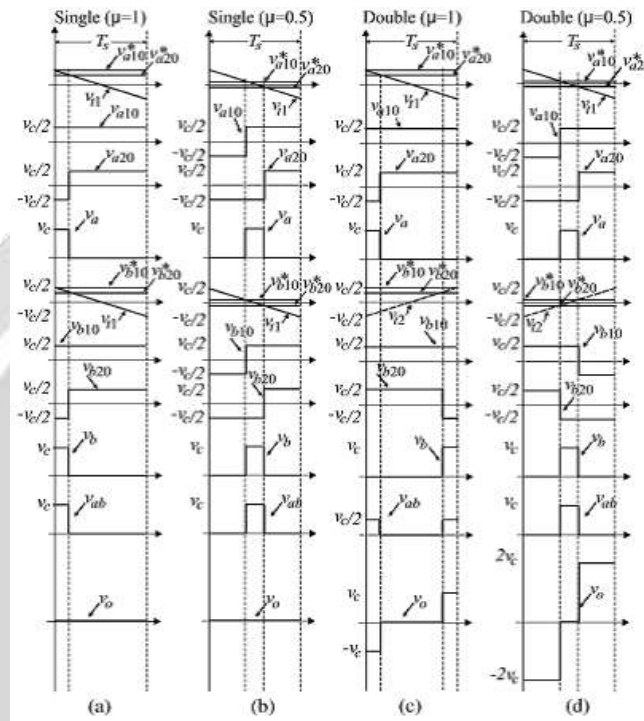
the conventional topology (with $\mu = 0.5$).

Fig. 5. Variables of rectifiers A and B. (a) Single-carrier with $\mu = 1$. (b) Single-carrier with $\mu = 0.5$. (c) Double-carrier with $\mu = 1$. (d) Double-carrier with $\mu = 0.5$.
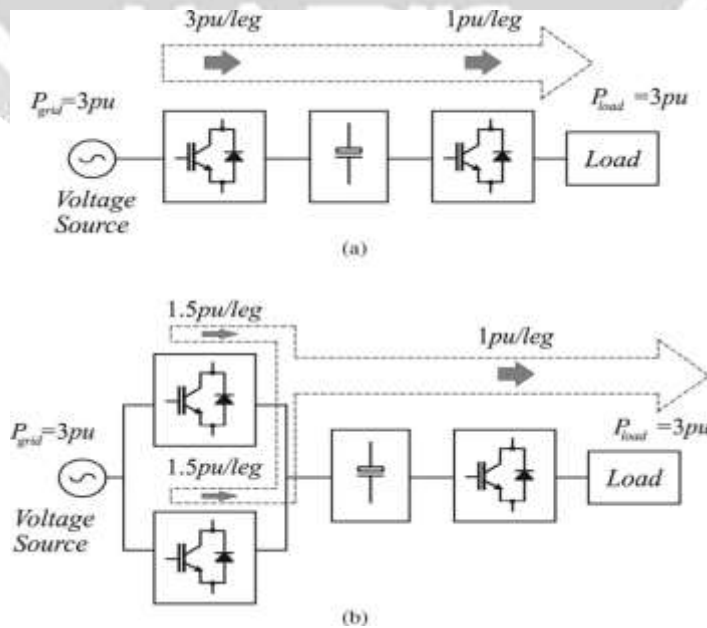
Fig. 7.   Flow of active power. (a) Conventional ac-dc-ac single-phase to three phase converter. (b) Proposed system with two rectifiers.

VI. RATINGS OF SWITCHES:

Assuming same rms voltages at both grid and machine sides, a machine power factor of 0.85 and neglecting the converter losses, currents of the rectifier switches normalized in terms of currents of the inverter switches are 2.55 and 1.27 for the conventional and the proposed single-phase to three-phase con-verter, respectively. Fig. 7(a) and (b) shows the flow of active power in the conventional and in the proposed single-phase to three-phase converter, respectively. For balanced system ($L^g = L_a = L^a = L_b = L^b$), voltage v_o is close to zero, so that the dc-link voltage is equal to that required by the conventional sys-tem. Since the parallel connection scheme permits to reduce the switch currents and preserve the dc-link voltage, the rating of each power switch in the rectifier side is reduced.

VII. DC-LINK CAPACITOR

The dc-link capacitor current behavior is examined in this section. Fig. 8 illustrates the harmonic spectrums of the dc-link capacitor current for the conventional converter ($\mu = 0.5$) [see Fig. 8(a)] and for the proposed converter using single-carrier with $\mu = 0.5$ [see Fig. 8(b)], double-carrier with $\mu = 0.5$ [see Fig. 8(c)] and double-carrier with $\mu = 0$ [see Fig. 8(d)]. The proposed converter using double-carrier with $\mu = 0$ provides the best reduction of the high frequency harmonics Table I (obtained from Fig. 8) presents the *THD* of the dc-link capacitor current of the proposed converter (*THDp*) referred to the *THD* of the conventional converter (*THDc*). The highest reduction of *THD* is obtained for the converter using double-carrier with $\mu = 0$. The *THD* obtained for $\mu = 1$ is equal to that for $\mu = 0$.
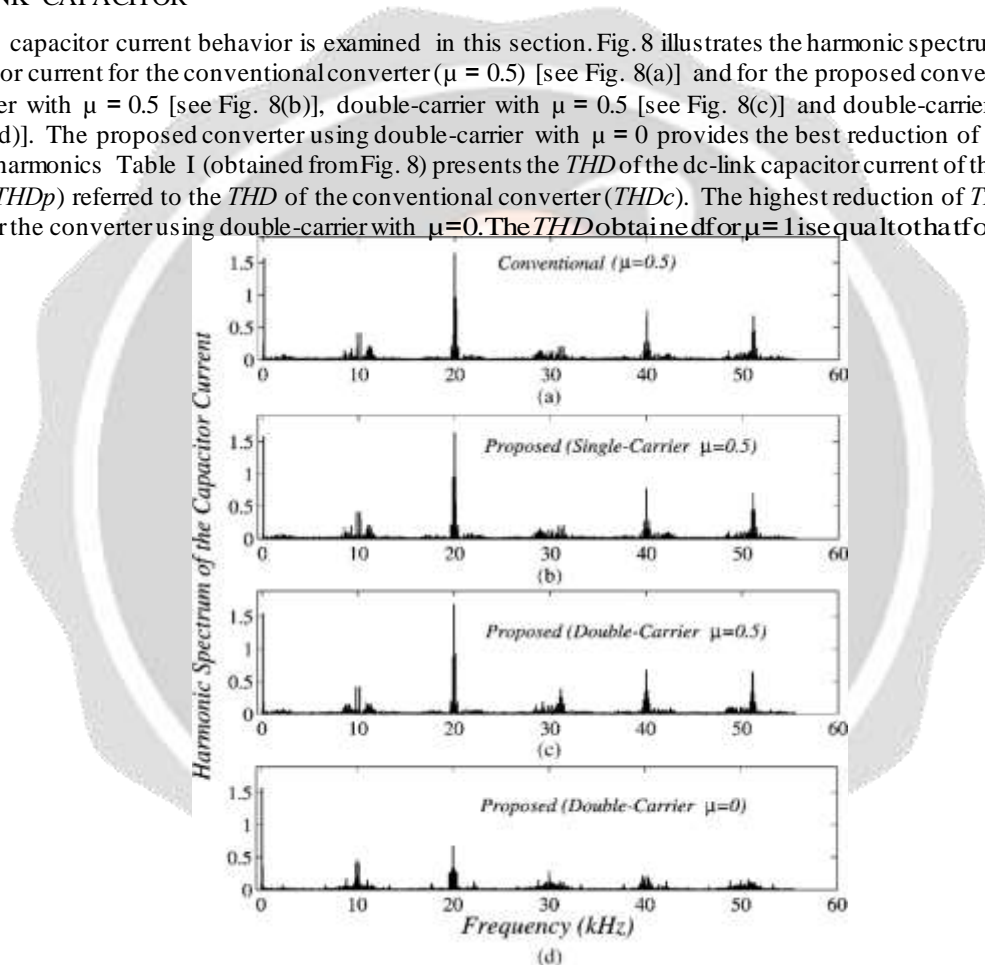

Fig. 8.   Harmonic spectrum of the dc-link capacitor current. (a) Conventional converter ($\mu = 0.5$). (b) Proposed converter with single-carrier ($\mu = 0.5$). (c) Proposed converter with double-carrier ($\mu = 0.5$). (d) Proposed converter with double-carrier ($\mu = 0$).

TABLE I
NORMALIZED THD OF DC-LINK CURRENT OF THE PROPOSED CONVERTER

Topology (PWM)	$THDp/THDc$
Proposed (Single $\mu = 0.5$)	0.994
Proposed (Double $\mu = 0.5$)	1.002
Proposed (Double $\mu = 0$)	0.717

It is possible to reduce the second order harmonic intro-duced by single-phase operation, but this is not of interest be-cause it requires unbalancing and increasing rectifier currents i_a and i_b.

VIII. INPUT INDUCTORS:

The PWM with double-carrier strategy reduces the *WTHD* of the resultant rectifier voltage v_{ab}, as observed in Fig. 4. When the input inductors of the proposed topology (L^g) are equal to that of the conventional topology (L_g), the reduction of the *THD* of the grid current is directly indicated in Fig. 4. Fig. 9 depicts the *THD* of the grid current as a function of µ for different values of l_n [the inductances of rectifiers A and B (l^g) referred to that of the conventional configuration (l_g), i.e., $l_n = l_g/l_g$]. For $l_n > 0.4$ ($l^g > 0.4l_g$) the *THD* of the grid current of the proposed topology is smaller than that of the conventional topology.

The harmonic distortion of the rectifier currents (i_a, i^a, i_b, i^b, and i_o) is higher than that of the grid current i_g. The adequate choice of the PWM strategy permits to operate with minimum harmonic distortion.
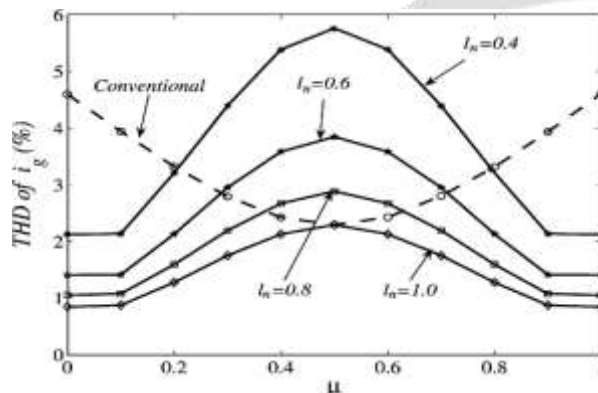

Fig. 9. Inductor specification in terms of *THD* of i_g and µ.

In any case, the use of additional common-mode inductors is a very efficient manner of reduce the harmonic distortion of these currents [12]. This approach may be also employed in the present case to reduce the total inductance required for an adequate operation of the system. The design of inductors may follows the guide lines presented in [12] for an active power filter system.

IX. FAULT COMPENSATION

The proposed system presents redundancy of the rectifier converter, which can be useful in fault-tolerant systems. The proposed system can provide compensation for open-circuit and short-circuit failures occurring in the rectifier or inverter converter devices. The fault compensation is achieved by reconfiguring the power converter topology with the help of isolating devices (fast active fuses—F_j, $j = 1, \ldots, 7$) and connecting devices (back-to-back connected SCRs—t_1, t_2, t_3), as observed in Fig. 10(a) and discussed in [41]-[44]. These devices are used to redefine the post-fault converter topology, which allows continuous operation of the drive after isolation of the faulty power switches in the converter. Fig. 10(b) presents the block diagram of the fault diagnosis system. In this figure, the block fault identification system (FIS) detects and locates the faulty switches, defining the leg to be isolated. This control system is based on the analysis of the pole voltage error.

The fault detection and identification is carried out in four steps:

1) measurement of pole voltages (v_{j0});
2) computation of the voltage error ε_{j0} by comparison of reference voltages and measurements affected in Step 1);
3) determination as to whether these errors correspond or not to a faulty condition; this can be implemented by the hysteresis detector shown in Fig. 10(b);
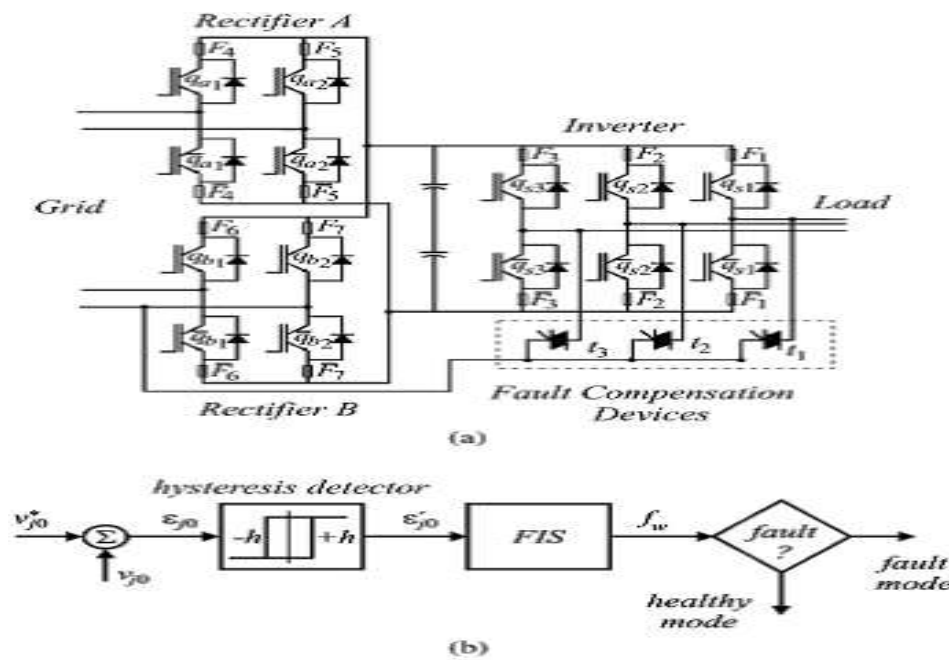4) identification of the faulty switches by using ε^{j0}.

Fig. 10.(a) Proposed configuration highlighting devices of fault-tolerant sys-tem. (b) Block diagram of the fault diagnosis system.
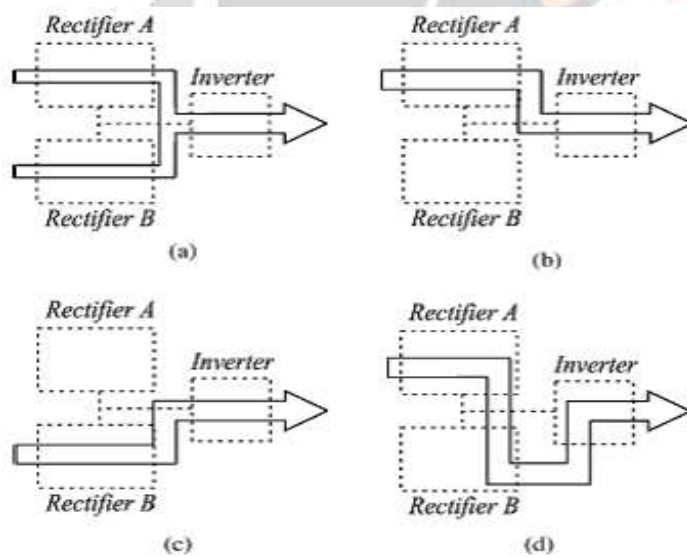

Fig.11.Possibilities of configurations in terms of fault occurrence. (a) Pre-fault system. (b) Post-fault system with fault at the rectifier B.
(c) Post-fault system with fault at the rectifier A. (d) Post-fault system with fault at the inverter.

X. LOSSES AND EFFICIENCY:

The evaluation of the rectifier losses is obtained through re-gression model presented in [45]. The switch loss model includes: 1) IGBT and diode conduction losses; 2) IGBT turn-ON losses; 3) IGBT turn-OFF losses; and 4) diode turn-OFF energy. The loss evaluation takes into account just the rectifier circuit, since the inverter side of converter is the same for the proposed and standard configurations. When the rectifiers operate with a switching frequency equal to 5 kHz, the conduction and switching losses of the proposed topology were 70% and 105%, respectively, of the correspond-ing losses of the conventional topology.

Consequently, in this case, the total losses of the proposed topology was smaller than that of the conventional topology. The increase of the switching frequency does not change the conduction losses of both topologies, but increases their switching losses, especially for the proposed topology that has a high number of switches.

The efficiency of the topologies operating with a switching frequency equal to 10 kHz and 5 kHz was evaluated by experimental measurement with a 2 kW load. Table II shows the experimental results of the rectifier efficiency. Such results are obtained for the proposed system (η_p) normalized in terms conventional one (η_c), for three cases: 1) both rectifiers operating at 10 kHz and $L_g = L_g$ 2) both rectifiers operating at 10 kHz and $L_g = L_g/2$; and 3) both rectifiers operating at 5 kHz and $L_g = L_g$. Three strategies are considered in terms of PWM control: 1) single-carrier with $\mu = 0.5$ (S-Ca $\mu = 0.5$);

2) double-carrier with $\mu = 0.5$ (D-Ca $\mu = 0.5$); and 3) double carrier with $\mu = 0$ (D-Ca $\mu = 0$). For case 1) the proposed configuration with double-carrier and $\mu = 0$ have its efficiency slightly smaller than that of the conventional one, but with the other PWM strategies its efficiency is clearly inferior. In the other cases, the proposed configuration with double-carrier and $\mu=0$ presents higher efficiency than the conventional one.

XI. COSTS AND APPLICATIONS OF CONFIGURATION:

The initial investment of the proposed system is higher than that of the standard one, since the number of switches and devices such as fuses and triacs is highest. But, considering the scenario when faults may occur, the drive operation needs to be stopped for a non programmed maintenance schedule. The cost of this schedule can be high and this justifies the high initial investment inherent of fault-tolerant motor drive systems. On the other hand, the initial investment can be justified if the *THD* or losses of the conventional system is a critical factor. Furthermore, the cost of power switches has decreased substantially [46]. This permits to employ extra switches without increasing the final price of converter dramatically.

The proposed system can be used in the same applications as the conventional configuration (rural or remote application), especially when the *THD* of the grid current, fault tolerance and efficiency of converter are critical issues. In Brazil, it is quite common to have a single-phase distribution system and a demand to supply a three-phase motor. A single-phase to three-phase converter with bidirectional flux in the rectifier circuit has been required in the distributed generation system [5].

XII. EXPERIMENTAL RESULTS:

The system shown in Fig. 2 has been implemented in the laboratory. The setup used in the experimental tests is based on a microcomputer equipped with appropriate plug-in boards and sensors. The system operates with a switching frequency equal to 10 kHz. Steady state, transient, fault analysis, and interleave operation have been evaluated in the experimental testes.

The steady-state experimental results are shown in Fig. 12. The waveforms in this figure are: (a) voltage and current of the grid, (b) dc-link voltage, (c) currents of rectifier A and circulating current, (d) currents of rectifiers A and B, and (e) load line voltage. Note that, with the proposed configuration, all control demanded for single-phase to three-phase converter has been established. The control guarantees sinusoidal grid current with power factor close to one [see Fig. 12(a)], dc-link and machine voltages under control [see Fig. 12(b) and (e)]. Furthermore, the proposed configuration provides current reduction in the rectifier side (half of the current of the standard topology) [see Fig. 12(d)], which can provide loss reduction. Also, the control guarantees the circulating current close to zero [see Fig. 12(c)]. The same set of experimental results was obtained for transient in the machine voltages, as observed in Fig. 13. A volts/hertz control was applied for the three-phase ma-chine, from V/Hz = 83.3 V/40 Hz to V/Hz = 125 V/60 Hz [see Fig. 13(e)], which implies in increased of power furnished by
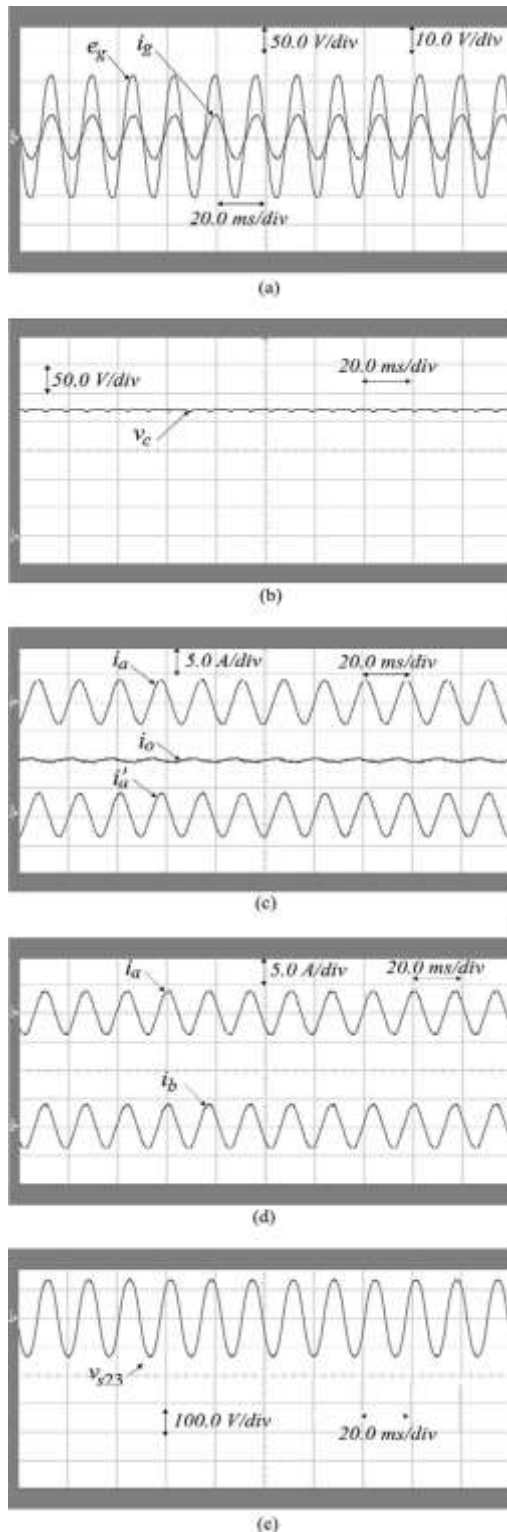
(a)

(b)

(c)

(d)

(e)

Fig. 12.   Steady-state experimental results. (a) Grid voltage (e_g)
and gird current (i_g). (b) Capacitor voltage (v_c). (c) Currents of
rectifier A (i_a and i^a) and circulating current (i_o). (d) Currents of
rectifiers A (i_a) and B (i_b). (e) Line voltage of the load (v_{s23}).
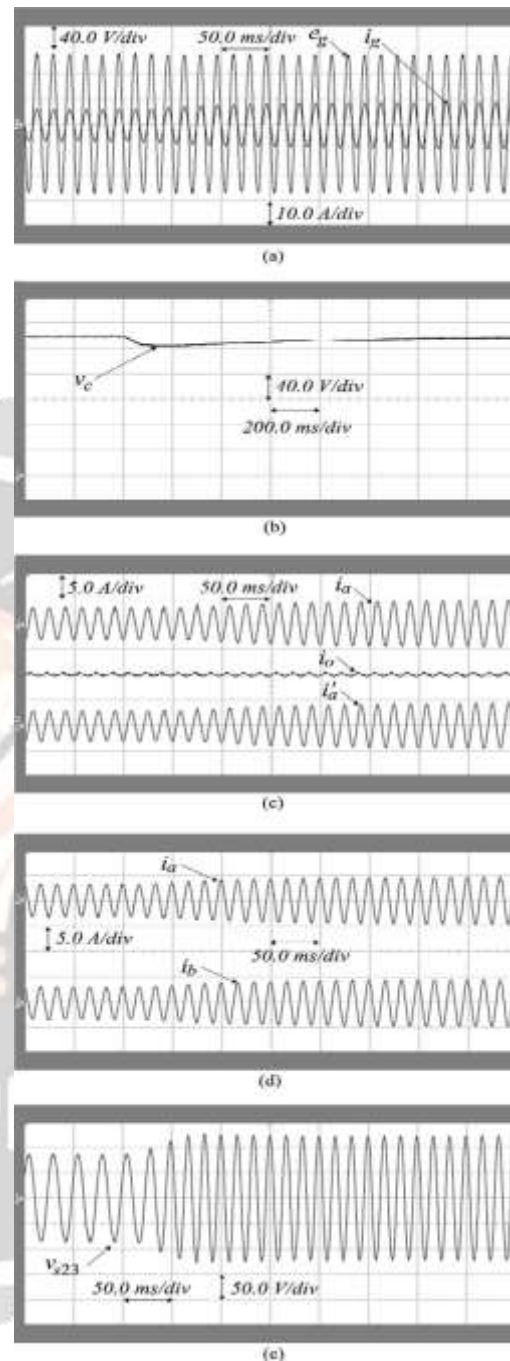

(a)

(b)

(c)

(d)

(e)

Fig. 13.   Experimental results for a volts/hertz transient
applied to the three phase motor. (a) Grid voltage (e_g)
and gird current (i_g). (b)Capacitor volt-age (v_c). (c)
Currents of rectifier A (i_a and i^a) and circulating current
(i_o).(d) Currents of rectifiers A (i_a) and B (i_b). (e) Line
voltage of the load (v_{s23}).

(a)

(b)

(c)

(d)

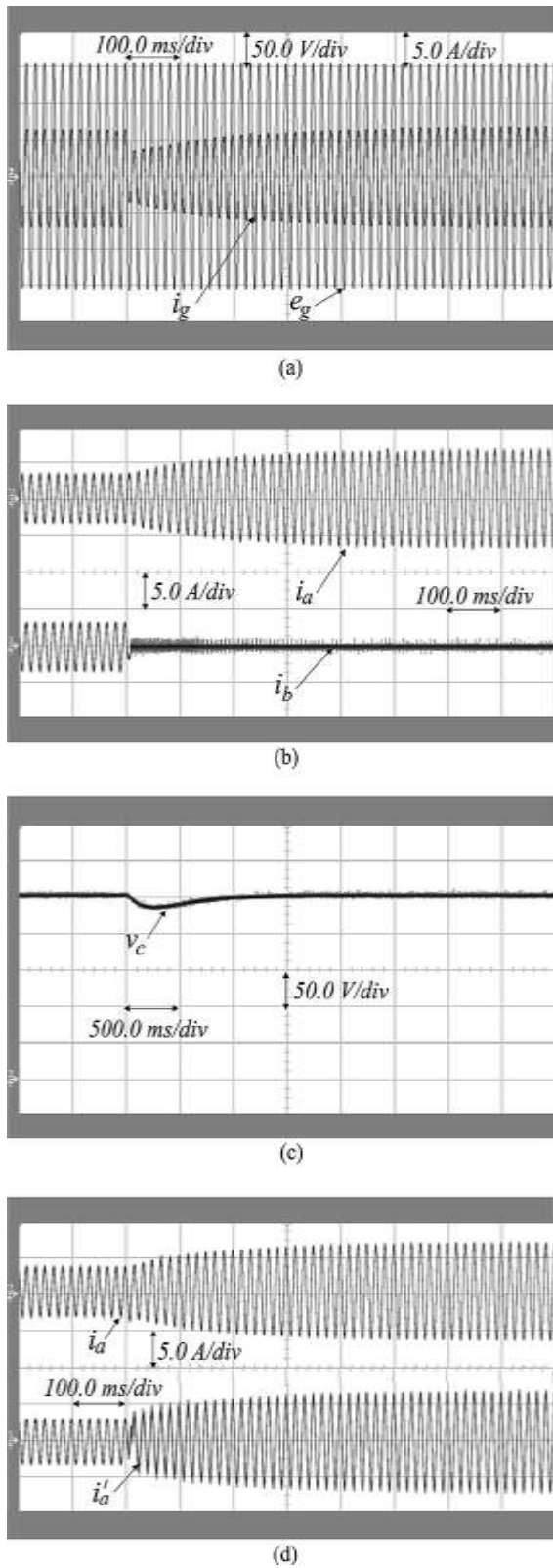Fig. 14. Experimental results of the proposed configuration when a fault is identified at the rectifier B. (a) Grid voltage (e_g) and grid current (i_g). (b) Currents of rectifiers A (i_a) and B (i_b). (c) Capacitor voltage (v_c). (d) Currents of rectifier A (i_a and i^a).
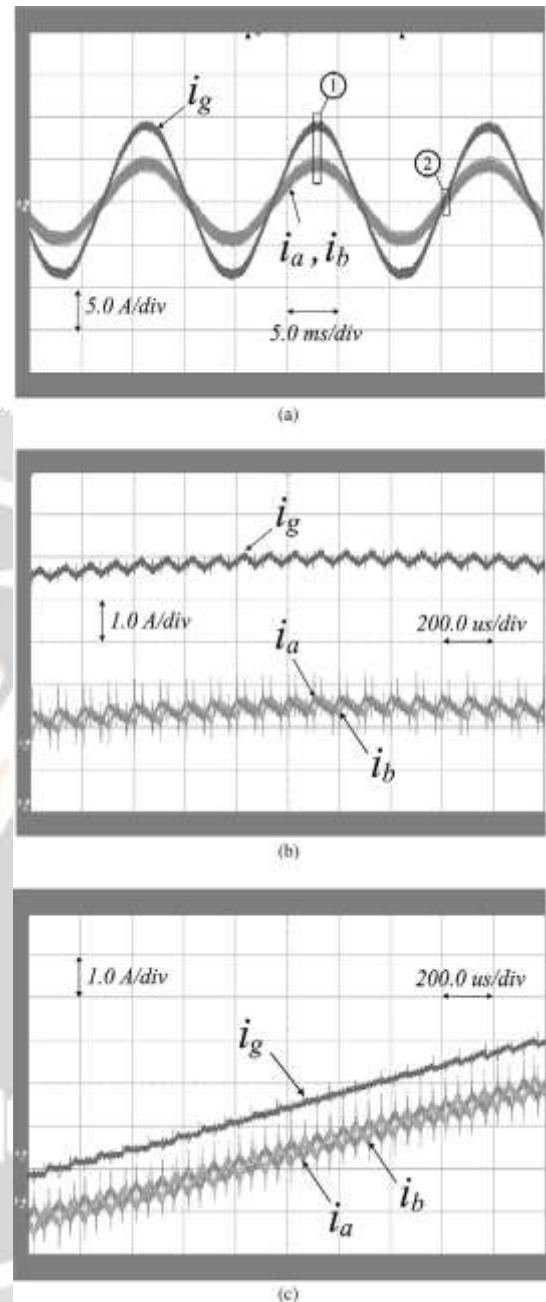

(a)

(b)

(c)

Fig. 15. Experimental results highlighting the interleaved operation (double carrier PWM). (a) Complete view. (b) Zoom of the point 1. (c) Zoom of the point 2.

the grid [see Fig. 13(a)]. In spite of this transient, the dc-link voltage [see Fig. 13(b)] and other variables are under control [see Fig. 13(c) and (d)]. Experimental results presented in Fig. 14 show the behavior of variables of the proposed system when a fault is detected in rectifier B. In this case, after fault detection given by the control system, the rectifier B has been isolated and the total flux of energy flows through rectifier A. Fig.14 shows grid voltage and current, currents of rectifiers A and B, capacitor voltage, and currents of rectifier A. The fault occurrence is intentionally created by using bypass switches. Fig. 15 shows the effect of interleaved operation in terms of grid and converter currents, i.e., i_g, i_a, and i_b. Point 1 of Fig. 15(a) indicates these variables (i_g, i_a, and i_b) when they flow at their peak values, as highlighted in Fig. 15(b). Instead, point 2 of Fig. 15(a) shows the current when they cross the zero, as highlighted in Fig. 15(c). Note that the benefit of the interleaved operation is emphasized in point 2, when the voltage pulse pattern has a duty cycle close to 0.5.

XIII. CONCLUSION:

A single-phase to three-phase drive system composed of two parallel single-phase rectifiers, a three-phase inverter and an induction motor was proposed. The system combines two parallel rectifiers without the use of transformers. The system model and the control strategy, including the PWM technique, have been developed.

The complete comparison between the proposed and standard configurations has been carried out in this paper. Compared to the conventional topology, the proposed system permits to reduce the rectifier switch currents, the *THD* of the grid current with same switching frequency or the switching frequency with same *THD* of the grid current and to increase the fault tolerance characteristics. In addition, the losses of the proposed system may be lower than that of the conventional counterpart.

The initial investment of the proposed system (due to high number of semiconductor devices) cannot be considered a drawback, especially considering the scenario where the cited advantages justify such initial investment. The experimental results have shown that the system is con-trolled properly, even with transient and occurrence of faults.

ACKNOWLEDGMENT:

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