ENHANCEMENT OF POWER FACTOR USING ISOLATED THREE PHASE AC-DC CONVERTER

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ABSTRACT

A new interleaved single-stage ac–dc converter is proposed in this project to reduce line current harmonics while achieving power factor correction (PFC). The proposed rectifier can produce input currents that do not have deadband regions with high PFC, operate with a continuous output current, and minimize the input electromagnetic interference filter size. The proposed converter uses a flying capacitor structure with standard phase shift PWM to improve efficiency, particularly at light load conditions. In the paper, the operation and its steady-state characteristics are explained and its design is discussed. In this paper, the operation of the new converter is explained, its features and design are discussed in results, and its operation is confirmed with simulation results obtained from a simulink model realization in MATLAB environment

Keyword: - *DC-DC Converter, Interleaved converter, AC-DC Converter, Power Factor*

1. INTRODUCTION

Power factor correction (PFC) is needed in ac–dc power supplies for them to comply with harmonic standards such as IEC 1000-3-2 [1]–[3]. Although it is possible to satisfy these standards by adding passive filter elements to the traditional passive diode rectifier/*LC* filter input combination, the resulting converter would be very bulky and heavy due to the size of the low-frequency inductors and capacitors. The most common approach to PFC is to use two-stage power conversion schemes. These two-stage schemes use a front-end ac–dc converter stage to perform ac–dc conversion with PFC with the output of the front-end converter fed to a back-end dc–dc converter stage that produces the desired isolated dc output voltage [4]. Using two converter stages in this manner, however, increases the cost, size, and complexity of the overall ac–dc converter, and this has led to the emergence of single-stage power-factor-corrected converters.

In order to reduce the cost, size, and complexity associated with two-stage ac–dc power conversion and PFC, researchers have tried to propose single-stage converters that integrate the functions of PFC and isolated dc–dc conversion in a single power converter. Several single-phase [5]–[11] and three-phase [4], [12]–[24] converters have been proposed in the literature, with three-phase converters being preferred over single-phase converters for higher power applications.

Previously proposed three-phase single-stage ac–dc converters, however, have at least one of the following drawbacks that have limited their widespread use.

1) They are implemented with three separate ac–dc single-stage modules [13]–[15].
2) The converter components are exposed to very high dc bus voltages so that switches and bulk capacitors with very high voltage ratings are required [17], [18].
3) The input currents are distorted and contain a significant amount of low-frequency harmonics because the converter has difficulty performing PFC and dc–dc conversion simultaneously [16].
4) The converter must be controlled using very sophisticated techniques and/or nonstandard techniques [5]–[11]. This is particularly true for resonant-type converters that need variable-switching-frequency control methods to operate.
5) The output inductance must be very low, which makes the output current to be discontinuous. This results in a very high output ripple so that secondary diodes with high peak current ratings and large output

capacitors to filter the ripple are needed [13]–[20].

6) Most of them are in discontinuous conduction mode at the input and need to have a large input filter to filter out large high-frequency harmonics [4], [13]–[15].

The authors proposed a three-phase single-stage three-level converter to mitigate these drawbacks in [24]. Although the converter proposed in that paper was an advance over previously proposed three-phase single-stage converters, it still suffered from the need to have a discontinuous output inductor current at light-load conditions to keep the dc bus capacitor voltage < 450 V, and it needed to operate with discontinuous input current, which resulted in high component current stress and the need for significant input filtering due to the large amount of ripple.

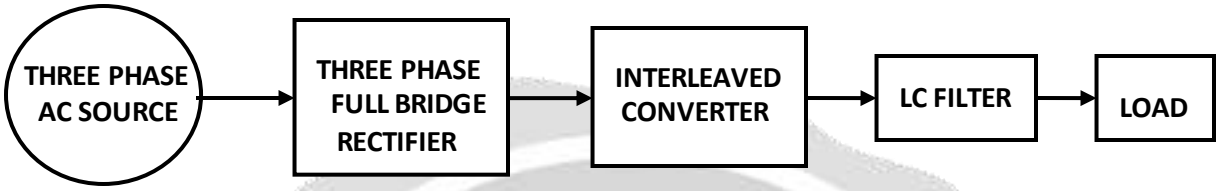


Fig-1: Block diagram of the proposed system

2. PROPOSED TECHNIQUE

The proposed converter and its key waveforms are shown in Figs. 1 and 2, respectively. The proposed converter uses auxiliary windings that are taken from the converter transformer to act as "magnetic switches" to cancel the dc bus capacitor voltage so that the voltage that appears across the diode bridge output is zero. When the primary voltage of the main transformer is positive, auxiliary winding 1 ($N_{aux1}/N_1 = 2$) cancels out the dc bus voltage so that the output voltage of diode bridge 1 (DB_1) is zero and the currents in input inductors L_{a1}, L_{b1}, and L_{c1} rise. When the primary voltage of the main transformer is negative, auxiliary winding 2 ($N_{aux2}/N_1 = 2$) cancels out the dc bus voltage so that the output voltage of diode bridge 2 (DB_2) is zero and the currents in input inductors L_{a2}, L_{b2}, and L_{c2} rise. When there is no voltage across the main transformer primary winding, the total voltage across the dc bus capacitors appears at the output of the diode bridges and the input currents fall since this voltage is greater than the input voltage. If the input currents are discontinuous, the envelope of the input current will be sinusoidal and in phase with the input voltages.

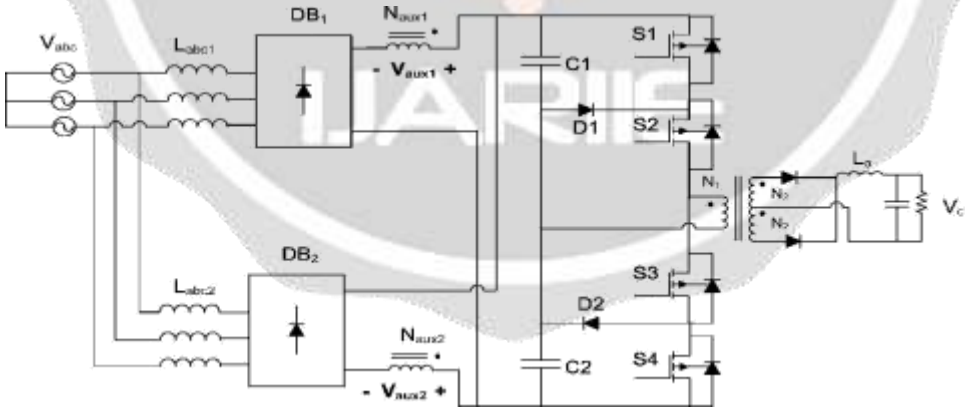


Fig-2: Proposed interleaved three-phase three-level converter.

The converter modes of operation are explained in this section. The typical converter waveforms are shown in Fig. 2. The equivalent circuit in each stage is shown in Fig. 3. The converter goes through the following modes of operation.

Mode 1 ($t_0 < t < t_1$) [Fig. 3(a)]: During this interval, switches S_1 and S_2 are ON. In this mode, the energy from dc bus capacitor C_1 flows to the output load. Due to magnetic coupling, a voltage appears across auxiliary winding 1 which is equal to the dc bus voltage but has opposite polarity and cancels the total dc bus capacitor voltage; the voltage at the diode bridge output is zero, and the input currents in L_{a1}, L_{b1}, and L_{c1} rise.

Mode 2 ($t_1 < t < t_2$) [Fig. 3(b)]: In this mode, S_1 is OFF, and S_2 remains ON. The energy stored in $L_1(L_1 = L_{abc1})$ during the previous mode starts to transfer into the dc bus capacitors. The voltage that appears across auxiliary winding 1 is zero. The primary current of the main transformer circulates through D_1 and S_2. With respect to the converter's output section, the load inductor current freewheels in the secondary of the transformer, which defines a voltage across the load filter inductor equal to $-V_L$.

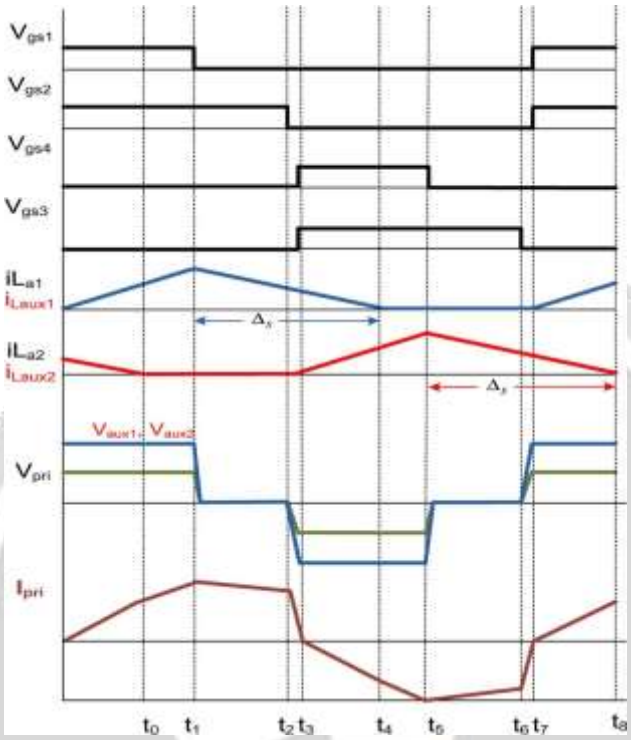
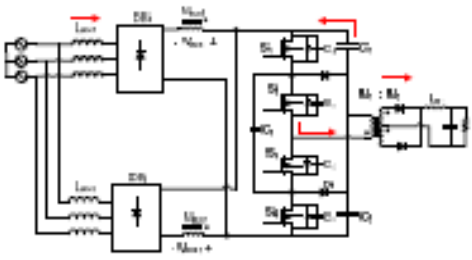
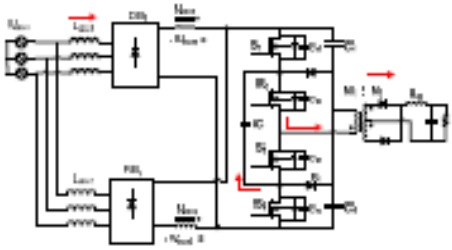


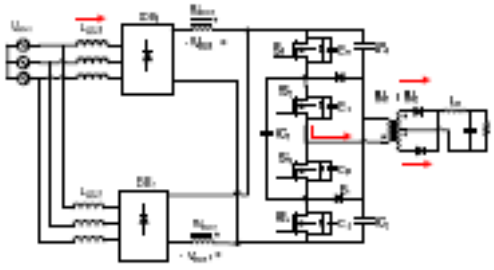
Fig-3: Typical waveforms describing the modes of operation.



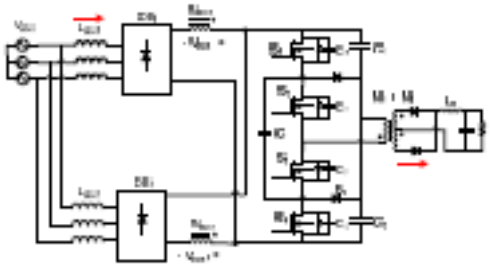
Mode 1 ($t_0 < t < t_1$)



Mode 2 ($t_1 < t < t_2$)



Mode 3 ($t_2 < t < t_3$)



Mode 4 ($t_3 < t < t_4$)

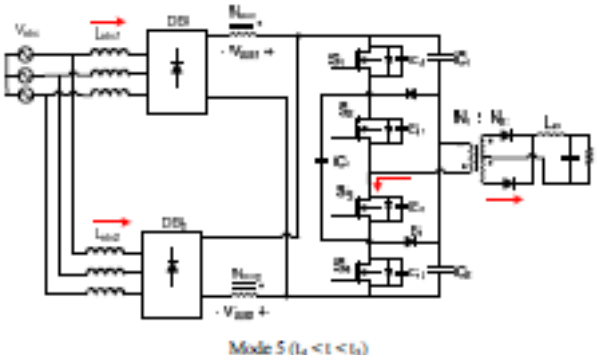


Fig-4: Modes of operation. (a) Mode 1 ($t_0 < t < t_1$). (b) Mode 2 ($t_1 < t < t_2$). (c) Mode 3 ($t_2 < t < t_3$). (d) Mode 4 ($t_3 < t < t_4$). (e) Mode 5 ($t_4 < t < t_5$). (f) Mode 6 ($t_5 < t < t_6$). (g) Mode 7 ($t_6 < t < t_7$). (h) Mode 8 ($t_7 < t < t_8$).

Mode 3 ($t_2 < t < t_3$) [Fig. 3(c)]: In this mode, S_1 and S_2 are OFF. The energy stored in L_1 still is transferring into the dc bus capacitor. The primary current of the transformer charges C_2 through the body diodes of S_3 and S_4. Switches S_3 and S_4 are switched ON at the end of this mode.

Mode 4 ($t_3 < t < t_4$) [Fig. 3(d)]: In this mode, S_3 and S_4 are ON, and the energy flows from capacitor C_2 into the load. The voltage appears across auxiliary winding 2 which is equal to the dc bus voltage but acts like a magnetic switch and cancels out the dc bus voltage. The voltage across the boost inductors L_2 ($L_2 = L_{abc2}$) becomes only the rectified supply voltage of each phase, and the current flowing through each inductor increases. This mode ends when the energy stored in L_1 completely transfers into the dc bus capacitor. For the remainder of the switching cycle, the converter goes through modes 1–4 but with S_3 and S_4 ON instead of S_1 and S_2 and with DB_2 instead of DB_1.

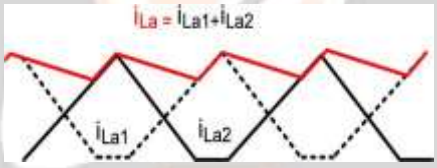


Fig-5: Interleaving between two input inductor currents.

Mode 5 ($t_4 < t < t_5$) [Fig. 3(e)]: In this mode, S_3 and S_4 are ON, and a symmetrical period begins. In this mode, the energy flows from capacitor C_2 into the load. The voltage across the boost inductors L_2 becomes only the rectified supply voltage of each phase, and the current flowing through each inductor increases.

Mode 6 ($t_5 < t < t_6$) [Fig. 3(f)]: In this mode, S_3 is ON and S_4 is OFF, and the primary current of the main transformer circulates through diode D_2 and S_3. The energy stored in the boost inductors L_2 during the previous mode starts transferring into the dc bus capacitor. The output inductor current also freewheels in the secondary of the transformer during this mode.

Mode 7 ($t_6 < t < t_7$) [Fig. 3(g)]: In this mode, S_3 and S_4 are OFF, and the primary current of the transformer charges capacitor C_1 through the body diodes of S_1 and S_2. The energy stored in the boost inductors L_2 transfers into the dc bus capacitor.

Mode 8 ($t_7 < t < t_8$) [Fig. 3(h)]: In this mode, S_1 and S_2 are ON. In this mode, the energy from dc bus capacitor C_1 flows to the output load. This mode ends when the energy in the inductors L_2 completely transfers into the dc bus capacitors. Time t_8 is the end of the switching cycle, and another switching cycle begins with the same modes.

It should be noted that the input current is the summation of inductor currents i_{L1} and i_{L2} which are both discontinuous. However, by selecting appropriate values for L_1 ($= L_{a1} = L_{b1} = L_{c1}$) and L_2 ($= L_{a2} = L_{b2} = L_{c2}$) in such a way that two inductor currents such as i_{La1} and i_{La2} have to overlap each other, the input current can be made continuous as shown in Fig. 4, thus reducing the size of the input filter significantly. There is a natural 180° phase difference between the currents in L_1 and the currents in L_2 as one set of currents rises when the transformer primary is impressed with a positive voltage and the other set rises when the transformer primary is impressed with a negative voltage—these two events occur 180° apart during a switching cycle.

3. SIMULATION RESULTS

A simulation circuit has been designed using MATLAB software. Two split capacitors each one rated at 470 µF are connected to the dc link. The output capacitor is 100µF. The input and output inductors are chosen as 27µH. The switching frequency of the switches is set to 125 kHz. The turns ratio of the transformer is 1:2. The neutral point clamping diodes (D_5 and D_6) are SiC diodes.. The power switches (S_1 to S4) used is N-Channel MOSFETs. The input power is 480W for this case. The ac voltage is supplied from an ac power source at 90Vrms at 60Hz. The input inductor current is discontinuous, and S_2-S_3 switch pair is switched at constant duty cycle. It is worth mentioning that an L-C network, connected to the circuit externally, is employed to filter the input current. The high PF can be observed from the alignment of input voltage and current, and the sinusoidal envelope. DC link voltage slightly oscillates with the twice of the input frequency around 400V.

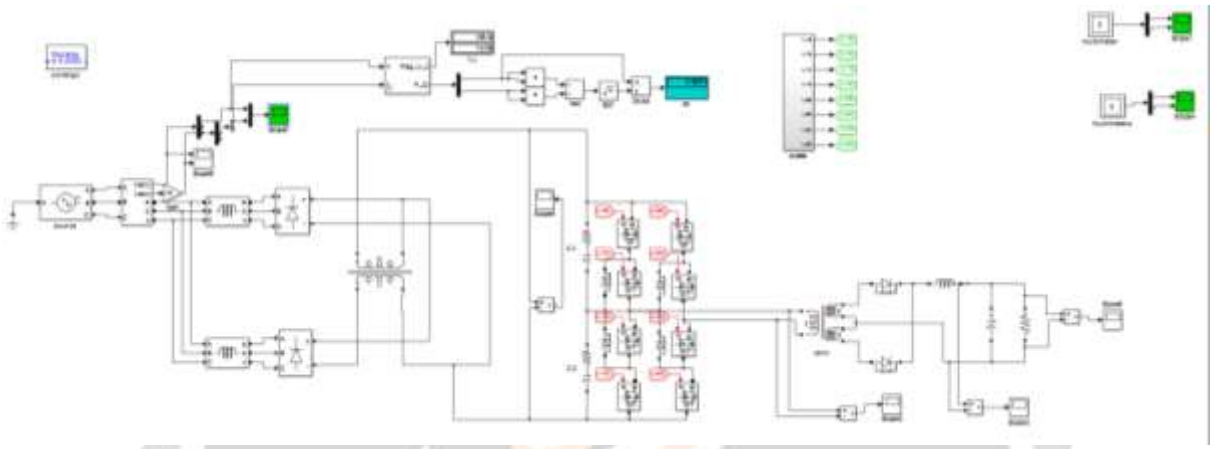


Fig-6: Simulation of the proposed circuit

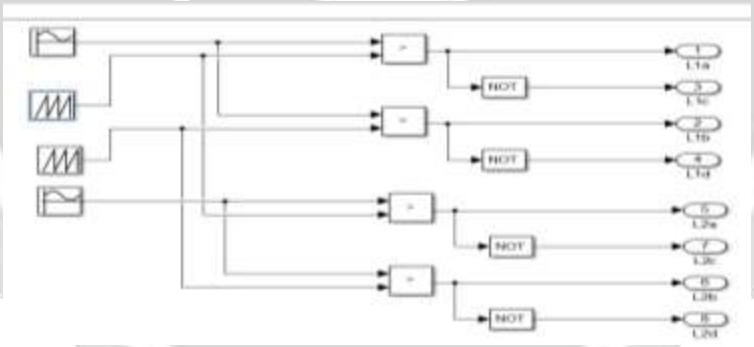


Fig-7: design of the proposed controller

When the middle switches are turned on, zero voltage is applied to the transformer primary winding. When one of the middle switches is turned off, and either S1 or S4 is turned on, half of the dc link voltage is applied to the transformer's primary winding. Meantime, the energy stored in the input inductor is transferred to the dc link. During the overlap of the switches, the output inductor current decreases under the output voltage, and when S2 or S3 is turned on along with S1 or S4, the output inductor current increases under Vdc/2N-Vo. The output inductor voltage and secondary transformer voltage are provided in Fig-9. The ac variation of the generated duty ratio is opposite the dc link voltage ripple, which effectively eliminates the low frequency ripple of the output voltage.

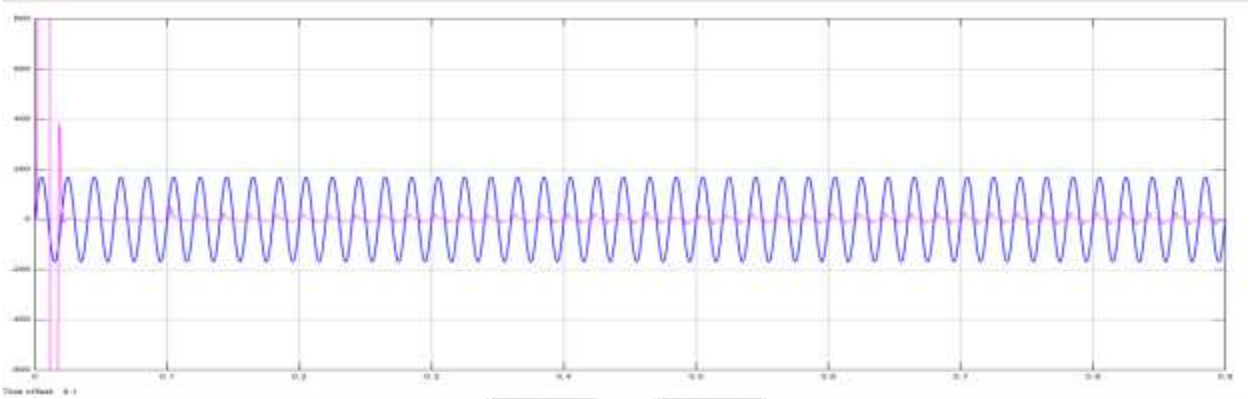


Fig-8: Input Voltage and current of the source

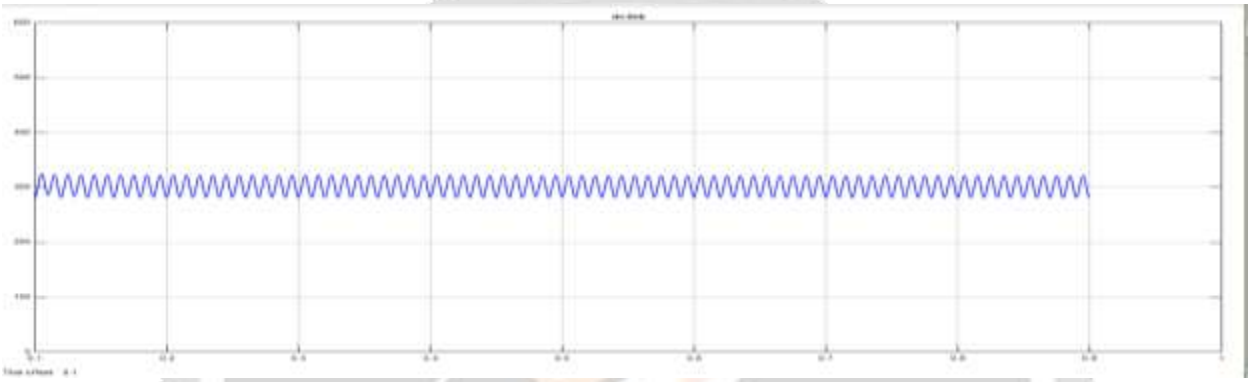


Fig-9: DC-link voltage of the proposed converter

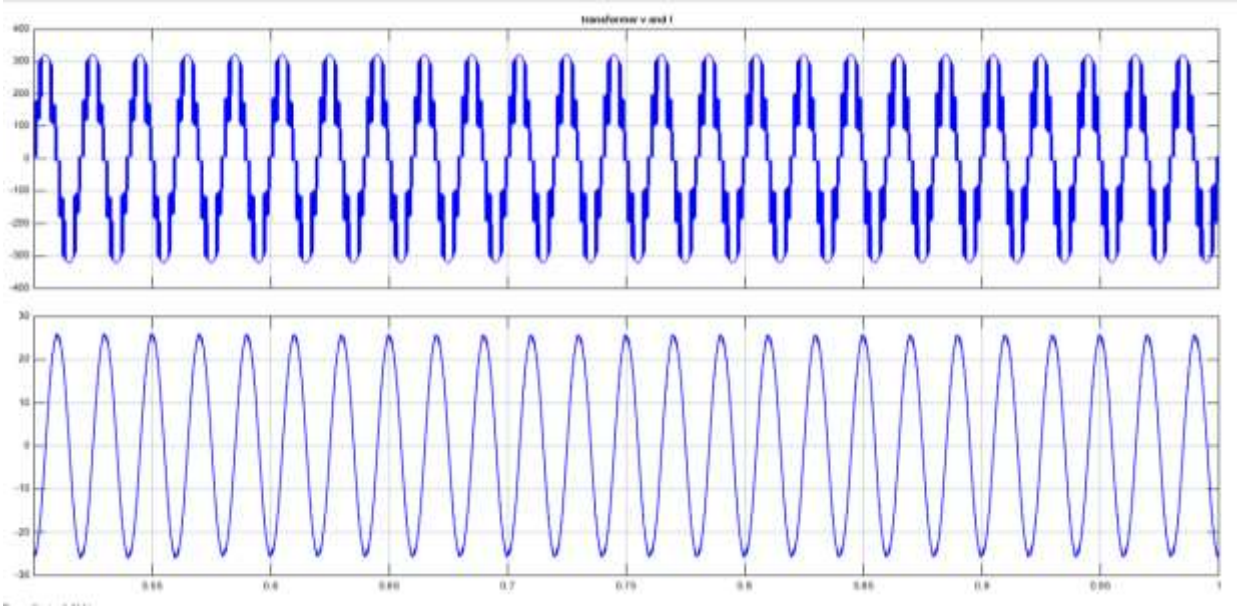


Fig-10: transformer winding voltage and current waveforms

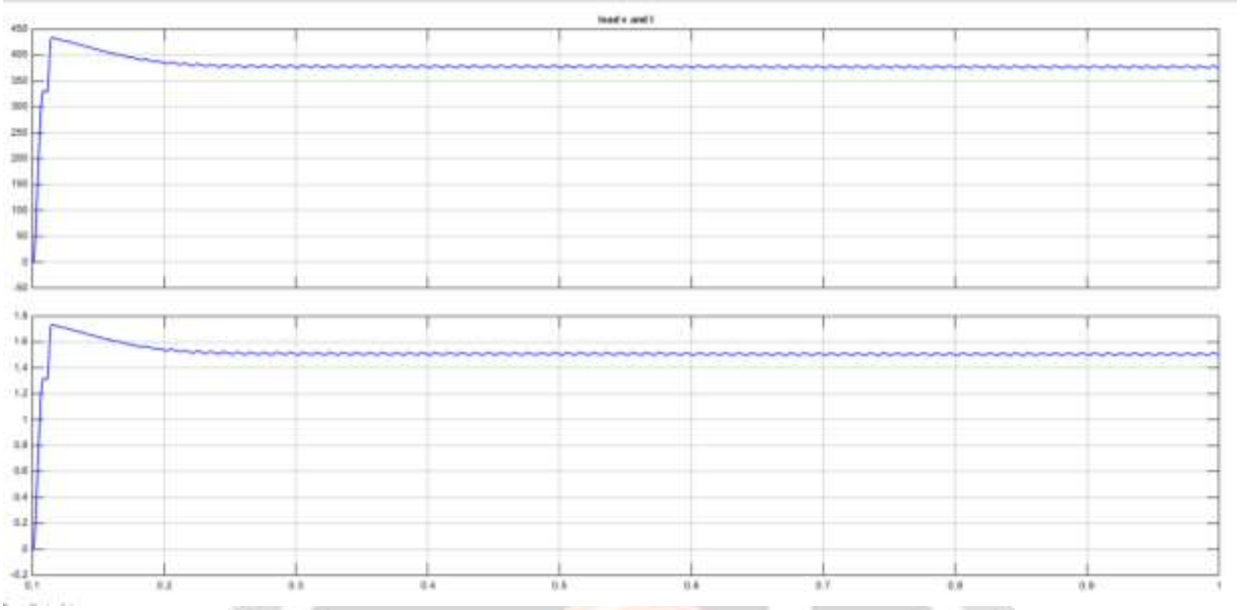


Fig-11: output voltage and current of the proposed system

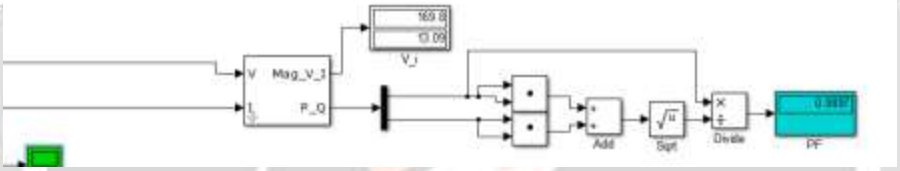


Fig-12: power factor of the input source using proposed system

4. CONCLUSIONS

A new three-phase three-level single-stage power-factor-corrected ac–dc converter with interleaved input has been proposed in this paper. The converter operates with a single controller to regulate the output voltage and uses auxiliary windings taken from its power transformer as magnetic switches to cancel the dc bus voltage so that the input section operates like a boost converter. The proposed converter has the following features. The proposed converter can operate with lower peak volt-age stresses across its switches and the dc bus capacitors as it is a three-level converter. This allows for greater flexibility in the design of the converter and ultimately improved performance. The proposed converter can operate with an input current harmonic content that meets the EN61000-3-2 Class A standard with reduced input filter due to the interleaved structure. The output inductor of the proposed converter can be designed to work in continuous conduction mode over a wide range of load variation and input voltage. This results in a lower output inductor current ripple than that found in previously proposed converters which helps reduce secondary component stresses and filtering. The aforementioned features are all an improvement on the original non interleaved converter that was presented in [24]. Moreover, the proposed interleaved converter operates with greater efficiency than the converter proposed in [24] because it has fewer diodes in the dc bus and it has less turn-on losses.

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