Effective Fault Diagnosis on LDPC check using C432 Benchmark Circuits

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ABSTRACT

The reliability of various devices were measured through effective fault diagnosis approaches. FPGA based devices either independent or a dependent to the application. In this paper, the fault diagnosis based on Low Density Parity Check (LDPC) is proposed. The C432 benchmark circuit is programmed with LDPC scheme to diagnosis the SA-O and SA-1 stuck-at faults in the circuit. The iterative shifting of bits in the register checks the fault in the circuit. The benchmark circuit is used for measuring the performance and reveals the efficient fault diagnosis based on LDPC scheme. The comparative analysis between the Bose, Chaudhuri and Hocquenghem (BCH) and proposed LDPC confirms the effective fault diagnosis in FPGA.

Keyword —*Bose, Chaudhuri, and Hocquenghem (BCH), Field Programmable Gate Array (FPGA), Fault Diagnosis, Low Density Parity Check (LDPC), Look Up Table (LUT).*

I. INTRODUCTION

Field Programmable Gate Arrays (FPGA) are the array of Configurable Logic Blocks (CLB), switching matrices surrounded by programmable input / output blocks. Due to the features of reprogrammable and flexible, the FPGA architecture used in various applications such as digital system design, LUT based applications, real time implementations of storage devices. The reconfigurable feature plays vital role in computing devices. The reprogrammable architecture is very helpful in real time embedded systems and research oriented process. The corruption of bit in FPGA occurs due to the radiations in the atmosphere termed as Single Event Upsets (SEUs) this permanently affects the performance of the FPGA architecture.

The testing process is necessary for the detection of SEU in FPGA to improve the performance. The testing process split into two types: application dependent and application independent. Application independent methodologies aim to detect the structural defects caused by the on chip manufacturer. During this process, the usage and non-usage intermediate parts are not considered. The application dependent diagnosis addresses the faults in the usage and non-usage parts of the chip.

The FPGA based devices with programmability feature increases the cost of reconfiguring while the design is fixed. Hence, the Application Specific Integrated Circuit (ASIC) are replaced with FPGA in order to reduce the manufacturing cost. Some of the FPGA devices in the application independent strategy used until the fault occurs in it. The cost reduction is also done by an alternative dependent strategy in which some defects are diagnosed thoroughly. But, in dependent strategy, once the particular configuration fails, the precise identification of faults in resource is required.

The automatic test pattern generation is possible by using the Genetic Algorithmic approach. The GA based approach uses the simulation based fault injection tool for fault coverage with desired test pattern. Various evolutionary based processes involves in the generation of automatic test pattern for fault diagnosis. There are two types in the evolutionary approaches. They are deterministic and random. The deterministic methods based on algorithmic process which is used to compute the test vectors for the faults with the knowledge of structure. The pseudo random n-tuples are generated in the random based test pattern generation. In this process, the knowledge of circuit structure is not necessary. But the large vectors are required to detect the faults. Hence, the quality of random test pattern generation is improved by coverage directed generation where the fault coverage for each group of test vectors is computed and they transformed into desirable patterns.

The simulations required to identify the performance of system is large under various constraints. The design time increases which is undesirable in deadline of the products. The intensive wide research component is the Forward Error Correction (FEC) to support the simulations. The occurrence of channel quality variation results in interference, multi-paths etc. The usage of low capability is enough to fulfill the Quality of Service requirements (QoS). The frame error rate and bit error rate in this model is better compared to other models. The probability of bit errors reduced with the help of System on Chip (SOC) based FPGA architecture. The SOC architecture needs transparent error detection and correction methods to improve the performance. Low- Density Parity Check (LDPC) based SOC architecture is the alternative solutions for other existing methodologies. The unique characteristics of FPGA are to maximize the throughput is LDPC based decoding. Folding is the optimization tool to enhance the memory usage in the energy efficient model. In this paper, the efficient fault diagnosis in FPGA architecture is proposed. The system uses the benchmark circuits built upon FPGA architecture. The no of LUT usage, delay and the number of flip-flops are calculated for existing and LDPC methods. The comparison results confirm the effectiveness of the proposed method over existing approaches using the benchmark circuits. The rest of the paper is organized as follows. Section II presents a description about the previous research which is relevant to fault diagnosis in FPGA architecture. Section III presents the detailed description about the proposed method. Section IV presents the performance analysis. This paper concludes in Section V.

II. RELATED WORK

This section deals with the works related to the fault diagnosis in the Field Programmable Gate Array (FPGA) architecture and the Low Density Parity Check (LDPC) are implemented to enhance the performance of benchmark circuits. Tahoori[1] uniquely identified single bridge, struck at or open faults in the interconnect and logic diagnosis also performed. But, there is a need of more accurate model than the struck at fault model to optimize the large set of faults. Evolutionary based approaches introduced for optimization. Bernardeschi et al [2] presented the Genetic Algorithm (GA) based automatic generation of test patterns for Single Event Upsets (SEU). The FPGA based architecture usage was extended to networking, financial markets where more no of libraries used. Hence, the improvement was required to minimize the faults in the architectures. Lockwood et al [3] investigated the low latency approach of FPGA in electronic trading. The identification and replacement of faulted device was crucial in electronic trading. Rodri et al[4] presented the novel failure detection technique under open and short circuits faults. The fault material was easily identified and replaced using failure detection method. Bernardeschi et al [5] presented the Genetic Algorithm (GA) based approach for fault diagnosis in Simulink models. Shahzad et al [6] presented the wireless based vibration analyzer for predicting the performance of rotating machinery and analyzing the fault in the circuit. The online adaptation of dynamically changing run time environment is necessary in the FPGA reconfigurable system. Abdelfattah et al [7] presented on line test method for reconfigurable integrated systems. The performance impact was reduced through optimization of test overhead. The high complexity of application development and hardware incompatibilities results in slow development cycle. Hence, Sidiropoulos et al [8] presented the platform independent methodology was applied to the routing process of multiple applications carried out without any performance degradation. The portability across different FPGA devices is feasible by mapping of the virtual FPGA cores into physical FPGA. A pipelined execution of multiple application mappings allowed feasible process in multiple independent installations.The fine tune topology was required for an interconnect topology in the fault diagnosis process. Chung et al [9]presented the custom interconnect topology that support communication requirements with minimized costs. The interconnect topology used the Shrink Wrap compiler analyzed the applications to provide the connectivity and bandwidth balancing between the hardware processing and kernel based applications. The enumeration of reference circuit in finite gain manner is impractical. Yang et al [10] presented an efficient architecture independent packing method for the elimination of finite gain problem. The reference circuit is transformed into preplaced clustered which simplified several design constraints. The results obtained in this model were compared with the existing methodologies for efficient transmission. The energy efficiency was disturbed due to more computational resources. Hence, the problem energy efficiency was minimized with the Look up Table (LUT) approaches. Ghosh et al [11] use embedded memory blocks for computing to improve the energy efficiency in complex applications. Complex applications were decomposed into various LUTs and they were mapped into embedded memory blocks and evaluated through single or multiple cycles. The utilization of System On-Chip (SOC) in FPGA architecture produces the errors in the inter FPGA links. Tian et al [12] presented the suitable error detection architectures in SOC based FPGA. This type of FPGA architecture improves the reliability of the devices. Xiaofei et al [13] developed Concurrent Error Detection (CED) in Recomputing with Permuted Operands (RPO) to improve the detection process of single bit faults. The hardware requirement to achieve the network throughput performance is more compared to existing methodologies. Pratas et al [14] presented the flexible, programmable and LDPC based target detection in FPGA environment. The LDPC based architecture provided the tremendous power savings and real time throughput enhancement compared to existing methods. The reliability and availability of the devices computed

on the basis of fault diagnosis processes. Freire et al [15] presented the open circuit fault diagnosis on FPGA based electrical drives. The real time detection and localization of faults in the FPGA architecture was possible using open circuit model. The presented results of FPGA based drives improve the reliability of the system. Ruan et al [16] split the Built in Self-Test (BIST) system into two types. They are hardware and software. The Test Pattern Generator (TPG) and the Output response Analyzer (ORA) belongs to software category and the circuit under test regarded as the hardware part. The configuration numbers was reduced using this type of architecture. The variation in the parameters and noise levels leads to larger error rate. Jayarani et al [17] proposed majority logic detector / decoder for fault detection strategy to reduce the error rate. The Euclidean Geometry LDPC (EG-LDPC) is the one step majority logic decoding to improve the error detection and correction in the FPGA architecture. The detection and location of faults in an application dependent model was the major concern in the research areas. Almurib et al [18] presented the scalable application dependent fault diagnosis architecture for Static Random Access Memory (SRAM) based FPGA devices. Multiple fault analysis done in this model hierarchically using LUT programming function 1 Bit Sum Function (BSF). The significant reduction in number of configuration and the faults done using BSF based architecture. The performance of SRAM based devices improved with the Spin Torque Transfer Magnetic Random Access Memory (STT-MRAM). Kui et al[19] focused on STT-MRAM technology and investigated the channel capacity measurement with the LDPC codes. The fault detection and location in this method used the reliability based min sum algorithm for decoding. The no of quantization bits also reduced with the energy maximization criterion quantized model. Researchers identified the trapping sets was the responsible for the maximum error. Hence, the suitable method was needed to detect the trapping set in FPGA architecture. Panda et al [20]presented the Bose, Chaudhuri, and Hocquenghem (BCH) encoder based FPGA real time implementation to break the trapping set at run time to reduce the error. The iterative LDPC based fault diagnosis is proposed in this paper.

III. PROPOSED METHOD

The objective of proposed work to implement fault diagnosis of bench mark circuits in FPGA architecture. The efficiency of the fault diagnosis method is validated by computing the performance parameters such as no of LUTs used, no of flip-flops used and delay. The block diagram of proposed method is shown in Fig.1.

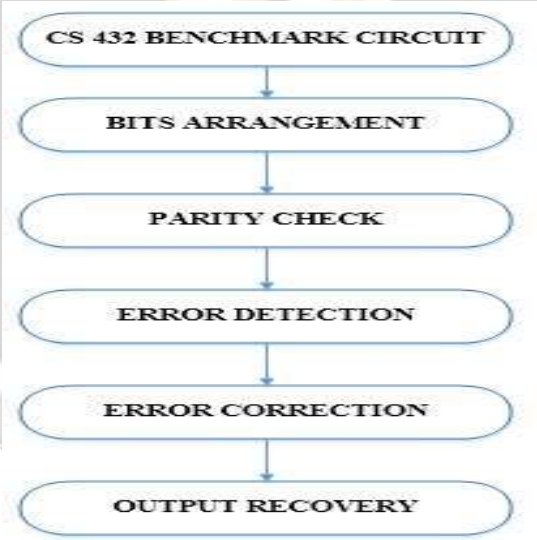

Fig. 1 Block diagram of proposed method

The proposed method implemented using various processes. The circuits for analysis are C432 benchmark circuits. The arrangement of bits carried out then the checking of parity with the given input is done. The error between the parity bits and the original bits evaluated which indicates the fault in the circuit. After the fault is detected, the correction of fault also carried out. Finally the required output is recovered from the system. The overall performance also evaluated over existing method. The flow for proposed method consists of successive steps. They are benchmark circuit results, shifting of serial bits, checking the error, modifying the bits according to error.

The fault in the FPGA architecture is identified through the shifting process of each bit in the data from the results of C432 benchmark circuit. The checking of error between the parity bits and the required output bits done. If the error is zero then there is no error occur which indicates the fault free circuit. Otherwise, the parity

bits of first set taken as the error bit and they corrected to produce the required output. The overall performance of fault diagnosis is validated through the help of measuring parameters. They are number of LUTs used, No of flip flops used and the delay time. The comparison of these parameters with the existing method shows the effectiveness of the proposed method.

The flow of proposed method of short cut tree routing as shown in Fig.2

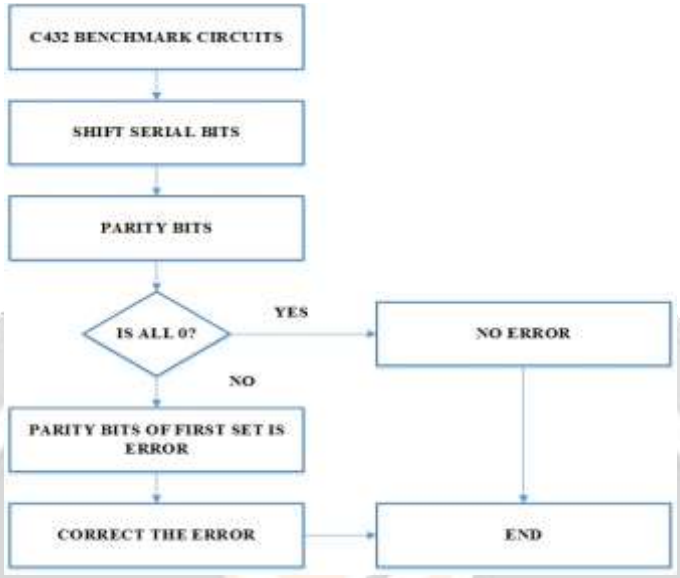

Fig. 2 Flow diagram of proposed method

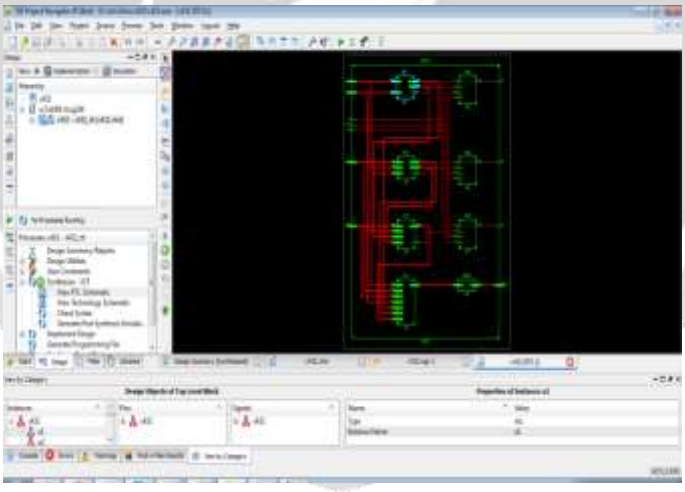

Fig. 3 C432 Benchmark Circuit

A. C432 Benchmark Circuit

C432 consists of a 27-channel interrupt controller, three 9-bit buses denoted as A, Band C. The bit position in each bus identifies the interrupt request priority. The enable and disable of the interrupt requests done by bus E. Modules labeled M1, M2, M3, and M4 contain the underlying logic. The C432 benchmark circuit for analysis is shown in fig. 3.

B. Bits Arrangement

The bits are arranged in the registers for the comparison of parity bits. Central Processing Unit (CPU) consists of set of register files in the array format. The difference between the fast SRAM and ordinary SRAM is the number of ports. Fast SRAMS have the dedicated read and write ports and ordinary SRAMS have the single

port through which read and write process occur. The individual registers for arrangement of bits are shown in fig. 4.

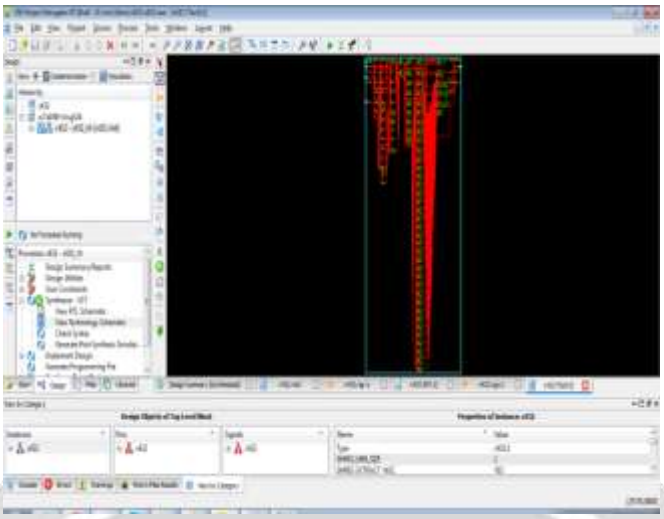

Fig. 4 Registers for bits arrangement

C. Parity Check

An LDPC code is used to check the error occurred in the FPGA circuit. It is defined as the null space of a parity check matrix H with each row (ρ) has number of 1's and each column (γ) also has number of 1's. In this code, the number of common 1's between any two columns is either 0 or 1. Also, both ρ and γ are small compared to the length of code.

As both ρ and γ are very small compared to the code length and the number of rows in the matrix H, H has a low density of 1's. Hence H is said to be a low density parity check matrix and the code defined by H is said to be a low-density parity check code.

The density of H (r) is defined to be the ratio of the total number of 1's in H to the total number of entries in H — in this case r = ρ/n = γ/J, where J is the number of rows in H. This kind of LDPC code is said to be a (γ, ρ)-regular LDPC code. If the weights of all the columns or rows in H are not the same, then it is called an irregular LDPC code.

D. Error Detection

In this section, the decoding carried in the FPGA fault circuit is discussed. Let the n-bit faulty code word c, r be the sum of the original code word, e be the error code (e is 1 at the locations at which the errors/faults have occurred, 0 otherwise). Then the sum of original code word is computed by following equation:

$$r=c+e \quad (1)$$

The decoder first calculates parity equations to find whether a particular error bit e_i is 1 or 0, each of which calculates a check sum on some bits of r. A set of J parity equations is orthogonal on e_i if each of the J parity equations check e_i (i.e., e_i is included in the check sum of each parity equation), but no other error bit is checked by more than one parity equation. If a set of J parity equations is orthogonal on e_i the ML decoding rule can be applied to decodee_i: e_i is decoded to 1 if the majority of the parity check sums of the J check sums are 1, otherwise e_i is 0.

E. Error Correction

In this module, the correction of error bit is carried out by checking last bit from shift register and bit from majority logic circuit.In this error correction stage, the output of XOR gate changes if any changes in the bit. The comparison between bits from last bit from shift register and bit from majority logic circuit carried out and finally error bit is corrected. The control signals from the memory repacking controller circuit (used to disable memory blocks in the bank architecture) are also used for selectively enabling and disabling modules of the checker, and for reconfiguring the encoder and checker components. Since we need only one controller for a complete memory bank, this module can be implemented using micro-level circuitry. The error corrected output is shown in fig. 5

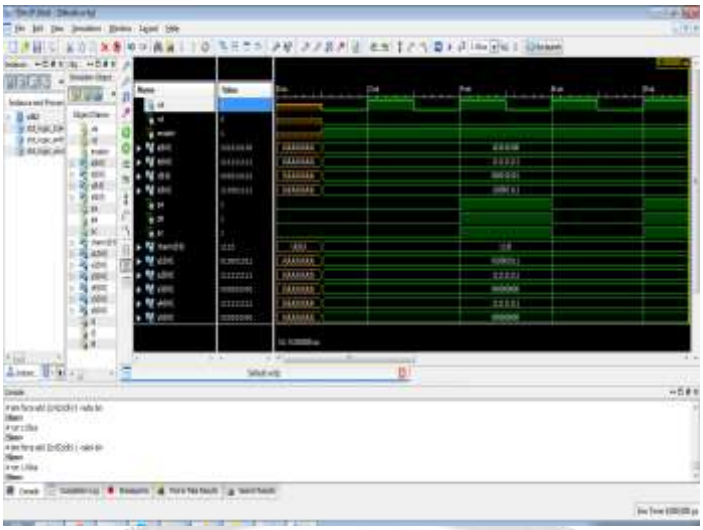

Fig. 5 Final Output

IV. PERFORMANCE ANALYSIS

This section presents the performance analysis of the proposed fault diagnosis scheme in FPGA. The proposed scheme used Low Density Parity Check (LDPC) for various measurements. The proposed scheme is also compared with the Bose, Chaudhuri, and Hocquenghem (BCH)model based on the number of LUTs used. The evaluation of the systemperformance on LUTs usage, flip flop usage and frequency is measured.

A. Look Up Tables (LUT)

Look up Tables (LUTs) are used to implement the various type of functions described in Configurable Logic Blocks (CLB). The number of LUTs is important to show the proposed algorithm is suitable for effective diagnosis compared to existing methodologies. The usage of LUT s is limited to a small value compared to the existing BCH method.

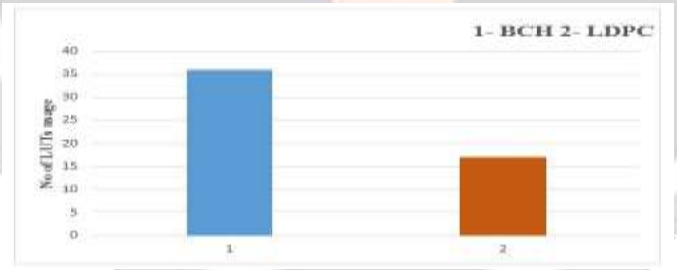

Fig. 6 No. of LUTs usage

Fig.6 describes the comparison between the BCH and LDPC. The number of LUTS is decreased in LDPC compared to BCH. The proposed LDPCalgorithm provide better usage of LUTs.

B. Flip flops

The measure of number of flip-flopsusedto store the bits are calculated using LDPC method. When the number of bits increased, the BCH method uses huge number of flip flops for storing whereas in LDPC minimum number of flip flops required as shown in fig. 7

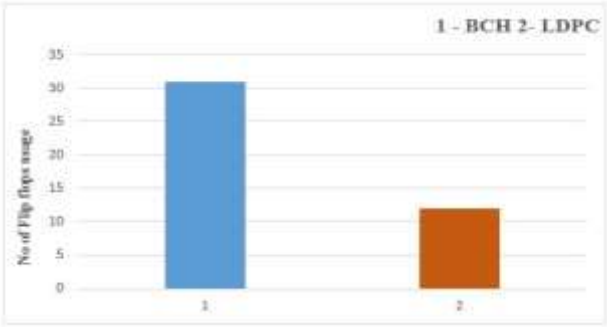

Fig. 7 No. of Flip-flops usage

Fig.7 describes the comparison between the BCH and LDPC. The number of flip flops is decreased in LDPC compared to BCH. The proposed LDPCalgorithm provide better usage of flip flops for storing the bits.

C. Clock Period

The measure of clock period required for the fault diagnosis is calculated using LDPC method. When the number of bits increased, the BCH method takes the maximum time for the fault diagnosis whereas in LDPC minimum delay time require

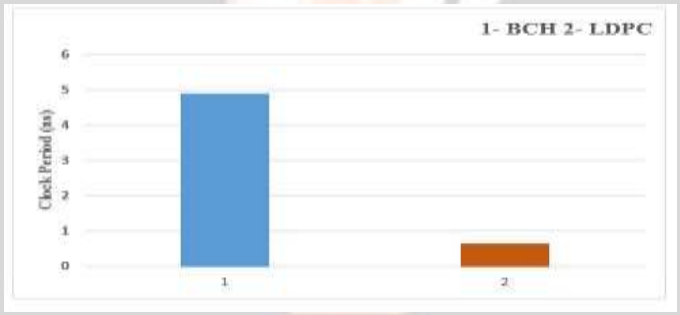

Fig. 8 Clock Period

Fig.8 describes the comparison between the BCH and LDPC. The delay time decreased in LDPC compared to BCH. The proposed LDPCalgorithm provide better performance for storing the bits.

The comparison between the BCH and the LDPC are listed in the table 1.

TABLE I

BCH VS.LDPC

Parameters	BCH	LDPC
No of LUT	36	17
No of flip flop	31	12
Clock Period (ns)	4.919	0.653

V. CONCLUSION

The reliability of the devices measured through the various fault diagnosis in this proposed method. In this paper, the fault diagnosis based on Low Density Parity Check (LDPC) is proposed. The C432 benchmark circuit is programmed with LDPC scheme to diagnosis the stuck at faults in the circuit are performed. The iterative shifting of bits in the register carried out and the fault in the circuit is checked. The benchmark circuit performance reveals the efficient fault diagnosis based on LDPC scheme. The comparative analysis between the existing Bose, Chaudhuri, and Hocquenghem (BCH) model and proposed LDPC confirms the effective fault diagnosis in FPGA.

VI.REFERENCES

[1] M. B. Tahoori, "High Resolution Application Specific Fault Diagnosis of FPGAs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 19, pp. 1775-1786, 2011.

[2] C. Bernardeschi, L. Cassano, M. Cimino, and A. Domenici, "Application of a genetic algorithm for testing seus in sram-fpga systems," in *Proceedings of the 6th HiPEAC Workshop on Reconfigurable Computing (WRC2012)*, 2012.

[3] J. W. Lockwood, A. Gupte, N. Mehta, M. Blott, T. English, and K. Vissers, "A Low-Latency Library in FPGA Hardware for High-Frequency Trading (HFT)," in *IEEE 20th Annual Symposium on High-Performance Interconnects (HOTI), 2012*, pp. 9-16.

[4] Rodri, x, M. A. guez-Blanco, S. Claudio, x, A. nchez, *et al.*, "A Failure-Detection Strategy for IGBT Based on Gate-Voltage Behavior Applied to a Motor Drive System," *IEEE Transactions on Industrial Electronics*, vol. 58, pp. 1625-1633, 2011.

[5] C. Bernardeschi, L. Cassano, M. G. C. A. Cimino, and A. Domenici, "GABES: A genetic algorithm based environment for SEU testing in SRAM-FPGAs," *Journal of Systems Architecture*, vol. 59, pp. 1243-1254, 2013.

[6] K. Shahzad, C. Peng, and B. Oelmann, "Architecture Exploration for a High-Performance and Low-Power Wireless Vibration Analyzer," *Sensors Journal, IEEE*, vol. 13, pp. 670-682, 2013.

[7] M. S. Abdelfattah, L. Bauer, C. Braun, M. E. Imhof, M. A. Kochte, Z. Hongyan, *et al.*, "Transparent structural online test for reconfigurable systems," in *IEEE 18th International On-Line Testing Symposium (IOLTS), 2012*, pp. 37-42.

[8] H. Sidiropoulos, P. Figuli, K. Siozios, D. Soudris, and J. Becker, "A platform-independent runtime methodology for mapping multiple applications onto FPGAs through resource virtualization," in *23rd International Conference on Field Programmable Logic and Applications (FPL), 2013*, pp. 1-4.

[9] E. S. Chung and M. K. Papamichael, "ShrinkWrap: Compiler-Enabled Optimization and Customization of Soft Memory Interconnects," in *IEEE 21st Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2013*, pp. 113-116.

[10] M. Yang, J. Lai, and A. Almaini, "An Architecture Independent Packing Method for LUT-based Commercial FPGA," *Journal of Computers*, vol. 9, pp. 1131-1137, 2014.

[11] A. Ghosh, S. Paul, and S. Bhunia, "Energy-Efficient Application Mapping in FPGA through Computation in Embedded Memory Blocks," in *25th International Conference on VLSI Design (VLSID), 2012*, pp. 424-429.

[12] M. Mozaffari-Kermani, T. Kai, R. Azarderakhsh, and S. Bayat-Sarmadi, "Fault-Resilient Lightweight Cryptographic Block Ciphers for Secure Embedded Systems," *Embedded Systems Letters, IEEE*, vol. 6, pp. 89-92, 2014.

[13] G. Xiaofei and R. Karri, "Recomputing with Permuted Operands: A Concurrent Error Detection Approach," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, pp. 1595-1608, 2013.

[14] F. Pratas, J. Andrade, G. Falcao, V. Silva, and L. Sousa, "Open the Gates: Using High-level Synthesis Towards Programmable LDPC Decoders on FPGAs," *IEEE GlobalSIP*, pp. 1274-1277, 2013.

[15] N. M. A. Freire, J. O. Estima, and A. J. Marques Cardoso, "Open-Circuit Fault Diagnosis in PMSG Drives for Wind Turbine Applications," *IEEE Transactions on Industrial Electronics*, vol. 60, pp. 3957-3967, 2013.

[16] A. Ruan, S. Kang, Y. Wang, X. Han, Z. Zhu, Y. Liao, *et al.*, "A Built-In Self-Test (BIST) system with non-intrusive TPG and ORA for FPGA test and diagnosis," *Microelectronics Reliability*, vol. 53, pp. 488-498,2013.

[17] M. A. Jayarani and M. Jagadeeswari, "A novel fault detection and correction technique for memory applications," in *International Conference on Computer Communication and Informatics (ICCCI), 2013*, pp. 1-6.

[18] H. A. F. Almurib, T. N. Kumar, and F. Lombardi, "Scalable Application-Dependent Diagnosisof Interconnects of SRAM-Based FPGAs," *IEEE Transactions on Computers*, vol. 63, pp. 1540-1550, 2014.

[19] C. Kui, Q. Zhiliang, and C. Bingjin, "Channel capacity and soft-decision decoding of LDPC codes for spin-torque transfer magnetic random access memory (STT-MRAM)," in *International Conference on Computing, Networking and Communications (ICNC), 2013*, pp. 550-554.

[20] A. K. Panda, S. Sarik, and A. Awasthi, "FPGA Implementation of Encoder for (15, k) Binary BCH Code Using VHDL and Performance Comparison for Multiple Error Correction Control," in *International Conference on Communication Systems and Network Technologies (CSNT), 2012*, pp. 780-784.