ERROR AMPLIFIER DESIGN FOR A CLOSED LOOP CLASS-D AMPLIFIER

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ABSTRACT

This paper presents the error amplifier stage design used in the control loop of an integrated Class D audio amplifier and its performance, especially towards EMC, CMRR and PSRR. The entire amplifier is designed using gpdk_090, a generic 90 nm CMOS process design kit. The input stage is biased with 1.8 V and common mode voltage is around 1.66 V. The error amplifier should have a DC gain of 78 dB and the unity gain frequency should be above 80 Mhz. Conducted emissions requirements are taken from the EN55032 standard. Three well-known topologies are compared which are the Two-stage op-amp, Telescopic and Folded Cascode op-amp. Simulations and layout modeling are carried out in Cadence Virtuoso ADE XL.

Keyword: *Op-Amp design, Error amplifier, EMC, Conducted emissions & immunity, Class D*

1. INTRODUCTION

The prominence of electronic systems and devices in all aspects of everyday life has made the Electromagnetic Compatibility compliance a critical concern for every system designer and manufacturer. Failure to comply with EMC standards will prevent a product to enter mass production and increase the time-to-market and cost of the product.

Audio amplifiers are widely used as they are present in communication devices and most modern appliances such as mobile phones, TV, public address, vehicles, computers, etc., where energy consumption tend to be more and more optimized. Consequently, Class-D amplifier has become a common choice due to its high efficiency compared to linear amplifiers. However, as Class-D operates by switching its power stage to the supply rails, the basic model has a serious EMI emission problem and is also susceptible to conducted EM parasites in the power supply. To limit such emissions and increase the PSRR, most modern class D designs don't use the basic open loop model but rather use a feedback loop taken before the LC filter [1] or after it [2]. In these conditions, an error amplifier is required at the input to circumvent the non-linearity of the switching stage and act as a controller stage (Usually PI or PID).

On the other hand, the first stage of a cascaded system will always be the most critical stage to design in terms of noise. Especially, when that stage is designed to have a high gain, its noise term will be amplified by a factor of the gain of the other stages after it. (1) shows the total noise of a three stage system with respectively a gain of A1, A2 and A3 and where $\overline{V_{n,t}^2}$ is the noise density of each stage, expressed in $nV/\sqrt{Hz}$.

$$\overline{V_{n,out}^2} = A2 * A3 * \overline{V_{n,1}^2} + A3 * \overline{V_{n,2}^2} + \overline{V_{n,3}^2} \quad (1)$$

In this paper, we will address the analysis of three major topologies that are commonly used to implement an error amplifier and discuss their characteristics in terms of voltage swing, DC gain and noise (Emissions).

2. BASIC CONCEPT

Although Class-D amplifiers operates by switching its output stage, the overall amplifier behavior could be linearized with a basic inverting amplifier model. That assumption takes place when the PWM switching frequency is much higher than the signal bandwidth [3].

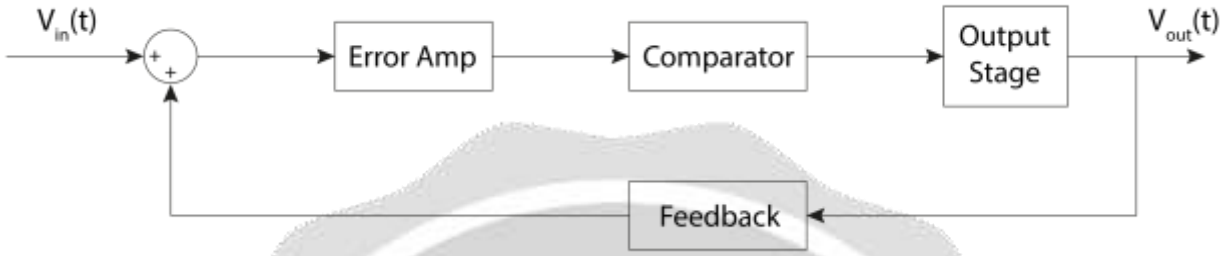


Fig -1: Function block of the Class-D amplifier

The error amplifier is implemented to provide high differential gain to suppress odd order harmonic distortions and differential noise.

As we have two different reference voltages for power stage and control stage (formed by the input, error amplifier and comparator), elements of the feedback loop, mainly composed by resistors, acts as a voltage divider and set the common mode voltage at the input of the error amplifier. Table-1 below shows the specifications that the herein error amplifier must satisfy.

Table -1: Error Amplifier design specifications

Parameter	Specified value
Technology	GPDK 90-nm
Supply voltage, V_{DD}	1.8 V
Common-mode voltage, V_{CM}	1.66 V
Unity gain frequency (f_{un})	> 100 MHz
Open-loop gain (A_{OL})	> 78 dB
Slew-rate (SR)	> 100 V/µs
Phase margin ($\emptyset_M$)	> 55 deg
Noise	45 µVrms

For the sake of clarity, it is worth to mention the following definitions and the difference between a component and a function. The following are components and may be used for many functions:

- Comparator: have an analog input and a digital output (logic level)
- Op-amp: have an analog input and an analog output (a voltage)
- OTA: have an analog input and an analog output (a current)

Whereas an error amplifier is a function, not a component, and may use a variety of components such as an Op-amp or an OTA to perform its function which is: comparing a desired reference with the actual value. Then produces an output that is proportional to the difference, the differential or the integral of the difference between the two values.

Thus, since we chose to use an Op-amp to implement the error amplifier, the above requirements apply to the operational amplifier and to avoid confusion, when we mention the Op-amp, we are referring to an Op-amp performing as an error amplifier.

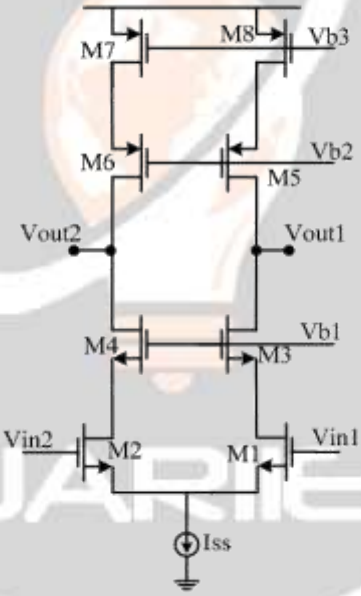
3. INPUT STAGE TOPOLOGIES

There are various architectures available for a differential op amp. Three major architecture that are widely used are implemented and discussed below.

3.1 Telescopic Cascode

The typical design of a telescopic Cascode is shown in Fig-2. The input differential pair M1-M2 injects the signal current into common gate stages. The transistors are placed one on the top of the other to create a sort of Telescopic composition. The appellation came after the fact that the structure in which MOSFETs on each branches are connected along a straight line like the lenses of refracting telescope.

This topology has a high gain compared to a simple differential pair and has also a lower noise factor. Another advantage of a telescopic Cascode is its high common mode and supply rejection ratio ensuring constant performance parameters. That makes the telescopic Cascode a suitable option to implement the error amplifier.



However, due to its numerous stack of transistors, it has a smaller voltage swing than other topologies.

Fig -2: Telescopic Cascode Operational Amplifier

3.2 Folded Cascode

Another Op-amp topology that is commonly used is the folded Cascode (Fig-3). Compared to the previous topology, it has a better frequency response and a higher unity gain frequency. Since the input transistor is not stacked with the Cascode transistor, it has more margin while performing under a low bias voltage. Folded Cascode op-amp (FCOA) improves the ICMR and PSRR to a decent level. The FCOA uses cascading at the output stage combined with differential amplifier, that results in achieving good ICMR.

This topology also provides larger output swing than the ordinary conventional telescopic amplifier although it consumes twice the current than the telescopic. The folded Cascode is more widely used than the telescopic Op-Amp [4]. The FCOA possess a very important property which allows the input common-mode level to be close to supply voltage. With PMOS input, the input common-mode level can be as low as 0V while one with NMOS input

would reach the supply voltage V_{DD}. As compared to ordinary op-amp, folded Cascode provides high gain with large output swing and is a single-pole op-amp. The major advantage of single-pole op-amp is that it provides great stability and large phase margin [5].

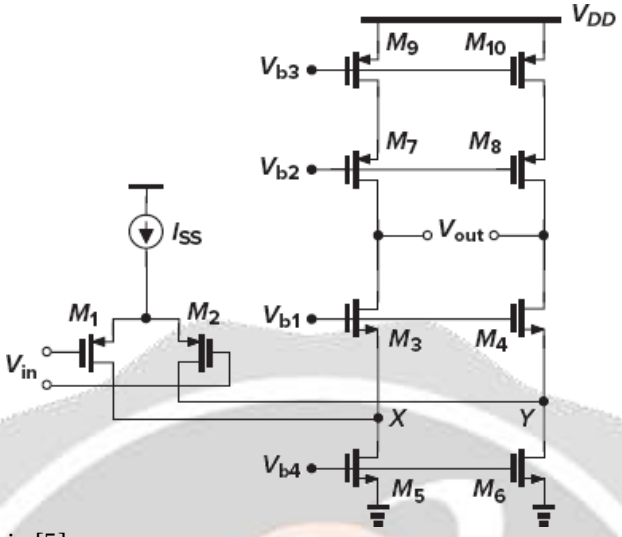


Fig -3: Folded Cascode Operational Amplifier

3.3 Two-stage operational amplifier

The last topology we are going to look at is the basic two-stage operational amplifier. The second stage is here added to improve the gain of the first stage and enhance the output resistance. Bias voltages are designed in a way that all transistors must operate in saturation.

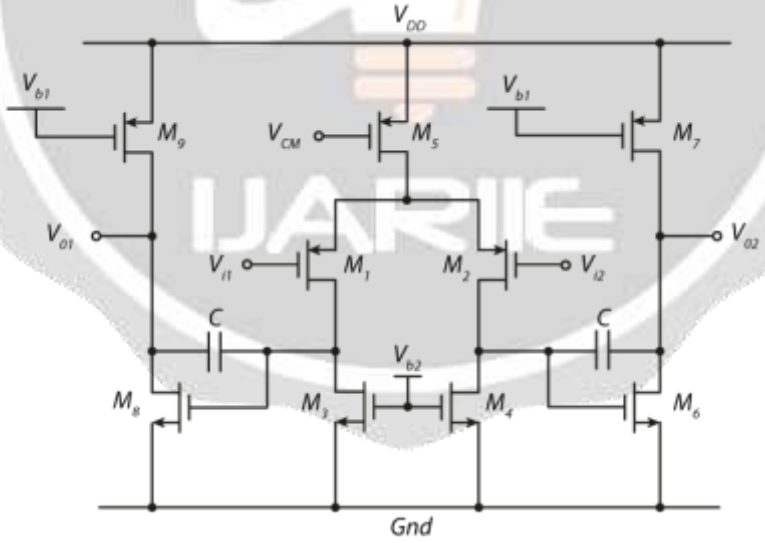


Fig -4: Two-Stage Operational Amplifier

The first stage of two-stage amplifier having differential inputs whose function is to convert given input voltage to current. The second stage is basically a common source amplifier whose work is to convert current to voltage. The total DC gain of this two-stage structure can be expressed as:

$$A_v = Av_1 * Av_2 \quad (2)$$

Where,

Av_1: gain of the first stage
Av_2: gain of the second stage

The DC gain (2) can also be expressed as:

$$Av = g_m * R_{out} \tag{3}$$

Where,

g_m: transconductance of the input network
R_{out}: equivalent output resistance

This topology has a high output voltage swing. However, due to the two stages in its design, it has a higher power consumption and a poor PSRR at higher frequency.

4. DESIGN AND SIMULATION

4.1 Biasing circuit

The first step of a design would be the definition of the bias current and voltages of the MOSFETs. Bias current, as a design parameter could be obtained by the transconductance equation [6]

$$g_m = \frac{2I_D}{\Delta V_{GS}} \tag{3}$$

In our design, a current of 20 µA is used as a reference current. A BMR circuit [7] (Fig-5) is designed and used as a bias circuit. A multiplier of K=4 was chosen so that $M1 = 40/1$. The transconductance of M1 at $I_D = 20\ \mu A$ is $g_m \approx 130\ \mu A/V$ and gives the value of the resistance $R = 7.702\ k\Omega$

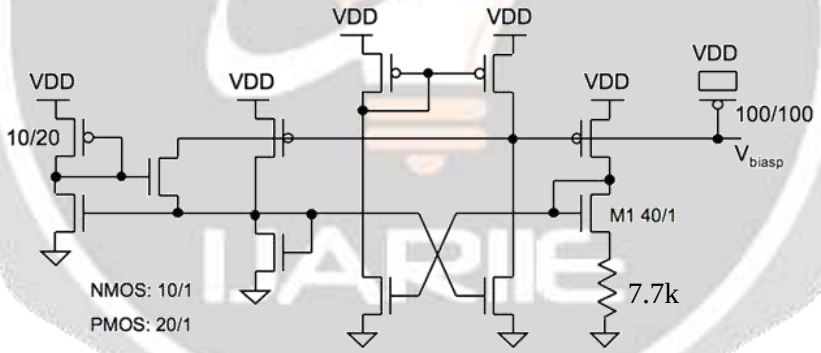


Fig -5: Beta-Multiplier reference and start up circuit [7]

The BMR voltage is fed into the biasing circuit shown in Fig-6. $V_{bias1-4}$ set the voltages for the current sources seen in Fig-2-4 for our test circuit. Table-2 shows the simulated values of each bias voltages.

Table -2: BMR Bias voltages

Parameter	Value
V_{DD}	1.8 V
V_{bias1}	1.38 V
V_{bias2}	1.16 V
V_{bias3}	539.4 mV
V_{bias4}	377.5 mV
V_{pcas}	966.8 mV

V_{ncas}	800 mV

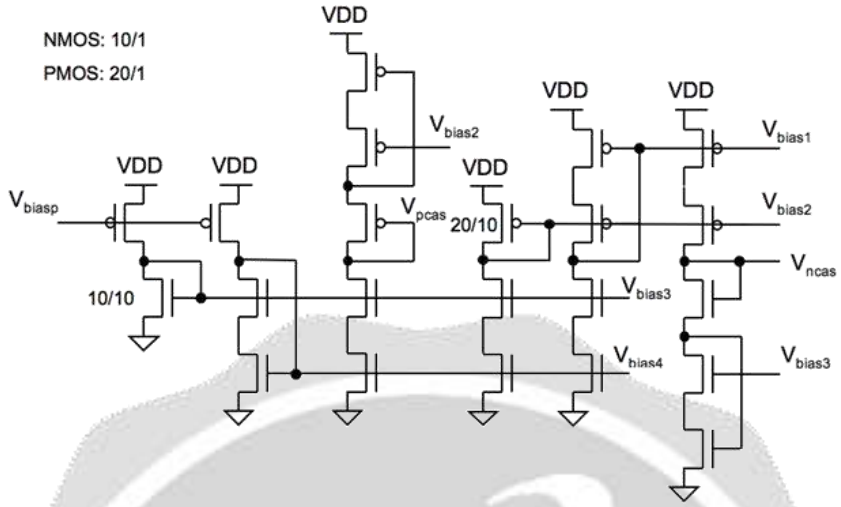


Fig -6: Short channel biasing circuit.

4.2 Common-mode feedback

We are implementing a fully differential Op-amp. Thus, a CMFB have to be implemented to prevent any transistor for going into triode region and compromising stability. The CMFB presented in [8] have the advantage of being flexible and stable for an internal common-mode feedback.

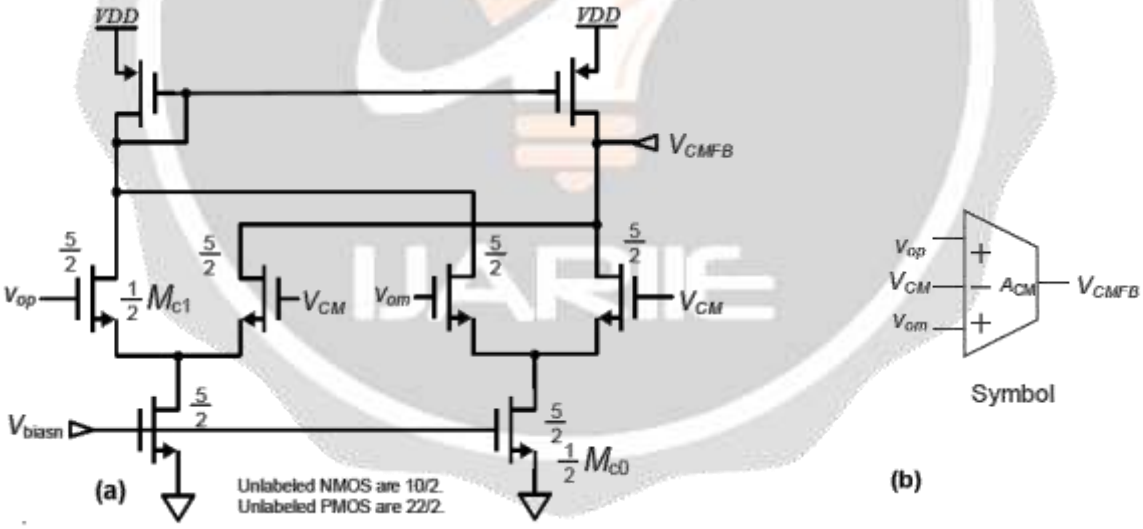
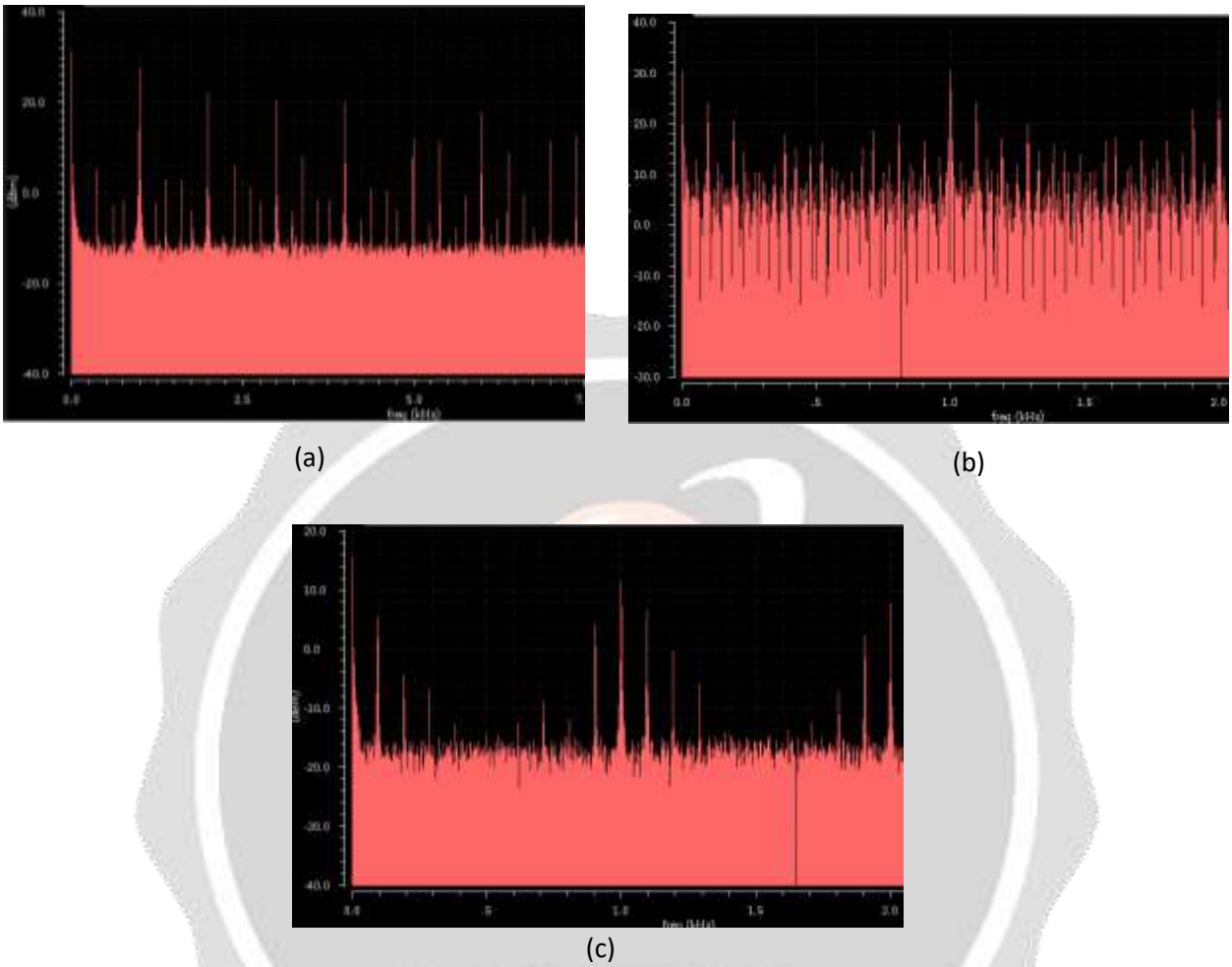


Fig -7: Common-Mode Feedback.

4.3 Simulation results

To have a fair comparison between the proposed topologies, we kept transistor sizing to a proportional value and all parameters external to the amplifier are also left unchanged.
After all parameters being set, simulation was carried on using Cadence Virtuoso ADE L and ADE XL. DC gain, phase margin and unity gain frequency are obtained with the ***stb*** analysis and emissions are done with transient ***dft***



(a) (b) (c)

Fig -8: FFT plot of a 1 kHz input signal for: Two-stage (a) - Telescopic (b) and Folded Cascode (c) op-amp

Table -3: Performance comparison between op-amp topologies

Topologies	Gain	Output swing	Power dissipation	Noise
Telescopic cascode	Medium	Medium	Low	Medium
Folded cascode	Medium	Medium	Medium	Medium
Two-stage op-amp	High	High	Medium	Low

5. CONCLUSION

As a major part of conducted and radiated emissions will couple through power supply rails and input path, the input stage, as a high gain stage, should be well designed to withstand EM perturbations. From the theoretical study of Two-stage op-amp, Telescopic and Folded Cascode presented in this paper, it is concluded that for our application, as long as we implement the CMFB, the common-mode voltage will not be a major issue for the choice of a given design. For our application, the gain matters the most, as all the other parameters will lie on the DC gain and the unity gain frequency of the stage. Consequently, for our application, a two-stage topology will be the most efficient. Moreover, the overall voltage swing of a Folded-Cascode Op-Amp is only slightly higher than that of a Telescopic

configuration. This advantage comes at the cost of higher power dissipation, lower DC gain and higher noise, although this topology makes it possible to handle input CM levels that are close to one of the supply rails. On the other hand, with telescopic op-amps, three voltages must be defined carefully, which are the input CM level, the gate bias voltage of the PMOS and NMOS cascode transistors, whereas in folded-cascode configurations only the latter two are critical. In terms of noise, all three topologies have quite the same response.

6. REFERENCES

[1]. Gaël Pillonnet, Remy Cellier, Angelo Nagari, Philippe Lombard, Nacer Abouchi. Sliding Mode Audio Class-D Amplifier for Portable Devices Powered by Editorial Manager® and Preprint Manager® from Aries Systems Corporation. Analog Integrated Circuits and Signal Processing, Springer Verlag, 2013, pp.13. hal-01103622

[2]. Roberto Mrad, Florent Morel, Gaël Pillonnet, Christian Vollaire, Angelo Nagari. Integrated Class-D audio amplifier virtual test for output EMI filter performance. Conference on Ph. D. Research in Microelectronics and Electronics, IEEE, Jun 2013, Villach, Austria. pp.4, 10.1109/PRIME.2013.6603127. hal-01103590

[3]. Wang W C, Lin Y H. 5.2 A 118dB-PSRR 0.00067%(−103.5dB) THD+N and 3.1W fully differential Class-D audio amplifier with PWM common-mode control[C]// IEEE International Solid-State Circuits Conference. IEEE, 2016.

[4]. Pallavi Kothe, "Design and Characterization of Low Power Folded-Cascode Operational Amplifier", International Conference on Recent Trends in Engineering Science and Technology (ICRTEST 2017) ISSN: 2321-8169-425 – 427 Volume: 5 Issue: 1(Special Issue 21-22 January 2017).

[5]. Zhang Kun+, Wu Di and Liu Zhangfa," A High-performance Folded Cascode Amplifier", International Conference on Computer and Automation Engineering (ICCAE 2011) IPCSIT vol. 44 (2012), DOI: 10.7763/IPCSIT.2012.V44.8.

[6]. Carusone, Tony C, David Johns, Kenneth W. Martin, and David Johns. "Analog Integrated Circuit Design". Hoboken, NJ: John Wiley & Sons, 2012. pp. 24-30

[7]. R. J. Baker, CMOS circuit design, layout, and simulation. Piscataway, NJ: Wiley, 2008, pp. 613–823.

[8]. Saxena Vishal, "ECE 415/515 –Analog Integrated Circuit Design", Presentation