

# FUNCTIONAL VERIFICATION OF USB 2.0 VIP USING SV- UVM

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## ABSTRACT

*This paper presents the verification of Universal serial Bus 2.0 using System Verilog- Universal Verification Methodology. At present as technology is increasing rapidly communication have become an important part of digital world. Some of the main features of USB are speed negotiation, data transfer, device detection. Test cases have been written to verify the functionality of the design. All the simulation work have been carried in Mentor Graphics EDA tool Questa Sim.*

**Keyword :** - Questa Sim, USB 2.0, SV, UVM.

## 1. INTRODUCTION

The use of many digital peripherals for exchange of data between the computing devices is been increasing day to day which leads to the design of USB protocol which have many advantages over the other peripheral protocols. Universal Serial Bus (USB) came from several considerations like ease-of-use, Port expansion etc. to meet this specifications requirement. User Application media like audio, video, voice have full support to the protocol to most of PC's peripherals, etc and other computing devices. Comprehension of various PC configurations and form factors make the USB a multifunctional protocol capable of servicing various solutions. The USB is a generic protocol making its interface capable of quick diffusion into product.

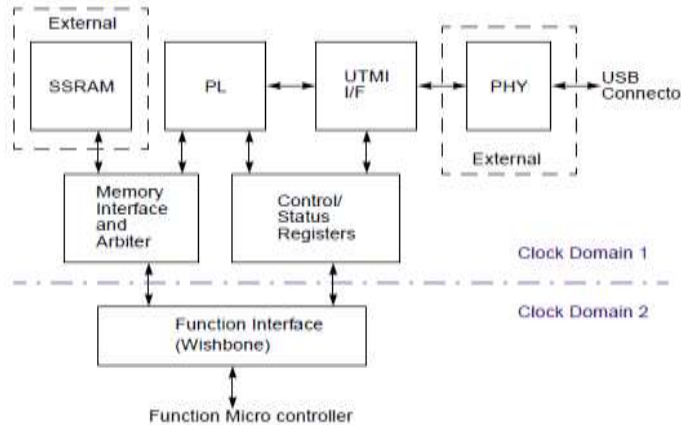
The USB is still the answer for connection of computer peripherals, PC and mobile architectures and also for consumer electronics. It is a bidirectional, fast, dynamically attachable and low-cost interface which fulfils the requirement of interconnection.

Earlier Versions of USB Specification:

1. USB 1.0: Released in January 1996. Specified data rates of 1.5Mbit/s (Low-Bandwidth) and 12Mbit/s (Full Bandwidth). Does not allow for extension cables or pass through monitors (due to timing and power limitations).
2. USB 1.1 Released in September 1998. Fixed problems identified in 1.0, mostly relating to hubs.
3. USB 2.0: Released in April 2000. Added High maximum bandwidth of 480 Mbit/s [60 MB/s] (now called "Hi-Speed").
4. USB 3.0: Released in November 2008. Now called Superspeed Bus having higher data rates of 5Gbit/s.

This study is to verify the functionality of the USB .Section II represents the architecture overview for USB.Section III represents the methodology used.Section IV represents simulation results for different testcases.Section V is conclusion.

**2. ARCHITECTURE OVERVIEW**



**Fig -1:USB 2.0 Architecture [1]**

The figure below illustrates the overall architecture of the core.It consists of blocks like UTMI I/F , Host interface which is w/b interface , SSRAM, Protocol layer , Memory interface and arbiter and control & status registers.

1. Protocol layer: It is responsible for all USB I/O and control communications. It defines that after it has received token then only it will send data packet.
2. SSRAM: It is single ported synchronous SRAM. It is used for temporary data storage.
3. Wishbone Interface : The host interface is wishbone interface .
4. UTMI interface: This block is used for tracking interface state. It consists of internal state machine which is responsible for speed negotiation.
5. Control & Status Registers : This registers are to indicate the functionality of the design and status whether it is suspend ,reset, resume.

**2.1 Features of USB 2.0 :**

**Table -1:** Features and operations to be verified

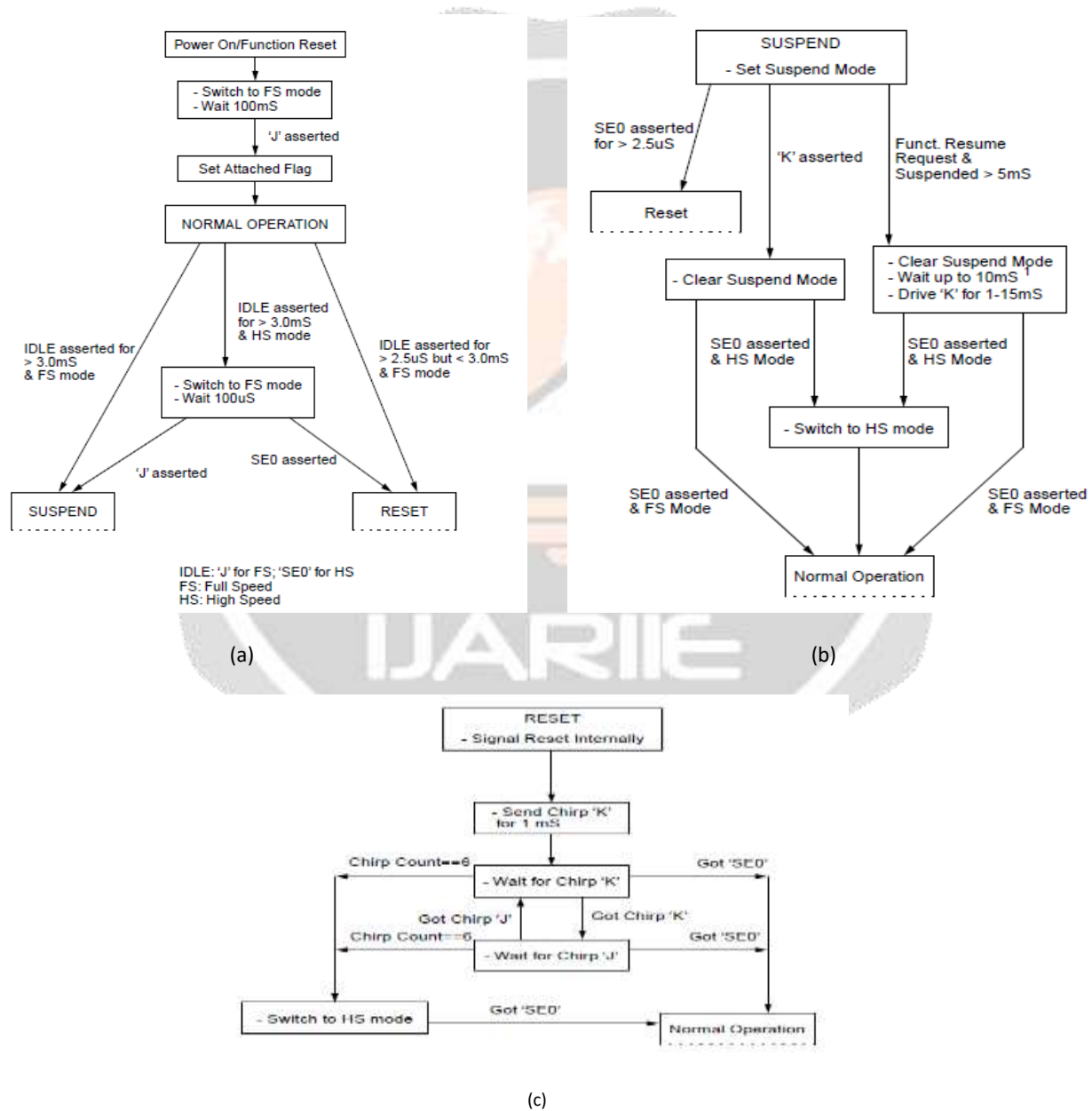
Sr. No.	Features	Description
1.	Device Detection	Host Recognizes LS or FS based on this.
2.	Speed Negotiation	Host Figures out if FS device supports HS by using speed negotiation.
3.	Enumeration	Read device information stored in device descriptor registers.
4.	Normal Data transfer	Token Packet -> Data Packet -> Handshake Packet

**2.2 USB device processing:**

USB provides a special mechanism to control the attached devices beyond data exchange.

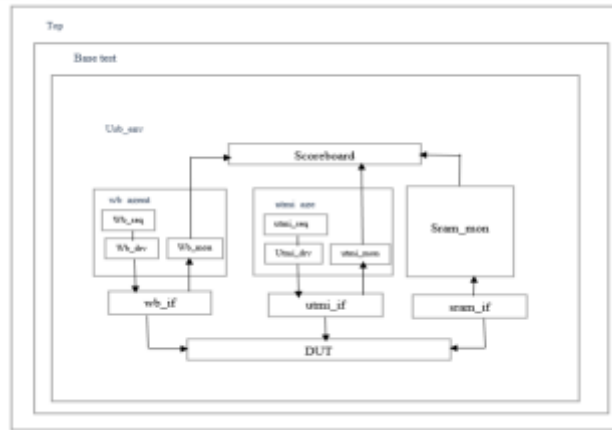
1. Reset
2. Suspend/Resume
3. Speed Negotiation

There is one state machine in the device which is utmi\_linestate which is responsible for this. After entering into POR state, it asserts J, wait for 100 ms and sets attach flag. Then it moves to reset and suspend state. Reset state means that it can start speed negotiation process.



**Fig -2 :** (a)USB Device Processing , (b)USB suspend processing, (c) USB reset processing [1]

### 3. METHODOLOGY



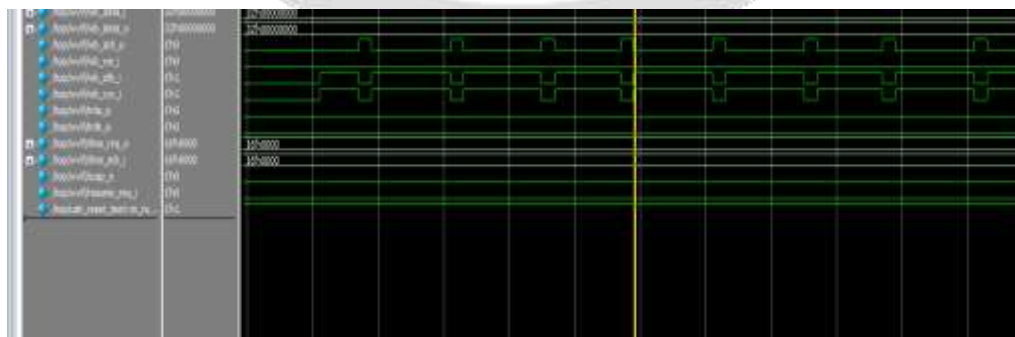
**Fig -3 : USB 2.0 UVC**

The modelling of USB 2.0 VIP is been done using UVM Methodology. The need of VIP is to verify the SoC. The VIP has 2 agents namely wb\_agent and utmi\_agent. The agents have their respective driver and sequencer. There is a top module in which the environment, interface, test library, coverage are instantiated. Figure 3 shows USB 2.0 universal verification component.

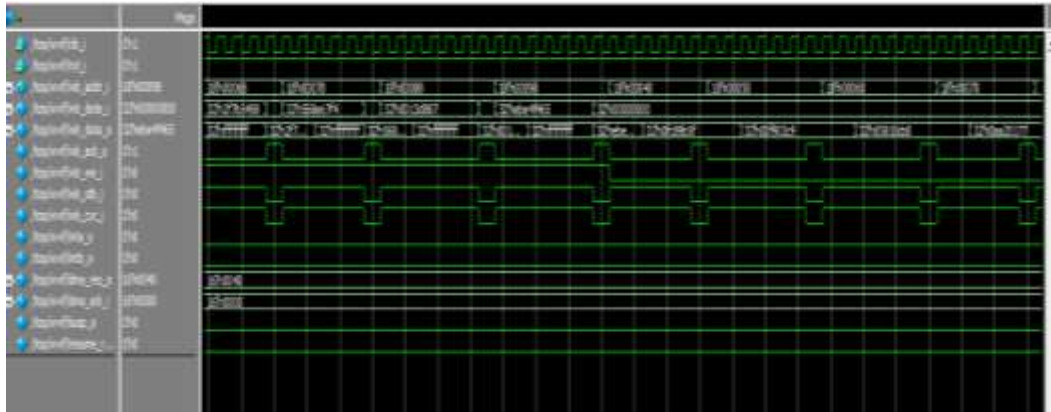
1. The sequence item : It has all signals related to VIP. The rand, constrained properties of system Verilog is used in sequence item to generate valid transactions.
2. Driver : It drives DUT signals. It receives transaction object from the sequencer and converts it into the pin level signal to the interface.
3. Sequencers: It is used to run the sequences when driver demands it.
4. Monitor: Monitor monitors all the transaction coming at the interface.
5. Agent: It is extended from uvm\_agent.
6. Environment: It is environment of the VIP. It is used to encapsulate the VIP.

### 4. VERIFICATION RESULTS

This section shows the verification results for testing the functionality of design. The first testcase for any SoC level verification is reset the register and read the value of register. Next testcase is write read. In this first registers are written and then read, In this we compare both write and read value.



**Fig -4 : Register reset testcase**

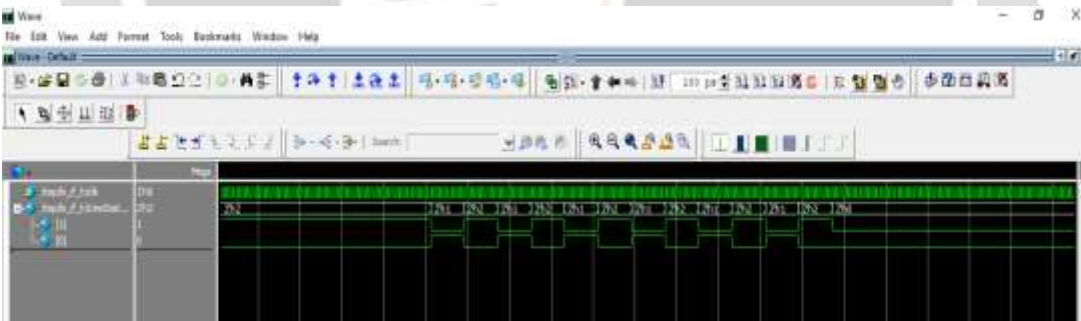


**Fig -5 : Register Write-read Testcase**

Figure 5 and 6 shows the waveform of wishbone signals.

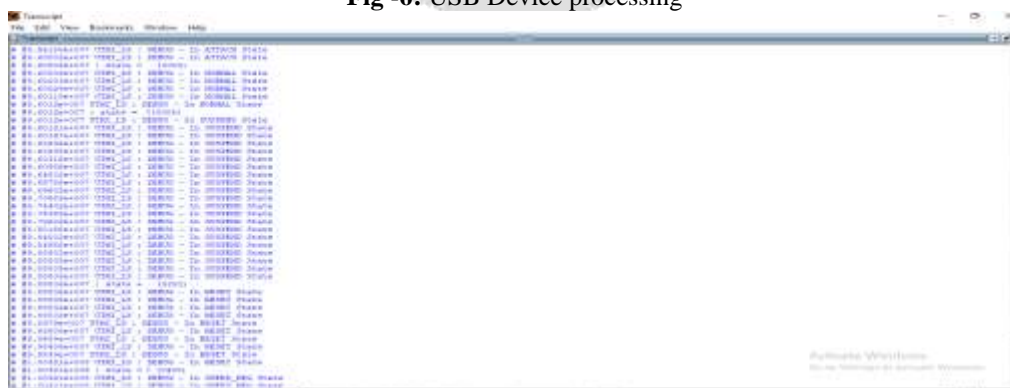


(a)



(b)

**Fig -6: USB Device processing**

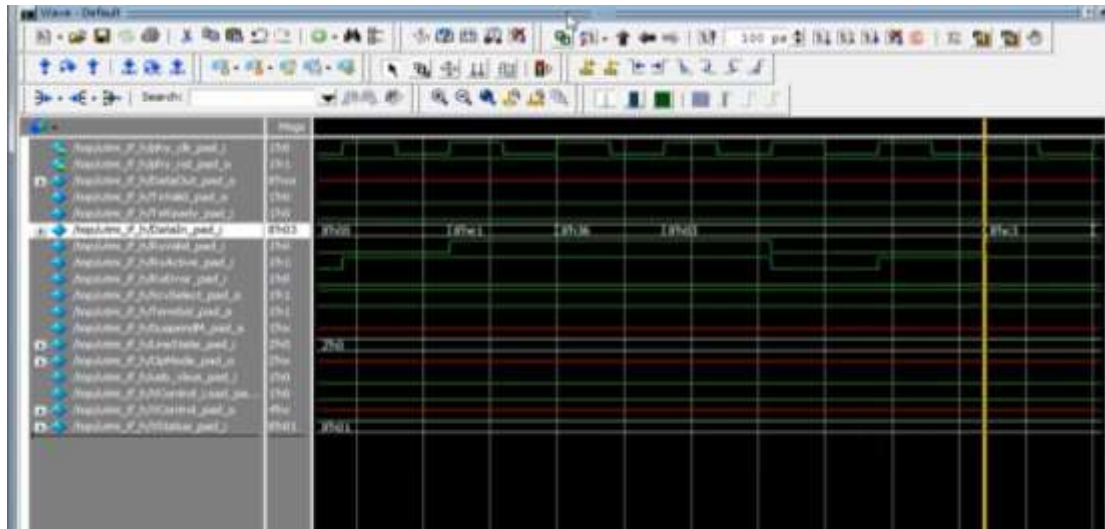


**Fig -7 : Transcript Window**

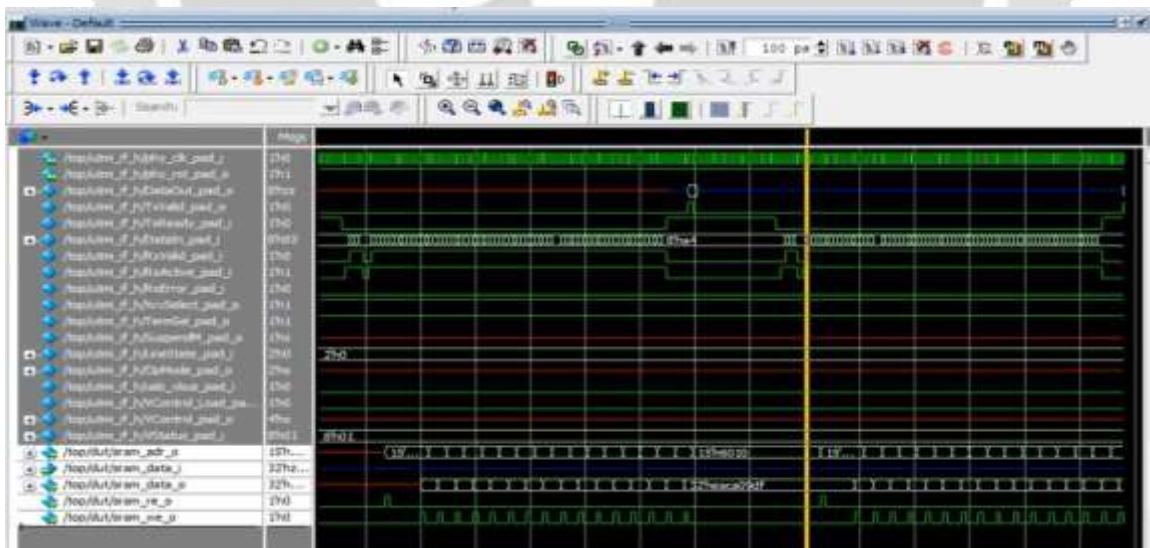
The figure 6 and 7 shows the waveform for USB device processing. After entering into reset state it enters into FS mode, asserts J waits for 100ms and sets attach flag. Then enters into normal operation. If J is asserted for more than 3 us then enter into suspend state mode. If SE0 is asserted for more than 2.5 us it enters into reset state.

After entering into reset state the device will send chirp K to host. After receiving host will acknowledge by sending 6 KJ chirp pattern, If SE0 comes in between it will move to High speed.

Figure 8 shows the waveform of utmi and sram signals for out data transfer. Since out transaction is from host to device. UTMI has two sub interfaces Rx and Tx interfaces



(a)



(b)

**Fig -7 : Data Transfer**

In out transaction token and data packets are send on Rx interface and handshake packet is sent on Tx interface. When Rx active and Rx valid is asserted then we receive token PID 8'he1 which is of 8 bits. After 3 bytes of token is received Rx active and valid is deasserted. Then again Rx active and valid are asserted we receive data

packet 8'hc3. Then after we receive 8'hd2 handshake packet. For all packet transfer we see transactions happening on SRAM.

## 5. CONCLUSION

In this verification environment for USB 2.0 is verified using SV- UVM Methodology. USB features like data transfer , speed negotiation , device enumeration has been verified.

## 6. REFERENCES

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