HIGH SPEED WALLACE TREE MULTIPLIER

[1]AARTI SHARMA, [2]ANMOL RUSTAGI, [3]AKRITI SINGH, [4]DEEPALI GUPTA, [5]PRAVEENA PRABHAT

Electronics and Communication Engineering
ABES Engineering College, Ghaziabad,India

Abstract

Now a days multiplication is an important arithematic operation in various systems like RISC Processor, Digital Processing Units and also for graphics and science computations etc. There have been various types of multipliers with digital design made, for example- Booth, Braun array, Modified Booth, Wallace Tree, Dadda and Ferrari – Stefanelli multipliers. All these multipliers have different speeds, areas and efficiency and these factors play an important role in deciding delay, area and consumption of power factors for the whole system. Hence improving any of the factors will lead to improvement in whole system. By changing the design by insertion of new technology at the implementation level can bring make viable in existing architecture and algorithms. This presents an approach towards reducing the delay of a Wallace multiplier by taking help of compressors in full as well as half adders to reduce partial product. The analyzed multiplier using Xilinx ISE Design Suite 14.7.

Keywords—*VHDL,Simulation*

I. INTRODUCTION

A change in design by the insertion of a new technology at the implementation level can bring viable an existing architecture and marginal algorithm. In present days speed, area and power are important conflicts in VLSI design technology, because of consistently increasing demands for rapid operations. Many technologies have been used to achieve high speed and low power digital circuits and among that pass transistor logic has been intensively studied as a breakthrough for producing new advancement in the field of digital circuits. In digital systems architecture are well established in the literature to develop modern arithmetic processors and use of latest innovations as well as advanced technologies dedicated to special logic circuits. Specifically the multiplier design is usually critical in signal processing applications of digital system where it requires larger number of multiplications. The multiplication operation is used in digital system for various applications and multipliers are important integral of the system like ALUs and DSP processors. The system performance majorly depends on the multiplier because they are often called the slowest components. So reduction of delay is important in this research.

This can be defined as a hardware implementation of a circuit which is used to multiply two integers, as adviced by Australian scientist in computer science. Wallace tree multiplier is fast multiplier compared to the easily accessible multiplier as they are used to save addition bits in the algorithm for the final product addition. In multipliers if there is a small increase in speed will improve the frequency of operation of a digital signal processor. Therefore, many new techniques are used on multipliers to make it faster.As when a multiplier is designed, high speed and delay can be produced. Hence, to reduce it, compressors and adders are used. The proposed multiplier uses highly efficient compressors such as 4:2 compressors to reduce delay and to achieve high speed. The higher order compressors are developed by merging binary counter property with compressor property. The design of Wallace tree multiplier consist of three essential steps.

1. Generating partial products.

2. Reducing partial products.

3. Sum-mission of partial products reduced to result in the final product.

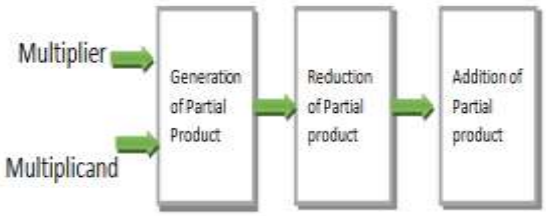

Fig 1. Block diagram of Wallace Tree Multiplier

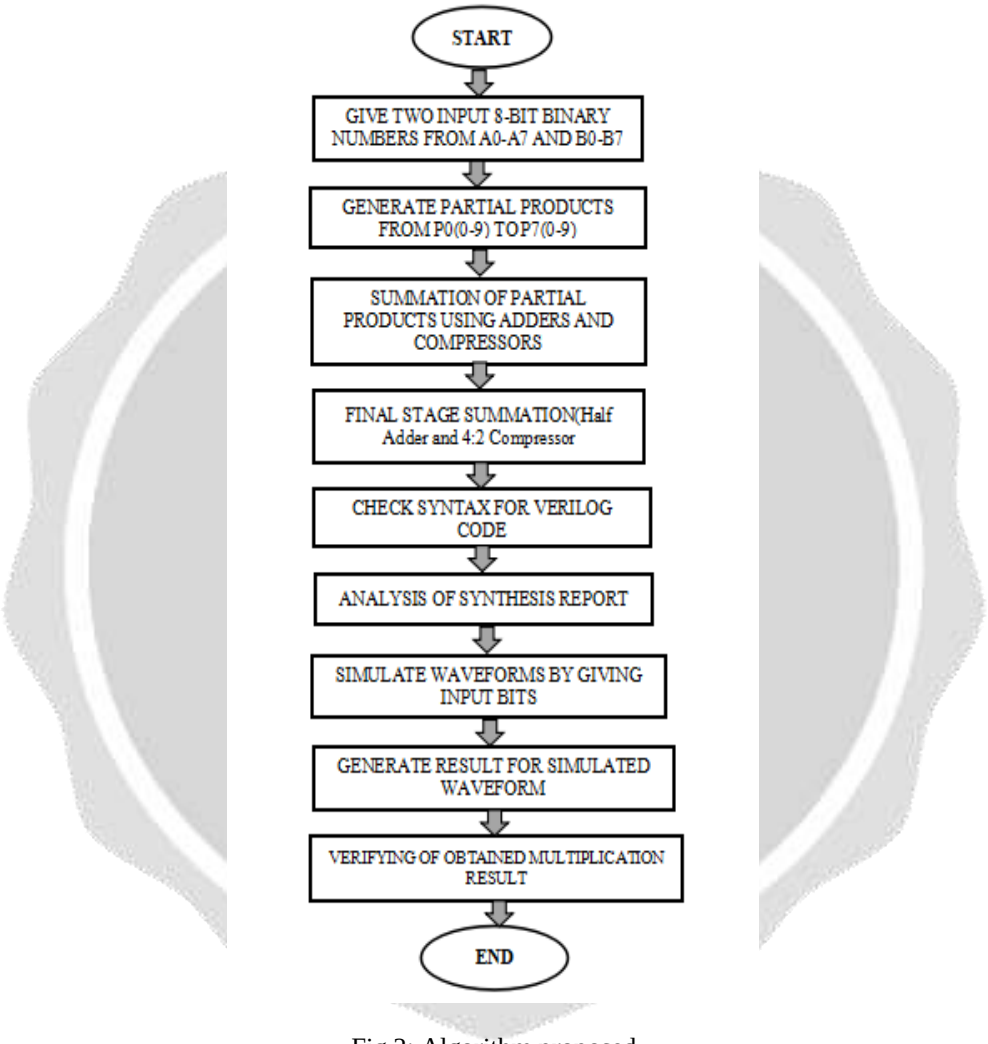

Fig.2: Algorithm proposed

II. PROPOSED WALLACE TREE MULTIPLIER ARCHITECTURE AND DESCRIPTION

An NxN multiplier, a partial product product reduction having height stage predetermined for having a multiplication with less delay and higher speed. After partial product is generated, in the upcoming stage the highest stage height. In our method the height of the defined stages is $2^{(n-j)}$, where 2^n is smaller integer near to N and j range is 0 to n-1.

The heights of stages are given by:

For Stage 2 = 2^n, For Stage 3 = 2^{n-1},

For 4^{th} stage = 2^{n-2}... Up to level 2 of final stage.

The given scheme is practiced using the 4:2 compressors while the height of stage are maintained.

The max. Of level 1 i.e. the stage of partial product is having eight bits and near 2^n integer less then 2^3 is four. Now the height of level 2 is 4 bit, that is the max. Height of the column. Now since the Wallace tree is for 8*8 bit hence here we examine each column and the reduction is given by:

a) C1 to C4 and C13 to C15 have heights less than or equal to 4 bits, therefore columns remain unchanged.
b) Col.5 is having 5 bits so, it is reduced to 4 bits by using a half adder.
c) Col.6 is having 6 bits and carry bits given by Col.5. Hence we use 4-2 compressor for reducing the height to 4 bits.
d) Col.7 is 7 bits and has a carry bit by Col.6, hence a half adder and a 4-2 compressor are used to make it of 4 bit height.
e) Col.8 is 8 bits long and has 2 carry bit from Col.7. Hence two 4-2 Compressors are used.
f) Col.9 is 7 bits long and has 2 carry bits from Col8. This uses two 4-2 bit compressor is used with one compressor having one input as zero.
g) Col.10 is 6 bits and 2 carry bit and a Cout from Col.9. Therefore a 4-2 compressor and full adder are used to make it height to 4 bits.
h) Col.11 is 5 bit long and 2 carry bits from Col.10. Therefore, a single 4-2 compressor is used.
i) Col.12 has 4 bits and a carry bit and a Cout given by Col.11. So, a half adder is used.

Now the next stage height is given by $2^{2-1} = 2$. The number of reduction steps have column height more than 2 and is given as follows:

a) Col., Col.2 and Col.15 remains unchanged, Col.3 have 3 bits hence, a half adder is used to make its height 2 bits.
b) The Col.4 has 4 bits and a carry given by Col.3. Thus 4-2 compressor is used.
c) A 4-2 compressor is used in each column, Since Col.5 to Col.12 is having 4 bits.
d) Col.13 is having 3 bits and carry and Cout from Col.12 hence, a 4-2 compressor is used.
e) Col.14 is having 2 bit. Hence, a half adder is used.

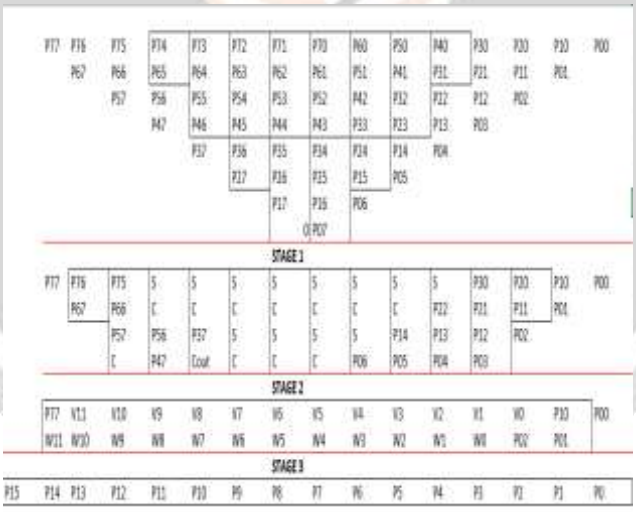

Fig 3: Architecture of proposed Wallace Tree Multiplier

Now after stage 1, having every column height equal to or less than 2 bits. Therefore, it is the last stage and all reduction stages are complete after this last stages is performed by CPA(carry propagation adder) which produces carry for final outputs of multiplier.This introduced 8x8 multiplier is using 13 full adder, 18 4-2 compressor and 7 half adders.

The 4x2 compressor can be used for proposed reduction format, in NxN no. Of multipliers where N>=4 to have an higher speed and less transistor count even than that of wallace tree multiplier having 4x2 count. For example a 10x10, 12x12 or 16x16 will have heigher bits like 8,4 or 2.

III. ANALYSIS OF IMPLEMENTATION DESIGN AND CONCEPT

The Wallace tree here is implemented by using half adders,

Full adders and 4-2 compressors.

1)Half adder

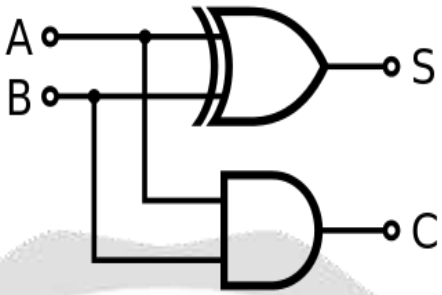

Fig.4**:** Half adder logical circuit Sum= a (Ex-or) b; Carry= a.b

Half adder is used in designing of Wallace Tree multiplier. Two inputs are provided to the half adder with generate output as sum and carry. The truth table of half adder is given as:

Input(A)	Input(B)	S(sum)	C(carry)
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Table 1: Half adder truth table.

2)Full Adder

A full adder performs binary logical addition a three one bit binary numbers. The full adder produces two outputs Sum and carry for three one-bit inputs.

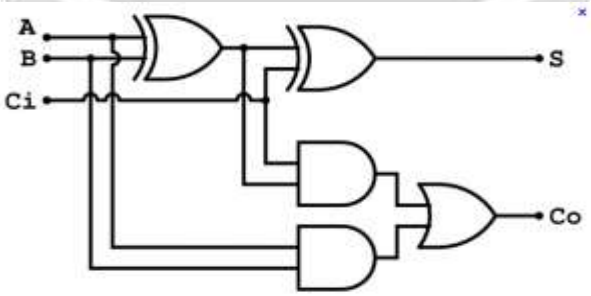

Fig 5: Logic diagram of Fulladder

SUM = (A XOR B) XOR Cin = (A ⊕ B) ⊕ Cin

CARRYOUT = A AND B OR Cin(A XOR B) = A.B + Cin(A ⊕ B)

3) 4-2 compressor

A 4-2 compressor is a combinational device which compresses 4 bit parity product into two bit parity product. The block diagram is shown in figure 1 (a). It accepts the inputs M1, M2, M3, M4 and Cin and produces three outputs namely S(Sum), C(Carry) and Cout. Cin is the output of compressor of lower stage and Cout serves as input to the compressor of higher stage. X1, X2, X3, X4, Cin and S(Sum) are equally weighed as i and Carry is weighed one binary bit order higher i.e. i+1. The property of a compressor which makes it better than a full adder is that Cin is independent of Cout and vice versa. The 4:2 compressor is implemented using 2 serial full adders as shown in Fig. 6.

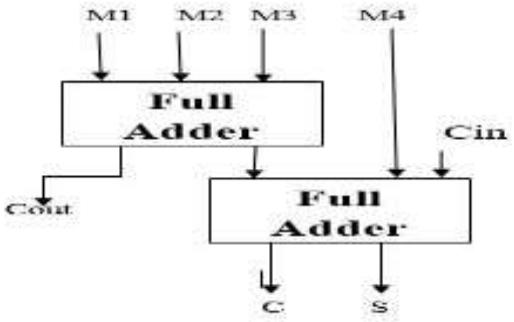

Fig 6: Logic Diagram for 4-2 compressor using two full adders.

S = m1 XOR m2 XOR m3 XOR m4 XOR Cin

Cout = m1 XOR m2 m3 + m1.m2

C = (m1 XOR m2 XOR m3 XOR m4) Cin + (m1 XOR m2 XOR m3) m4.

IV. RESULTS AND DISCUSSION

The Wallace tree multiplier designed for 4bit, 8-bit, 16-bit. The obtained results will be simulated and synthesized using Xilinx ISE 14.7,and synthesis report will be given. For input of x and y both are 8 bits then output generated will be of 16 bit.

Given by using the above reduction format in multipliers, the output result and the reduction stages are reduced also Power Delayy Product(PDP) gets reduced as 4-2 Compressors have less delay and less no. Of interaconnections as compared to multipliers with full adder cells. The present format provides faster speed formats as compared to Wallace tree multipliers with full adders.

Fig 7: Simulation result of Multiplier using Compressors.

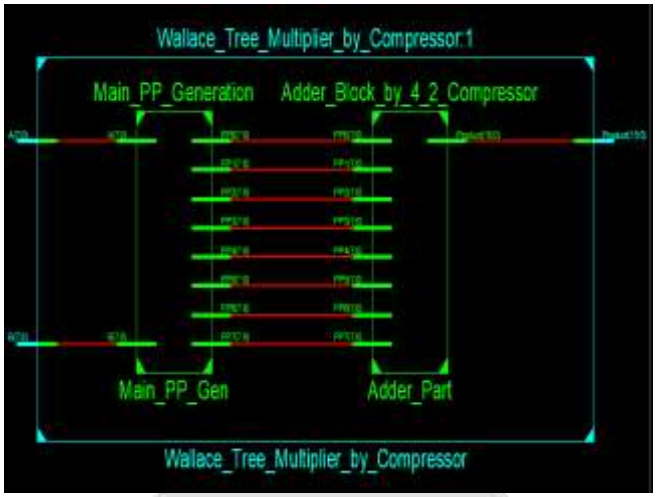

Fig 8 : RTL Schematic view of Wallace tree using 4:2 compressor

METHOD NAME	MULTIPLIER NAME	NORMAL WALLACE TREE MULTIPLIER	WALLACE TREE MULTIPLIER USING COMPRESSOR
AREA IN NUMBER OF LUT	LUT	176	137
	GATE COUNT	97	822
	SLICES	1056	77
MEMORY IN kilobytes	SIZE	243608 KILOBYTES	177360 KILOBYTES
DELAY	DELAY	44.844ns	30.528 NS
	GATE OR LOGIC DELAY	19.138 NS	147.91 NS 46.4 LOGIC
	PATH OR ROUTE DELAY	26.7NS 58.3 LOGIC	16.349NS 53.6 LOGIC

Table2: Total device utilization review of multipliers.

V. CONCLUSION

The analysis design of Wallace tree multiplier is implemented in verilog. The simulation and synthesis results for 8-bit Normal and 8 bit multiplier using compressors are obtained. The code is simulated using Xilinx ISE 14.7.The results are analyzed in terms of speed, successive two major weights after arrival of sum bit maximum combinational path delay, logic delay, route delay for different multipliers. For 8*8 Wallace tree architecture the maximum combinational path dElay as given in the table. This can be improved further.

Future Scope of Work

The proposed Wallace multiplier now can be improved with the help of revised booth algorithm at the stage of generating partial product. For faster multiplication we have use Brent Kung Adder to reduce area and to increase speed we can use Kogge Stone Adder.

VI. REFERENCES

[1] "Design of an Energy Efficient 4-2 Compressor"- By M.Kumar[1],J.Nath[2],"published in IOP Conference Series: Materials Science and Engineering 2017.

[2] " Wallace Tree Multiplier Designs: A Performance Comparison Review", By H.Bansal, K. G. Sharma, T.Sharma,, published in International Institute for Science, Technology and Education,Vol.5, No.5, 2014.

[3] " Implementation of Wallace Tree Multiplier Using Compressors, By N.K.Gahlanetal, published in International Journal of Computer Technology & Applications,Vol 3 (3),MAY-JUNE 2012.

[4] " Analysis Of High Speed Wallace Tree Multiplier Using Compressors For DSP Applications" By Jayalakshmi N[1], H.V.Kumar[2], K.Rambabu[3] , published in Journal of Engineering Research and Application Vol. 8, Issue 7 (Part -III) July 2018.

[5] "Design of Wallace Tree Multiplier using Compressors" By K.Gopi Krishna[1], B.Santhosh[2], V.Sridhar[3], published in Internationl Journal of Engineering Research and Technology (IJESRT),September,2013.