IMPLEMENTATION OF HIGH SPEED AND LOW AREA RECONFIGURABLE FIR FILTER USING MULTIPLE CONSTSANT MULTIPLIER

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ABSTRACT

The direct Form FIR filter is used for DSP applications where the filter order is fixed. Generally this filter consumes more area and power. To overcome this problem reconfigurable architecture of transpose form FIR filter which is similar to direct form FIR filter where only delay and multiplier unit switched positions is incorporated. The RFIR structure consist of Coefficient selection unit (CSU), register unit(RU),Inner product unit (IPU) and pipeline adder unit(PAU). The PAU is used to add output from the IPU unit .The CSU is used to store coefficient of all the filter to be used for the reconfigurable application. Here RFIR is designed using a IPU which consumes more area and delay. The modified RFIR is designed further to reduce the area and delay. The modified RFIR filter the IPU is replaced by the multiple constant multiplier (MCM). The MCM consumes less area, delay than compared methods.

Keyword: *Finite impulse response filter(FIR),Reconfigurable architecture, Multiple constant multiplier,etc.*

1.INTRODUCTION

Finite impulse response filter is the filter where the impulse response is of finite duration and it settles zero at finite time. This is in contrast to the infinitely impulse response which have feedback and response at infinite duration. For a FIR filter order N the output sequence is given as the sum of the recent inputs.

$$Y[n]=b_0x[n]+b_1x[n-1]+b_2x[n-2]\cdots\cdots b_Nx[N-1]$$
$$=\sum_{i=0}^{N} x[N-i] \quad (1)$$

- where x[n] is the input signal,
- y[n] is the output signal,
- N is the filter order; an Nth-order filter has (N+1)terms on the right-hand side
- b_i is the value of the impulse response at the i'th instant for 0<=i<=N of an Nth-order FIR filter.

The output of the FIR filter is given in form Z transform of the FIR frequency response.The basic structure of the FIR filter of order N is given as follows

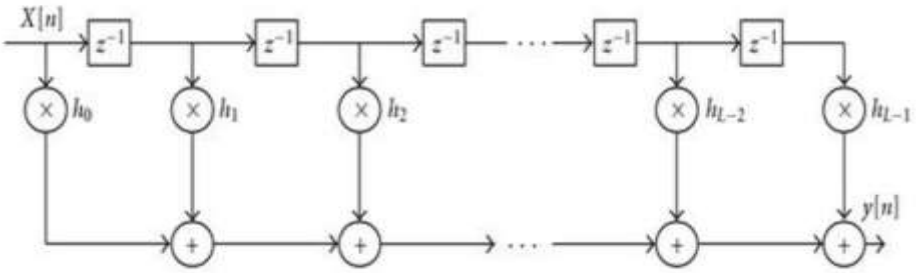

FIG 1 FIR Filter

Where z^{-1} is the delay element and x[n] is the input impulse and y[n] is the output of the FIR filter where the output is given in recurrence relation represented in the above equation. The above figure is given as the direct form FIR filter. The FIR is commonly used in the DSP application like equalization, software defined radio, and other digital communication applications.

1.1.OBJECTIVE

Generally the software defined radio require many large order filter , this large order filter occupies more area and delay is large. Here the design becomes complex.to reduced this complexity the various techniques was introduced. The proposed structure of the FIR filter is designed as Reconfigurable FIR filter and the coefficients are fixed in order to reduce the multiplication complexity.

2.RECONFIGURABLE FIR FILTER

Reconfigurable FIR filter is designed such that the it consist of a coefficient storage unit(csu),register unit (RU).Inner product unit(IPU) and a pipeline adder unit.The reconfigurable FIR filter is given as follows

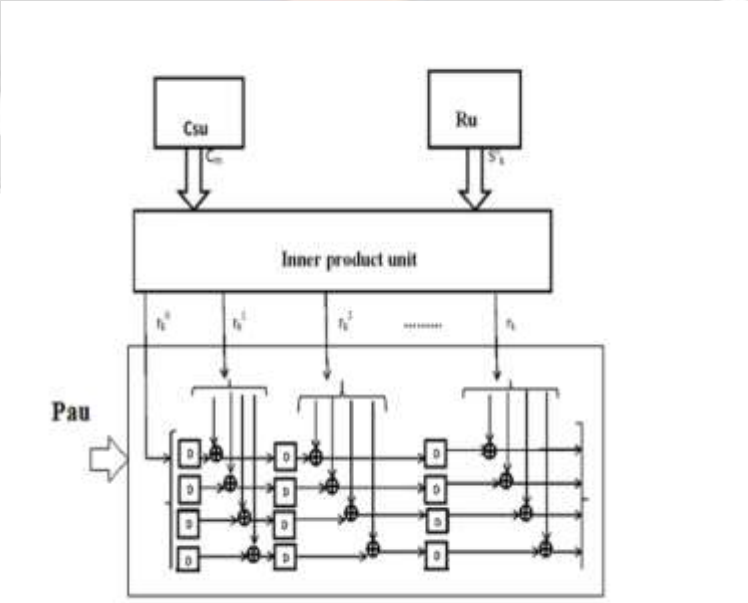

Fig 2 Reconfigurable FIR filter architecture

The figure 2 shows the architecture of the RFIR which shows all the blocks. Here the CSU stores the coefficients of all the filter to be used. It is implemented using the LUT's, such that the filter coefficient is obtained in one clock cycle. The coefficient is given as c_m which is given by a equation

$$C_m=\{h(mL),h(mL+1),h(mL+2)\cdots\cdots\cdots,h(mL+L-1)\} \quad 2$$

Where L is the block size.

The register unit (RU) gets a input x at the k_{th} cycle and produces a output with respect to the block size L. The output of the register unit is given to the M IPU unit. Where M is given as N\L. The inner product unit gets input from the coefficient storage unit and the register unit. In IPU unit the matrix multiplication of the output from the CSU unit and RU is performed. Then the partial product produced at the inner product unit is given to the pipeline adder unit (PAU). All the IPU acts parallel and give the output to the PAU unit. The output of the PAU unit is given in recurrence relation.

$$Y_k = \sum_{m=0}^{M-1} r^m_k \quad 3$$

$$r^m_k = S^0_{k-m}.c_m$$

thus the Y_k is given in the form as follows

$$Y(z)=S^0(z)[z^{-1}((z^{-1}(z^{-1} c_{M-1} + c_{M-2}) + c_{M-3}) + \dots) + c_1) + c_0] \quad 4$$

the equation 3 represnts the output of the PAU unit.

Where,

- Y_k is the output of the signal
- S^0 is the signal from the register unit
- C_m is the coefficient vector

The 4 represents the output signal of y_k given in the z-domain.

But in this implementation of the RFIR with inner product unit large area is required which is comparatively less compared to the N no of direct form FIR filter. Thus inorder to reduce the area and to increase the performance a method called multiple conatant multiplier is used.

3.MULTIPLE CONSTANT MULTIPLIER

Multiple constant multiplication (MCM) is defined as a technique used to reduce the number of addition/subtraction operations required for the multiplication of multiple constants by an input variable . Multiplier Constant Multiplications is a way constant multiplications using a shift-adds architecture. It is first to define the constants under a particular number representation, and second, for the nonzero digits in the representation of the constant, is to shift the input variable according to the digit positions and add/subtract the shifted variable with respect to the digit value.

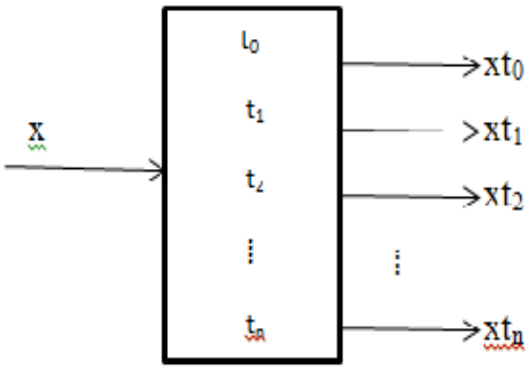

Fig 3 multiple constant multiplier

Fig 3 represents the basic MCM block where a input x is multiplied with a constant coefficient $t_0,t_1,\ldots\ldots t_n$ and the output is obtained parallelly .MCM uses shifter for multiplication in order to reduce the number of multipliers and adder used for calculating the partial products. This multiple constant multiplier can implemented only in the transpose form FIR filter. The transpose form FIR filter is similar to that of the direct form FIR filter only difference is that the delay and multiply unit is interchanged. So that the MCM can implemented easily on the FIR filter.

3.1 RECONFIGURABLE FIR FILTER USING MCM

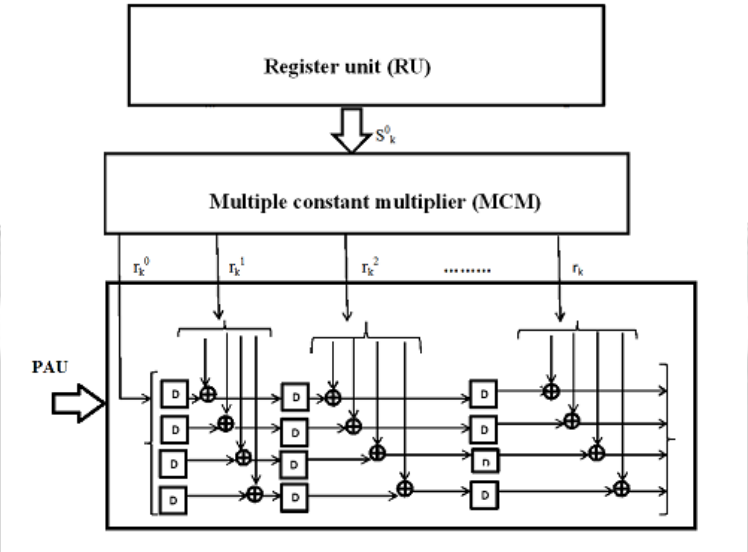

Fig 4 MCM based FIR filter

The figure 4 represents the MCM based architecture of the reconfigurable FIR filter. The derivation of MCM units for transpose form block FIR filter is shown in the figure. For fixed-coefficient implementation, the CSU is no longer required, since the structure is to be tailored for only one given filter. Similarly, IPUs are not required. The multiplications are given to the MCM units for a low-complexity realization. The proposed method for MCM-based implementation of block FIR filter makes use a symmentry input matrix S^0_k to perform horizontal and vertical common subexpression elimination and to minimize the number of shift-add operations in the MCM blocks. MCM block produces the necessary product terms.The subexpression of the MCM blocks are shift adding the adder network to produce the inner-product values (rl,m), for $0 \leq l \leq L-1$ and $0 \leq m \leq (N/L)-1$ corresponding to the matrix product . The inner-product values are finally added in the PAU.In pipeline adder unit the

4 RESULTS AND COMPARISON

4.1 Results of IPU based FIR filter

4.1.1 Simulation output

Fig 5 Modelsim output for reconfigurable FIR filter

By following the procedure to run the Modelsim the simulation results are obtained. Figure 5 represents simulation results of reconfigurable FIR filter

4.1.2 Area

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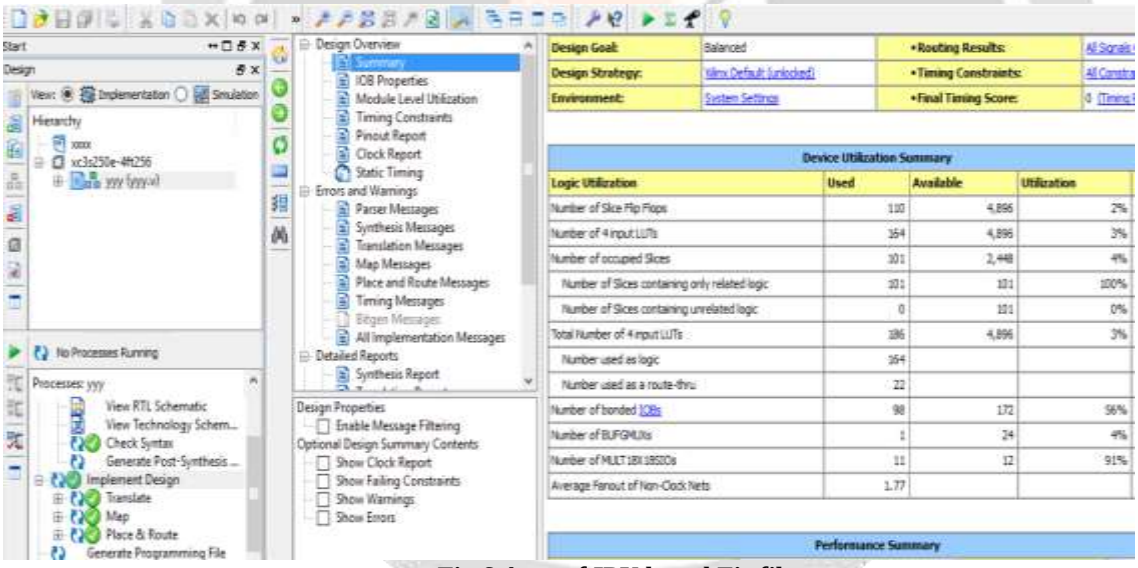


Fig 6 Area of IPU based Fir filter

As shown in the figure 6 the number of occupied in the reconfigurable IPU based FIR filter is 110 out of 2489 . The number of LUT's is 164

4.1.3 Delay

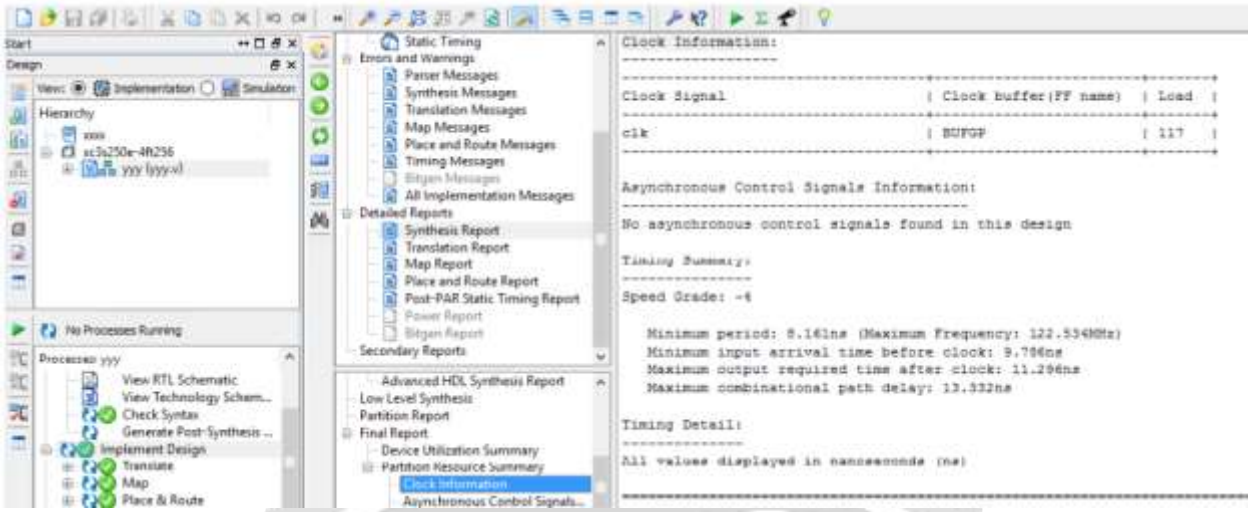


Fig 7 Delay of IPU based FIR filter

As shown in the figure 7 the delay produced by using innerproduct unit is 21.07ns.

4.2 Results of MCM based FIR filter

4.2.1 Simulation output

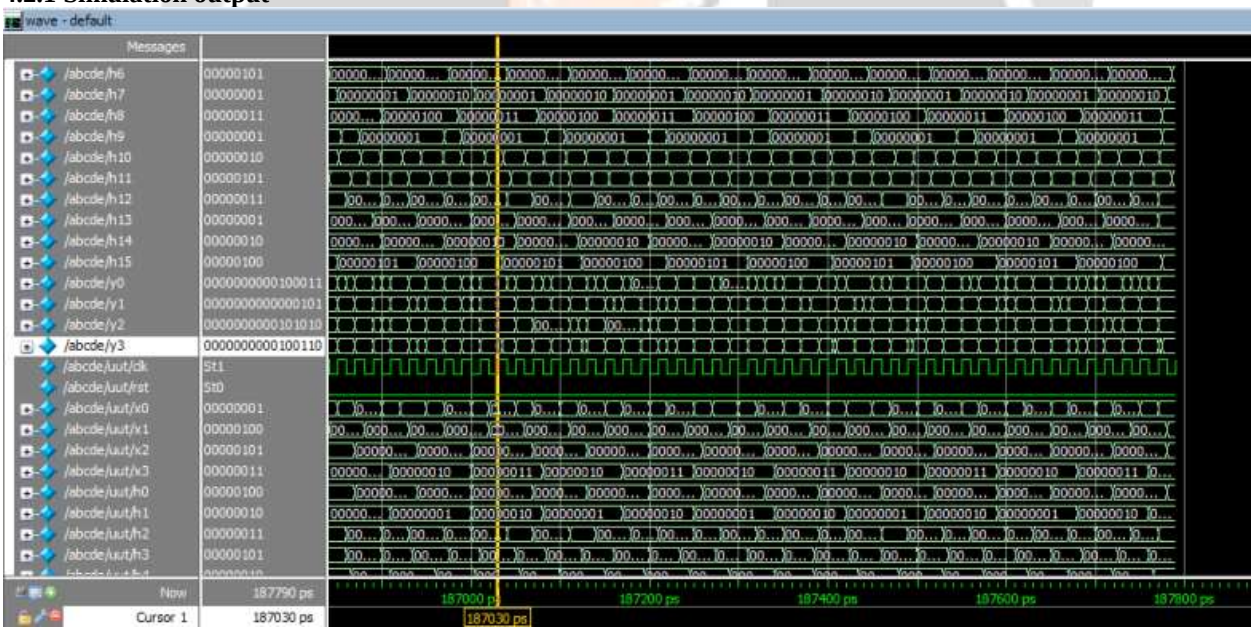
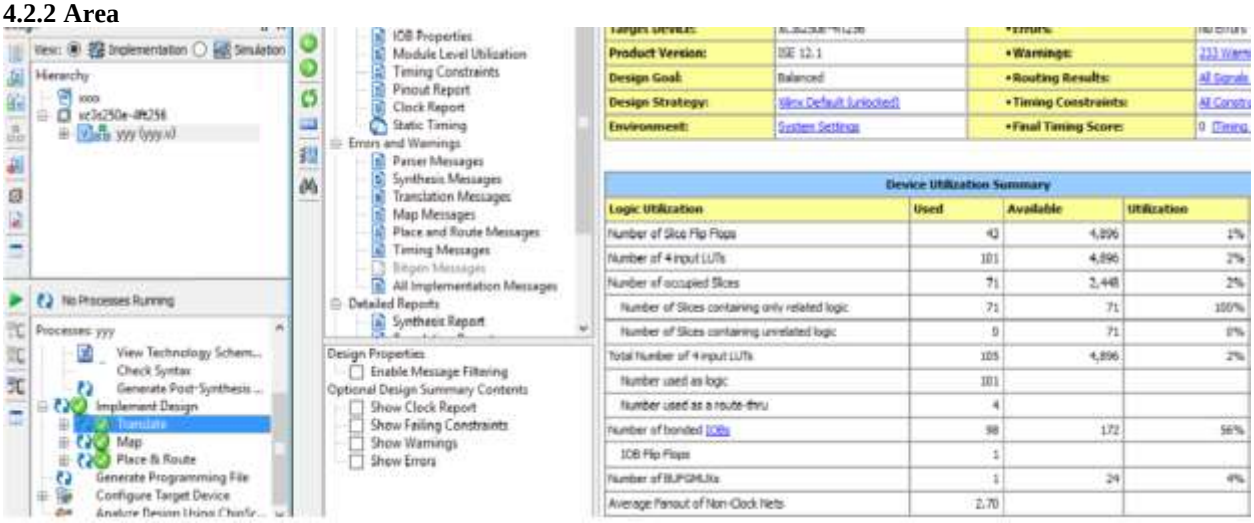


Fig 8 Modelsim output of MCM based FIR filter

By following the procedure to run the Modelsim the simulation results are obtained. Figure 8 represents simulation results of reconfigurable FIR filter

4.2.2 Area



Product Version:	ISE 12.1	**•Warnings:**	233 Warn
Design Goal:	Balanced	**•Routing Results:**	All Signals
Design Strategy:	Xilinx Default (unlocked)	**•Timing Constraints:**	All Constr
Environment:	System Settings	**•Final Timing Score:**	0 (Timing

Device Utilization Summary

Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	42	4,896	1%
Number of 4 input LUTs	101	4,896	2%
Number of occupied Slices	71	2,448	2%
Number of Slices containing only related logic	71	71	100%
Number of Slices containing unrelated logic	0	71	0%
Total Number of 4 input LUTs	105	4,896	2%
Number used as logic	101		
Number used as a route-thru	4		
Number of bonded IOBs	98	172	56%
IOB Flip Flops	1		
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	2.70		

Fig 9 Area of MCM based FIR filter

As shown in the figure 9 the number of occupied slices in MCM based FIR filter is 71 out of 2488 . The number of LUT's is 101 out of 4896

4.2.3 Delay

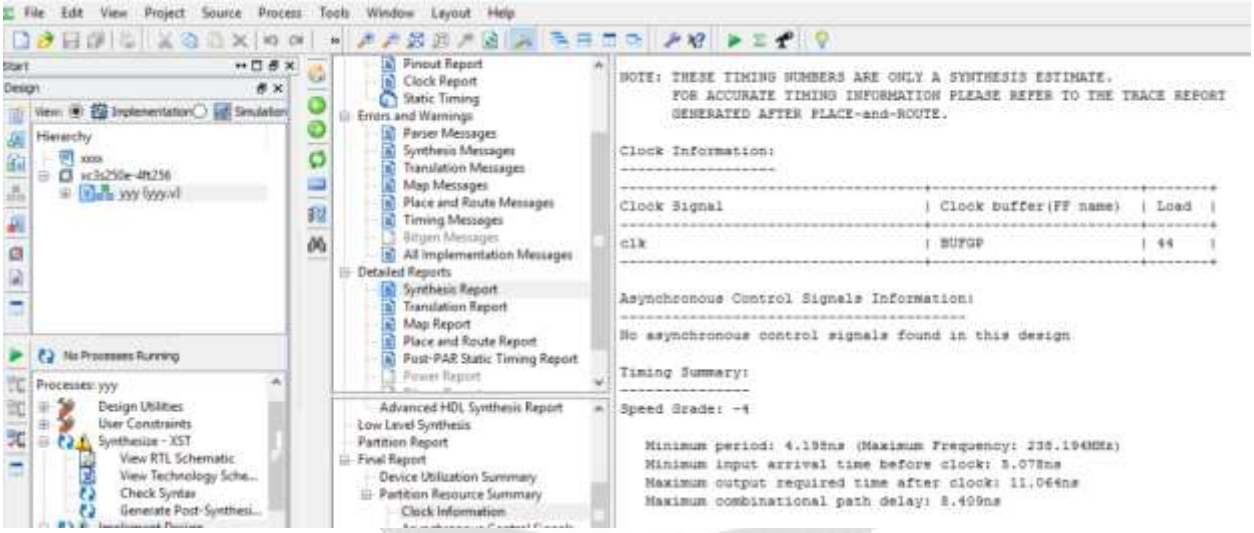


Fig 10 Delay of MCM based FIR filter

As shown in the figure 10 the delay produced by using MCM unit is 16.14ns.

4.3 Comparison of results

4.3.1Using table

The result of various multiplier used are described in the following table

TABLE 4.1 Results of various reconfigurable implementation

Reconfigurable FIR filter	Area		Delay
	LUT's	Slices	
IPU based	164	110	21.07 ns
MCM based	101	43	16.14 ns

From the above table it is clear that the Area ,Delay and power are reduced respectively for each multiplier . Reconfigurable FIR filter with IPU consumed more Area and Delay . The multiple constant multiplier have reduced area and power.

4.3.2 Using graph

- X-Axis denotes various multipliers.
- Y-Axis denotes the values.

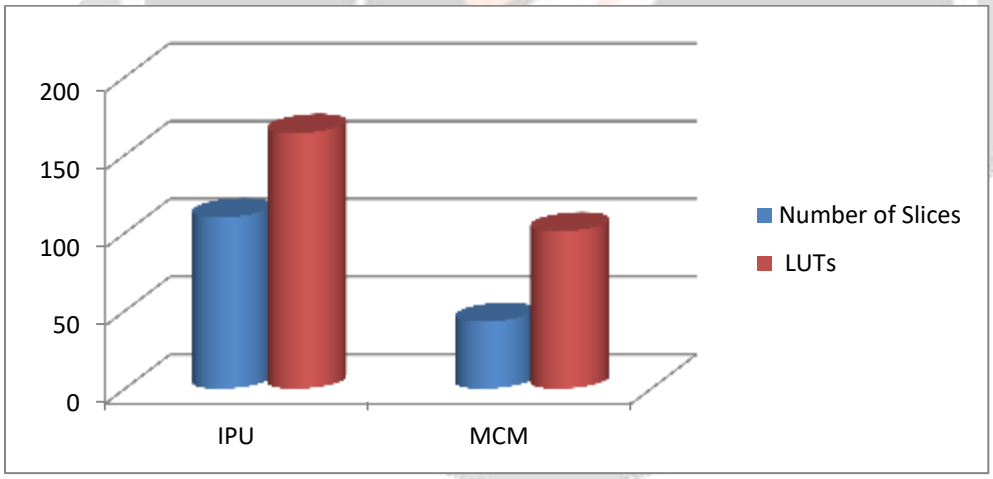


Fig 11 Area comparison

Figure 11 represents the area of various implementation of FIR using a inner product unit and MCM. The number of slices used and LUT's in IPU based FIR filter used is 164 and 110 respectively .The number of slices used and LUT's in MCM based FIR filter used is 101 and 43 respectively.

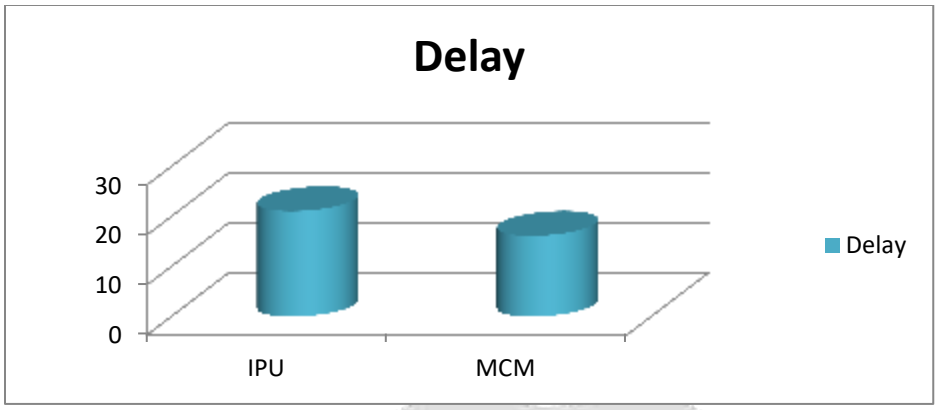


Fig 14 comparison graph on Delay

Figure 12 represents the delay of various implementation of FIR using a inner product unit and MCM. The delay IPU based and MCM based FIR filter is 21.07ns and 16.14ns respectively.

5 CONCLUSION

An area efficient and high speed multiple constant multiplier is proposed. Multiple constant multiplier consumes slices ,of delay when compared to the inner product unit. This multiple constant multiplier is incorporated in the RFIR. This proposed reconfigurable FIR filter with multiple constant multiplier is compared with the reconfigurable FIR filter with inner product unit. The results show that the proposed reconfigurable FIR filter with multiple constant multiplier offers better performance than the conventional reconfigurable FIR filter with a inner product unit. Thus this proposed FIR filter con be used in the digital communication applications like the software defined radio.

6 REFERENCE

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