IMPLEMENTATION OF HIGH SPEED MULTIPLIER USING VEDIC MATHEMATICS

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ABSTRACT

Multipliers play a major role in processors and in many computational systems. The speed of these systems greatly depends on the speed of its multipliers. In order to enhance the speed of the systems the faster and efficient multipliers should be employed. Vedic Multiplier is one of the best solution which is capable of performing the quicker multiplications by eliminating the unwanted steps in the multiplication process. Power dissipation is another important constraint in an embedded system which cannot be neglected. The Reversible Logic has received great attention in the past recent years due to its ability in reducing the power dissipation, which is the major concern in Digital Designing. Here we present a high speed Vedic Multiplier which is efficient in terms of speed, making use of Urdhva Tiryagbhyam, a sutra for multiplication from Vedic math's. It is a simple architecture coupled with increased speed forms an unparalleled combination for serving any complex multiplication computation.

1. INTRODUCTION

Multiplier is an essential functional block of a microprocessor because multiplication is needed to be performed repeatedly in almost all scientific calculations. The fast and low power multipliers are required in small size wireless sensor networks and many other DSP (Digital Signal Processing) applications. They are also used in many algorithms such as FFT(Fast Fourier transform), DFT(Discrete Fourier Transform) . There are two basic multiplication methods namely Booth multiplication algorithm and Array multiplication algorithm used for the design of multipliers. The schemes for e client addition of partial products are Wallace tree ,Dadda tree . The speed of multiplication (as well as power dissipation) is dominantly controlled by the propagation delay of the full / half adders used for the addition of partial products. Multipliers have large area, long latency and consume considerable power. Vedic multiplier architecture achieves high speed, low area and less power consumption. We are implementing this multiplier using vedic mathematics. As the existing methods have their own limitations there are different approaches which use Vedic mathematics. The ancient system of Vedic Mathematics was rediscovered from the Indian Sanskrit texts known as the Vedas, between 1911 and 1918 by Sri Bharati Krisna Tirthaji (1884-1960) from the Atharva Vedas. According to his research all of mathematics is based on sixteen Sutras, or word-formulas.

These formulae describe the way the mind naturally works and are therefore a great help in directing the student to the appropriate method of solution. In the Vedic system di cult problems or huge sums can often be solved immediately by the Vedic method. These striking and beautiful methods are just a part of a complete system of mathematics which is far more systematic than the modern system. Vedic Mathematics manifests the coherent and uni ed structure of mathematics and the methods are complementary, direct and easy. Its a unique technique of calculations based on simple principles and rules , with which any mathematical problem - be it arithmetic, algebra,

geometry trigonometry, or even calculus can be solved mentally[2]. The sixteen sutras of Vedic mathematics are listed below.

Ekadhikina Purvena : By one more than the previous one

Nikhilam Navatashcaramam Dashatah : All from 9 and the last from 10

Urdhva-Tiryagbyham: Vertically and crosswise

Paraavartya Yojayet: Transpose and adjust

Shunyam Saamyasamuccaye: When the sum is the same that sum is zero.

(Anurupye) Shunyamanyat: If one is in ratio, the other is zero.

Sankalana-vyavakalanabhyam : By addition and by subtraction

Puranapuranabyham : By the completion or non-completion

Chalana-Kalanabyham: Differences and Similarities

Yaavadunam : Whatever the extent of its deficiency

Vyashtisamanstih: Part and Whole

Shesanyankena Charamena : The remainders by the last digit

Sopaantyadvayamantyam: The ultimate and twice the penultimate

Ekanyunena Purvena: By one less than the previous one

Gunitasamuchyah: The POS is equal to SOP

Gunakasamuchyah: The factors of the sum are equal to the sum of the factors.

He claimed thatthe very word Veda" has this derivational meaning; i.e. the fountain-head and illimitable store house of all knowledge. This derivation, in effect, means, connotes and implies that the Vedas should contain within themselves all the knowledge needed by mankind relating not only to the so-called spiritual matters but also to those usually de-scribed as purely \secular", \temporal", or \worldly"; and also to the means required by humanity as such for the achievement of all round, complete and perfect success in all con-ceivable directions and that there can be no adjectival or restrictive epithet calculated to limit that knowledge down in any sphere, any direction or any respect whatsoever.

The real beauty and e effectiveness of the Tirthaji system cannot be fully appreciated without practicing the system. One can then see why its enthusiasts claim that it is the most re ned and e client calculating system known. Di cult arithmetic problems and huge sums can often be solved immediately by Tirthaji's methods. These striking and beautiful methods are a part of a system of arithmetic which Tirthaji claims to be far more methodical than the modern system. "Vedic" Mathematics is said to manifest the coherent and unified structure of arithmetic, and its methods are complementary, direct and easy.

The simplicity of the Tirthaji system means that calculations can be carried out men-tally, though the methods can also be written down. There are many advantages in using a flexible, mental system. Pupils can invent their own methods; they are not limited to one method. This leads to more creative, interested and intelligent pupils. Interest in the Tirthaji's system is growing in education, where mathematics teachers are looking for something better and nding the Vedic system is the answer. Research is being carried out in many areas including the effects learning the Tirthaji system has on children; developing new, powerful but easy applications of these Sutras in arithmetic and algebra.

”Vedic Mathematics" refers to a technique of calculation based on a set of 16 Sutras, or aphorisms, as algorithms and their upa-sutras or corollaries derived from these Sutras. Its enthusiasts advance the claim that any mathematical problem can be solved mentally with these sutras.

2.LITRATURE SURVEY

In may 2016 Rakesh M et.al, proposed an efficient 64 bit multiplication is implemented making use of VEDIC multiplier to extend the ease of computation as compared with con-ventional method. The less number of gates and high speed specification are achieved in this design. The 32 bit multiplicand and multiplier divided into MSB and LSB bits each of length 16 bit and this is implemented in given 16X16 block multiplier. Xilinx Synthesis 16.1 tool is used for synthesis purpose. The four 32 bit Vedic multipliers and two modified carry save adder are required to realize 64 bit multiplier. The proposed architecture is very fast and accurate.[1].

In april 2016 K.N.Vijeyakumar et.al, developed and designed high speed along with area efficient Arithmetic unit suitable for high performance speed. This provides the suitability for the proposed AU to gain high speed portable VLSI implementation. Note that the structuring of our proposed AU with equal logic depth maintains parallelism and uniform delay across all the outputs. In addition the design of the blocks and multiplexers are such that the design can be recon gured for higher bitwidths of input operand with ease.[2]

In april 2016 Shraddha Wanjari et.al, propounded work on designing and implementation of adder using DKG gate reversible logic. There is no power dissipation if a circuit contains only reversible gates. The register designed in the accumulator is used to add the multiplied numbers. MAC unit is formed by the multiplier, adder , accumulator. To obtain the nal multiplication output we add the partial product to these results. Vedic Multiplier has put forward to intensity the action of the MAC Unit. The results are analyzed by com-paring proposed MAC with conventional one. The results obtained using there design had better performance when compared to the pervious MAC designs. [3]

In april 2016 Shiksha Pandey et.al, presented the design and implementation of high speed 16x16 bit Vedic multiplier architecture which is somewhat different from the Con-ventional method of multiplication like addition and shifting. The implementation and simulation of Verilog HDL code for Urdhva tiryakbhyam Sutra for 16x16 bits multiplication and carry select adder is carried on XilinxISE9.2i. There is reduction in area in FPGA and also improve the performance in terms of speed. It will be veri ed by comparing it will hardwired unsigned multiplier.[4]In February 2016, Arunkumar P. Chavan et.al, has worked on two multiplier using kogge stone adder and ripple carry adder respectively. The modelling used for multiplier was verilog HDL and synthesized Using Cadence Digital Complier (DC) . Here 45nm technology was used . The synthesized netlists were loaded into Cadence SOC Encounter to carry out RTL to GDSII code. Processing time was decreased therefore the advantage of high speed was acquired.[5]

In 2016 Pankaj Prajapati et.al, Used nikhilam sutra and barrel shifter for implementation of multiplier. The o ered multiplier has fast response, least area and consumed power. The barrel shifter reduced the delay when compared to conventional multipliers. The designer is being developed on Xilinx 14.1i updated version. Xilinx 9.2i has features like low mem-ory requirement, fast debugging, and low cost. The design provides 27% low memory. ISE 14.1i software features gives sudden advancements in place and route and clock algorithm providing up to a 15% performance advantage.[6]

Rakshith Saligram et al[7](2013) : The focus of this paper is mainly to design a low power high speed multiplier which is done by constructing the multiplier using reversible logic gates. The quantum cost is a parameter that directly re ects the delay of the quantum circuit. Besides imbibing the design criterion that fan-out must be generated within the circuit, the perposed design is also reduce the TRLIC as compared to the previously proposed design.

Gowthami. P et al [8] (2016): This paper presents the new design of 2x2 Urdhva Tiryakbhayam multiplier using reversible logic gates. This author presented design is an optimized structure in terms of reversible gates, garbage outputs, quantum cost and TRLIC. Lower the value of design constraints more efficient is the design. The reversible gates used in the design are two BME, one Peres, one BVF and one CNOT gate. Reversible logic is functionally veri ed through simulation process using Xilinx ISE 14.1. The simulation is per-formed by creating a test bench for the design. The Verilog hardware description language is used to code the proposed design.

Rakshith TR.et al [9] (2013): In the present research, This multiplier may and applications in Fast Fourier Transforms (FFTs), and other applications of DSP like imaging, software defined radios, wireless communications. This design stems from the conventional logic implementation. After this, the 2x2 UT multiplier block is cascaded to obtain 4x4 multiplier. The ripple carry adders which were required for adding the partial products were constructed using HNG gates.

A. Shifana Parween1, et al [11] (2014):In this paper a 4 X 4 Vedic multiplier is designed using reversible logic gates which is e cient in terms of constant inputs, garbage outputs, quantum cost, area, speed and power. The design is simulated using Verilog. The design of the reversible 2x2 and 4x4 multipliers is logically verified using XILINX 9.2i. First 2X2 UT multiplier is designed using Peres gate and Feynmen gate. The ripple carries adders which were required for adding the partial products were constructed using HNG gates.

G Sree Lakshmi et al[12](2016): This paper reviews Reversible logic gates became very important and computing paradigm having its applications in low power CMOS technologies and Quantum computing Reversible logics are used to reduce the depth of the circuits . The design is simulated, synthesized and power estimation was done using TSMC 180nm technology using Cadence Digital tools. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there exist one-to-one correspondence between its input and outputs.

3.PROPOSED SYSTEM

The increasing demand in developing an ability of processors to handle the complex and challenging processes has resulted in the integration of processor cores into one chip. even then the load, on the processor is not less. This load is reduced by supplementing the main processors with co-processors, designed to work upon specific type of functions. A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most of the system. Vedic mathematics is the ancient system of mathematics which has unique technique of calculations based on 16 sutras. Employing these techniques in the computations algorithm of processor will reduce the complexity and execution time.

4.BLOCK DIAGRAM

In the design of the proposed Vedic multiplier and-GATE and half adders are fundamental block (Basic block) is shown in figure. Also symbol of this fundamental block is shown to be used in2x2 bit Multiplier.

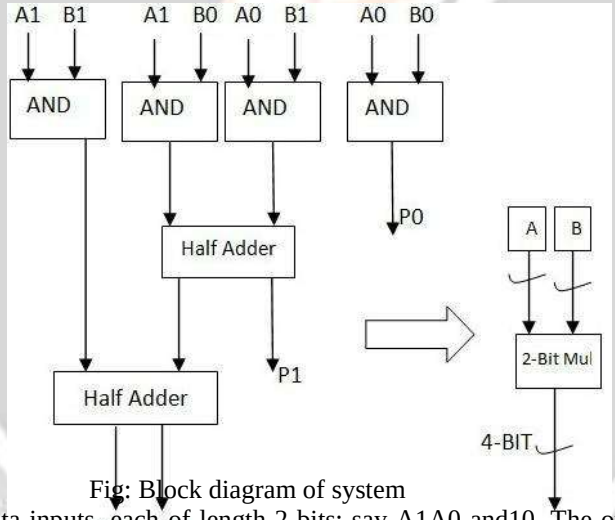


Fig: Block diagram of system

Let us consider two data inputs, each of length 2 bits; say A1A0 and10. The output can be of four bit length, say3210. As per basic method of multiplication, we can obtain the result by getting partial product and then by adding it.

In Vedic multiplier, 0 is obtained by vertical multiplication of data bits 0 and 0, 1 is obtained by addition of crosswise bit product i.e. 1 0 and 1 0 and next 2 is obtained by adding the product vertical data bits 1 and 1 with the carry generated from the previous

$$\begin{array}{r} A_1A_0 \\ \times\ B_1B_0 \\ \hline A_1B_0\ \ A_0B_0 \\ A_1B_1\ \ A_0B_1 \\ \hline P_3\ \ P_2\ \ P_1\ \ P_0 \end{array}$$

4. RESULTS AND OUTPUTS :

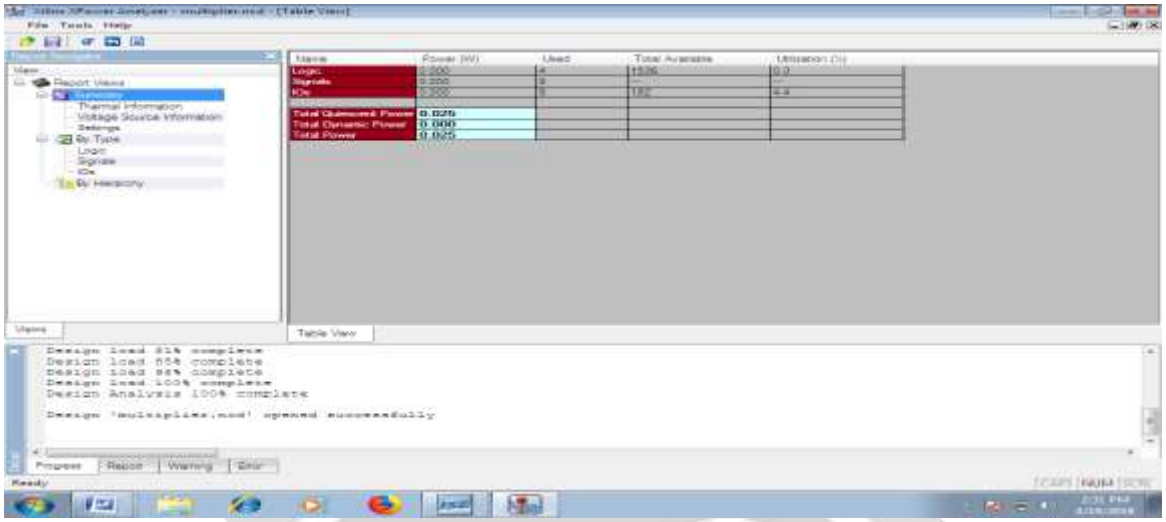
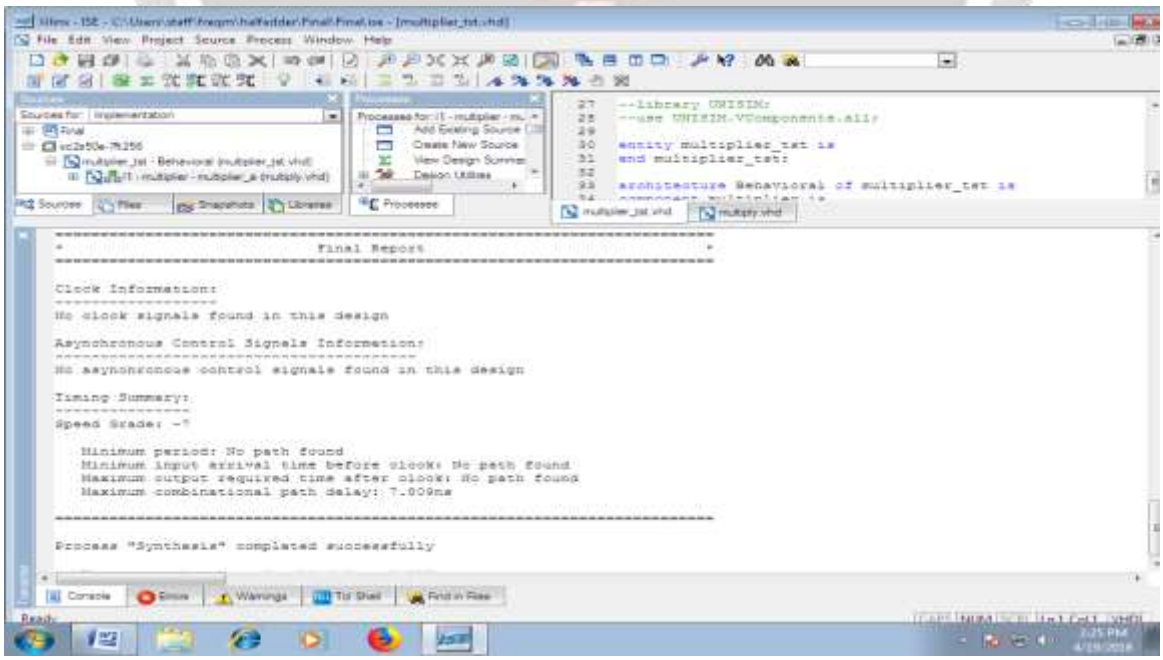


fig: power of multiplier

fig: delay of multiplier

4. CONCLUSIONS

The purpose of this implementation is to study existing methods used for multiplication using Vedic math's techniques to gain better performance in terms of high speed, low power consumption and small area, also to identify the outcomes and shortcomings of the earlier work. It has been observed that in recent years many researchers have use Urdhva Tiryagbhyam sutra for the multiplication purpose. The survey identifies challenges that have not yet been resolved. In turn, this will help researchers in this area focus their research effort on those issues identified as bottlenecks and to eventually develop better multiplication techniques. This work shows the implementation of Urdhva Tiryakbhayam Vedic Multiplier. We have implemented the 2 bit, Vedic multipliers by using Verilog and then the codes are compiled and simulated in micro wind and xilinx software. Efforts are made in this design to reduce the propagation delay.



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