IMPROVING TEST COVERAGE OF SCL USING TEST POINT INSERTION

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ABSTRACT

IC testing is one of the most important steps in today's complex system-on-chip design. After manufacturing, if an IC failed in performing when applied in real condition it will increase the cost for manufacturing and also increases the time of design. So this testing should be done before the manufacturing. Sleep Convention Logic is a promising Asynchronous Logic Style. And its design is a combination of Multi Threshold CMOS design and Null Convention Logic. Its architecture is different from the NCL therefore a new design for testability should be proposed. Scan cell based DFT is proposed here and to improve its test coverage an additional Test Point Insertion technique is included.

Keyword:- *Design for testability (DFT), Sleep convention logic (SCL), Null convention logic (NCL), Multi threshold complementary metal oxide semiconductor (MTCMOS), Test point insertion (TPI), Scan cells.*

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1. INTRODUCTION

Design for testing or design for testability (DFT) consists of IC design techniques that add testability features to a hardware product design. The added features make it easier to develop and apply manufacturing tests to the designed hardware. The purpose of manufacturing tests is to validate that the product hardware contains no manufacturing defects that could adversely affect the product's correct functioning. Tests are applied at several steps in the hardware manufacturing flow and, for certain products, may also be used for hardware maintenance in the customer's environment. The tests are generally driven by test programs that execute using automatic test equipment (ATE) or, in the case of system maintenance, inside the assembled system itself. The response of vectors (patterns) from a good circuit is compared with the response of vectors (using the same patterns) from aDUT (device under test). If the response is the same or matches, the circuit is good. Otherwise, the circuit is not manufactured as it was intended.

The most common method for delivering test data from chip inputs to internal circuits under test (CUTs, for short), and observing their outputs, is called scan-design. In scan-design, registers (flip-flops or latches) in the design are connected in one or more scan chains, which are used to gain access to internal nodes of the chip. Test patterns are shifted in via the scan chain(s), functional clock signals are pulsed to test the circuit during the "capture cycle(s)", and the results are then shifted out to chip output pins and compared against the expected "good machine" results.

An asynchronous circuit, or self-timed circuit, is a sequential digital logic circuit which is not governed by a clock circuit or global clock signal. Instead it often uses signals that indicate completion of instructions and operations, specified by simple data transfer protocols. This type of circuit is contrasted with synchronous circuits, in which changes to the signal values in the circuit are triggered by repetitive pulses called a clock signal. Most digital devices today use synchronous circuits. However asynchronous circuits have the potential to be faster, and may also have advantages in lower power consumption, lower electromagnetic interference, and better modularity in large systems. Asynchronous circuits are an active area of research in digital logic design.

Sleep Convention Logic (SCL) which is also called as Multi Threshold Null Convention Logic (MTNCL) has advantage of both Null Convention Logic and Multi Threshold Complementary Metal Oxide Semiconductor technology since it is a combination of both these technologies [1]. Register-less NULL convention logic (RL-NCL) design paradigm, achieves low power consumption by eliminating pipeline registers, simplifying the control circuit, and supporting fine-grain power gating to mitigate the leakage power of sleeping logic blocks. In Multi Threshold CMOS technology as its name indicates it uses transistors with multiple threshold voltages [3] like high threshold voltage for the transistors connected to either power supply or ground for reducing leakage current and low threshold gates for the transistors used for the logic implementation for speeder performance[2]. Null Convention Logic is an asynchronous logic design [3] composed of the ideas of dual rail encoding [10] and multi threshold logic gates [3]. NCL circuits utilize multi-rail signals, such as dual-rail logic, to achieve delay-insensitivity. A dual-rail signal, D, consists oftwo wires namely, D0 and D1. The DATA0 state (D0 = 1, D1 = 0) corresponds to a Boolean logic 0; the DATA1 state (D0 = 0, D1 = 1) corresponds to a Boolean logic 1; and

the NULL state (D0 = 0, D1 = 0) corresponds to the empty set meaning that the value of D is not yet available. The two rails are mutually exclusive, such that both rails can never be asserted simultaneously; and if two rails are asserted simultaneously then this state is defined as an illegal state [3], [7], [10]. NCL circuits are normally composed of 27 fundamental gates, called threshold gates, which comprise the set of all functions of four or fewer variables.The primary type of threshold gates is the THmn gate, where $1 \leq m \leq n$.THmn gates have n inputs and at least m of the n inputs must be asserted for the output to become asserted; and NCL threshold gates are designed with hysteresis state-holding capability, such that after the output is asserted, all inputs must be deasserted before the output will bedeasserted.Hysteresis ensures a complete transition of inputs back to NULL before asserting the output associated with the next wave front of input data [3].

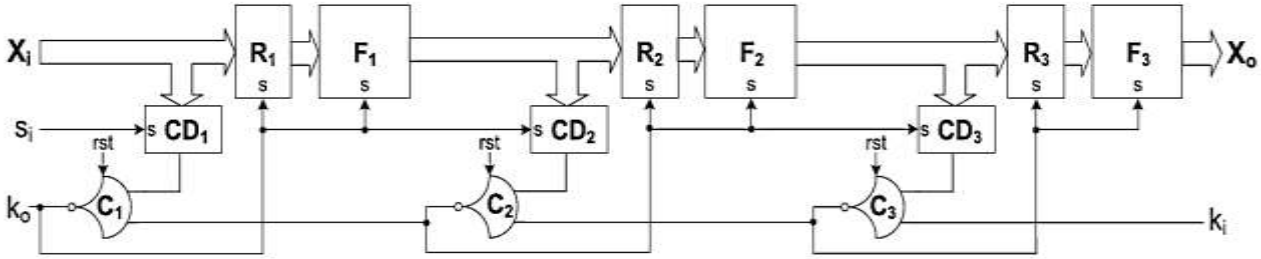


Fig-1: SCL architecture.

2. RELATED WORKS

2.1 SCL architecture

The SCL framework is shown in Fig. 1. As in Null Convention Logic, in each pipeline stage of SCL architecture a combinational logic function block (Fi), a register block (Ri), and a completion detector block (CDi) are contained. And this SCL requires an additionalgate to synchronize between DATA and NULL phases of the circuit. This additional gate is a simple resettable C-element with inverted output and it is known as the completion C-element (Ci). Combinational logic blocks in the SCL are made of threshold gates [14], [15] which implement the unatefunctions and there is no logic inversions are allowed.

An SCL gate is generally denoted as THmnWw1,…,wn where n is the number of inputs, m is the threshold of the gate, and w1, w2,... ,wn are the weights of inputs when the weights are > 1. If the inputs of the SCL gate are taken as x1,….,xn, the output of the SCL gate is logic 1 if $x1w1 + \cdots + xnwn \geq m$. For example, a TH23 gate has three inputs and its threshold is 2. In normal Boolean logic, the output of the TH23 gate can be expressed as Z = AB + AC + BC, here A, B, and C are its inputs. The transistor level design of this TH23 gate is shown in Fig.2.

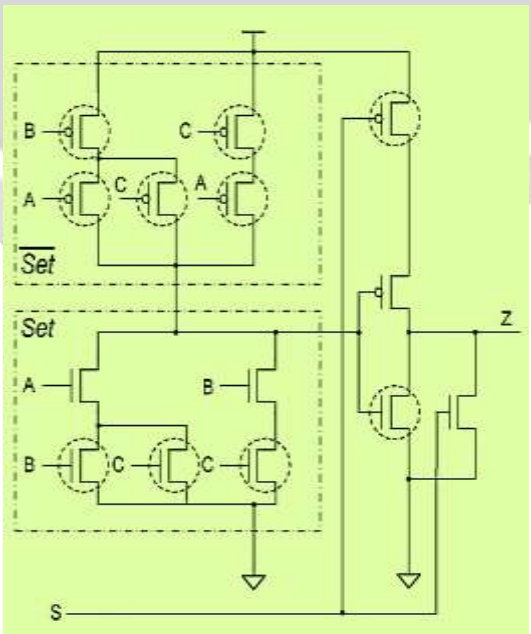


Fig- 2:SCL gate implementation of the TH23 gate.

Sleep Convention Logic comprised of fine grained power gating which a technique used for reducing the power consumption within a circuit. In this each separate units will have an additional sleeping mechanism that helps to avoid the

power usage when that particular unit is inactive. As in the NCL gates [17], [18], each SCL gate is made of a set block and a hold0 block (denoted as $\overline{set}$ in Fig. 2). Unlike NCL gates, the reset and hold1 blocks are removed from SCL gate. The functioning of removed reset block is now done by the sleeping mechanism. Asserting the sleep signal disconnects the output inverter from VDD and pulls the gate's output, Z, to GND, and this resets the gate. Since the inputs of each SCL gate are taken from the outputs of preceding SCL gates, the internal node would then precharge to VDD and complete the reset phase.The hold1 block's job was to add hysteresis to the NCL gates that helps to ensure input-completeness with respect to NULL. In the SCL circuits, since all the gates within the combinational blocks are forced to reset by asserting the sleep signal, the input-completeness with respect to NULL is already ensured and therefore NULL wavefront propagation is not needed. The circled transistors in Fig.2 are of high threshold voltagefor reducing leakage current when the gate is in inactive state and it reduces the static power consumption in the circuit.

2.2 Design for testability

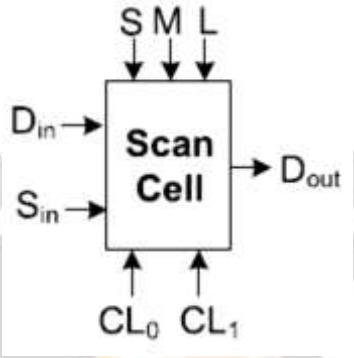


Fig-3: SCL scan cell.

Since asynchronous architecture is different from synchronous architecture it needs a testing procedure which is different from the normal synchronous testing methods. For that it uses scan cell based DFT methods.The components of a scan cell are shown in Fig.3.The testing procedure is as follows.

1) All stuck-at faults on the inputs and output of all completion C-elements can be detected by applying a single {DATA, NULL} pair to the SCL pipeline and allow it to propagate through the whole circuitry.
2) SCL combinational logic block becomes a normal Boolean circuit when disabling the sleep signal, then it can be checked for stuck-at faults using the traditional combinational ATPG tools.
3) The stuck-at faults on the sleep signal forks within a combinational logic block are either untestable (stuck-at-0 faults) or can be ignored through fault collapsing (stuck-at-1 faults).
4) The stuck-at faults on the sleep signal forks within a completion detector block are either untestable (stuck-at-0 faults) or can be detected during the test of the completion C-elements (stuck-at-1 faults).
5) The scan chain design is used to test the stuck-at faults on the sleep signal forks within a register block. For this scan chain is also needed to apply the ATPG generated test patterns to the combinational logic blocks.

The scan chain design of the SCL architecture is shown in Fig. 4. A scan cell is needed to connect to a single rail in the circuitry. Since in SCL architecture each data is represented using dual rail encoding for each data bit there will be two scan cells connected. The overall circuit can be divided into many different functional blocks as shown in Fig.4 and then after each of these functional block a scan chain is there, that consists of as many scan cells as the number of rails and c-element. Like that its goes on until the final functional block. Then as mentioned above in the points by applying a single {DATA, NULL} pair through the overall circuit the faults are detected.

3. PROPOSED SYSTEM

In the proposed system an additional test point insertion technology is included in order to increase the test coverage.

3.1 Control and observation points

Test point insertion involves adding control and observation points to the circuit-under-test in a way that the system function remains the same, but the testability is improved. An observation point is an additional primary output that is inserted in the circuit to increase theobservability of faults in the circuit. In the example in Fig. 5(a), an observation point is inserted at the output of gate G1 such that faults are observable regardless of the logic value at node y. Control points inserted in the circuit such that when it is activated, it fixes the logic value at a particular node to increase the controllability of some faults in the circuit. A control point can also affect the observability of some faults in the circuit because it can change the propagation paths in the circuit. In Fig. 5(b), a control point is inserted to fix the logic value at the output of gate G1 to a '1' when the control point is activated (this is called a control-1 point). This is accomplished by placing an OR gate at the output of gate G1. In fig. 8(c), a control point is inserted to fix the logic value at the output of gate G1 to a '0' when the control point is activated (this is called a control-0 point). This is accomplished by placing an AND gate at the output of gate G1. During system operation, the control points are not activated and thus don't affect the

system function. However, control points do add an extra level of logic to some paths in the circuit. If a control point is placed on acritical timing path, it can increase the delay through the circuit.

3.2 Test Point Insertion (TPI)

Test points can be inserted to put the uncontrollable or unobservable logics into the scan chain. By using this technique, these logics can be tested, and test coverage and test efficiency can be improved greatly. Test Point Insertion (TPI) is a useful technique for solving the potential testability problem and improving the test coverage of a design by making its uncontrollable logic controllable and unobservable logic observable. This technique also helps to improve the test efficiency since the higher coverage can be derived with few test vectors increasing. This technique is very easy to put into application since only a few commands are added in the existing scripts.

In addition, DFT engineers must guarantee the function remains unchanged during DFT design. In some designs, as some mission mode function logics are uncontrollable and unobservable, and these logics potentially cause many test problems. Test coverage for these designs could not be improved without using advanced test techniques or simply by increasing the number of test patterns. Test coverage is defined as the percentage of detected faults out of total detectable faults. This coverage is a more meaningful evaluation for test pattern quality. Fault coverage is defined as the percentage of detected faults out of all faults, including the ATPG Undetected faults. The primary input and output pads are used for controllability and observability in DFT design. In case of AND and NAND operations usually the controlling value(fan in) is taken as 0 and in case of OR and NOR operations it is 1.

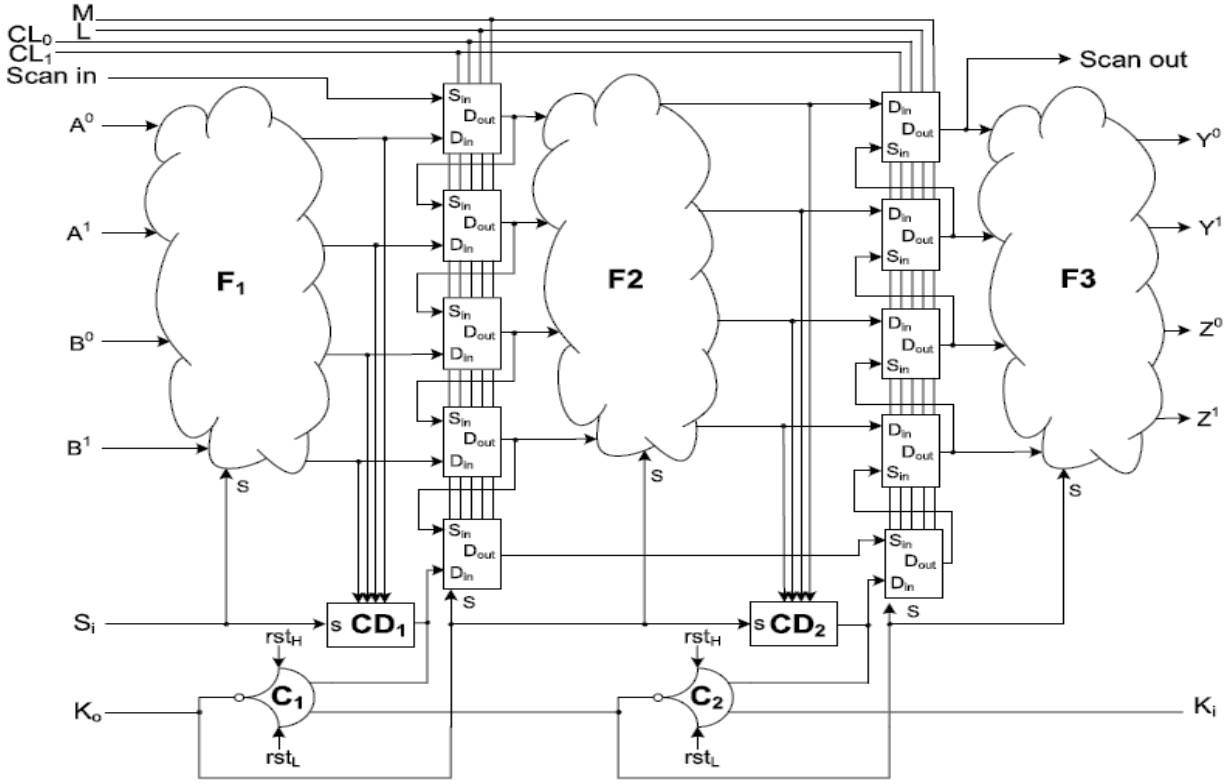
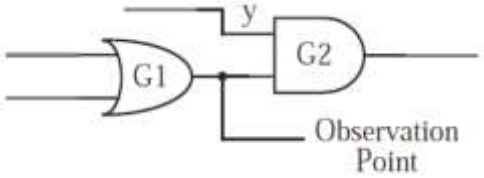
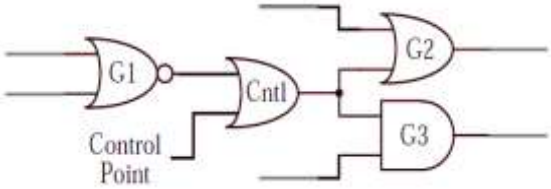


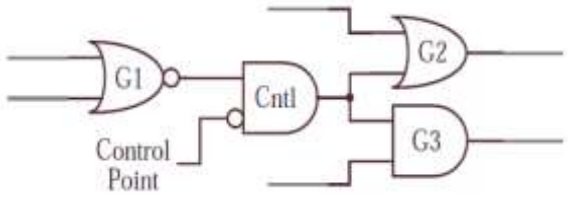
Fig-4: SCL scan chain design.



(a)



(b)



(c)

Fig-5: (a) Example of observation point. (b) Example of control-1 point. (c) Example of control-0 point.

4. IMPLEMENTATION

A 32- t0- 5 bit priority encoder is implemented with the SCL logic using 4 8- to- 3 bit priority encoders. Then the scan cells are used to make circuit testable. An additional test point insertion is applied for improving the test coverage of the design.

Fig. 7 shows the functional block diagram of the 8- to- 3 bit priority encoder. Between each logic block an array of scan cells are arranged for make it testable. Since in SCL logic each data is represented as dual rail, two scan cells are used for a single data bit. The scan in pin is used to provide the test pattern into the scan cells. During test mode, for each clock pulse it is shifted to each scan cells and finally all the scan cells are fed by this test pattern. And during normal mode the circuit generates the output corresponding to the input data provided. Two circuits of 32- to- 5 bit priority encoders are designed, one with faults and another without faults and is designed as shown in Fig. 8. Both of the circuits are fed with same inputs and test pattern. Allow them to work in both normal mode and test mode. Both of the outputs are compared and find the number of faults in the circuit.

Then the faulty circuit is injected with test points, and again repeats the same process. Then an increment in the fault detection is noticed and is shown in the Table I.

Fig. 10. shows the areas in which faults are made in the circuit. Likewise faults are injected in diffrenet circuit elements.

4.1 Results

Fig. 11 and 12 shows the waveform of the circuit without test point insertion and with test point insertion respectively. In the first result it showed an 80% of the test coverage but in second case it is increased to 90%. These results are tabulated in Table I.

PARAMETERS	DFT WITHOUT TPI	DFT WITH TPI
NO.OF INSERTED FAULTS	80	80
NO.OF DETECTED FAULTS	64	72
FAULT COVERAGE	80%	90%

Table-1: Analysis of the results.

5. CONCLUSION

The problem of increasing the test coverage of the SCL design is investigated for a 32- to- 5 bit priority encoder. Test point insertion resulted in considerable increment in the test coverage, and provided a 90% of test coverage. Asynchronous circuits have the potential to be faster, and may also have advantages in lower power consumption, lower electromagnetic interference, and better modularity in large systems therefore synchronous circuits are an active area of research in digital logic design. And hence a better testing procedure is needed.

Future work consists of exploring other testing techniques, such as delay testing and quiescent current (IDDQ) testing. Since stuck-at faults cannot model all the possible defects in the CMOS technology, other testing techniques are usually used in addition to stuck-at fault testing to increase fault coverage. For example, transistor-level faults that are notcovered by the stuck-at fault model, such as bridging faults, stuck-shorts, and stuck-opens, could be potentially tested using IDDQ testing. In addition, in the SCL pipeline, some redundant faults such as the stuck-at-0 faults on the sleep signal forks within a combinational logic block or a completion detector block might be testable using delay testing.

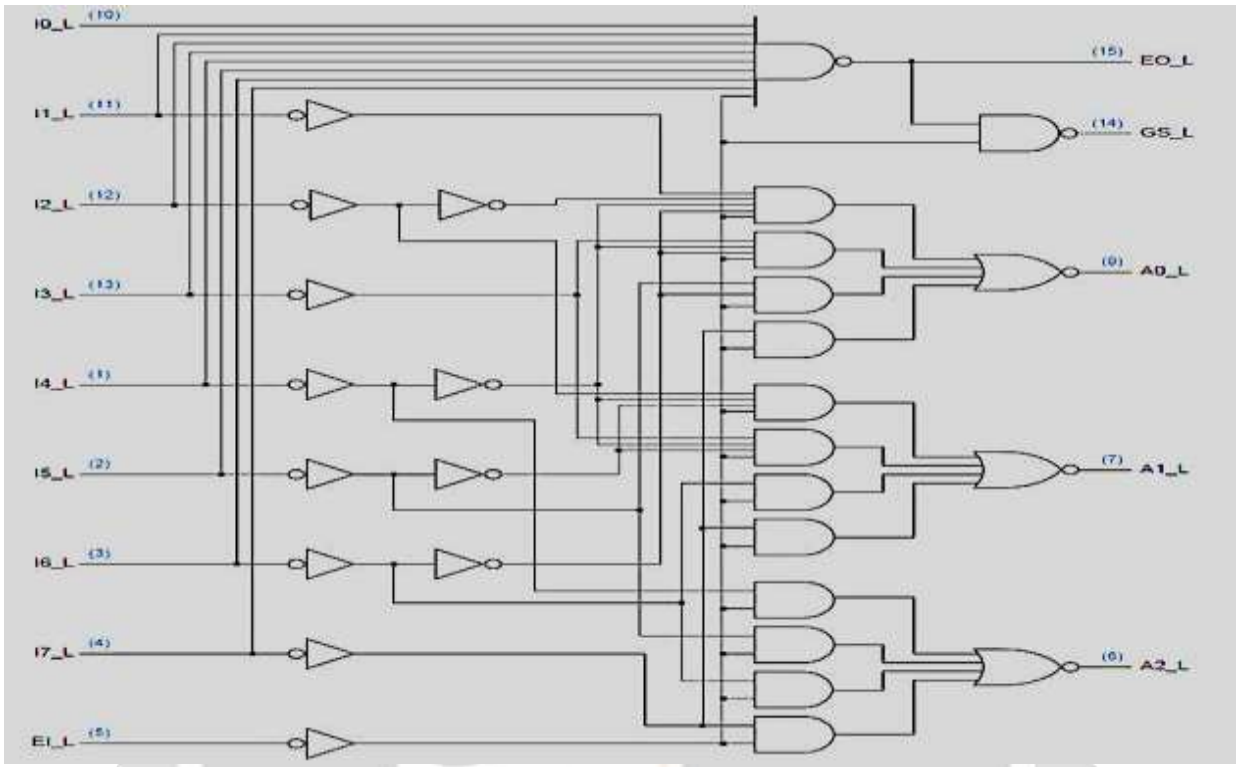


Fig- 6: Circuit diagram of 8- to- 3 bit priority encoder.

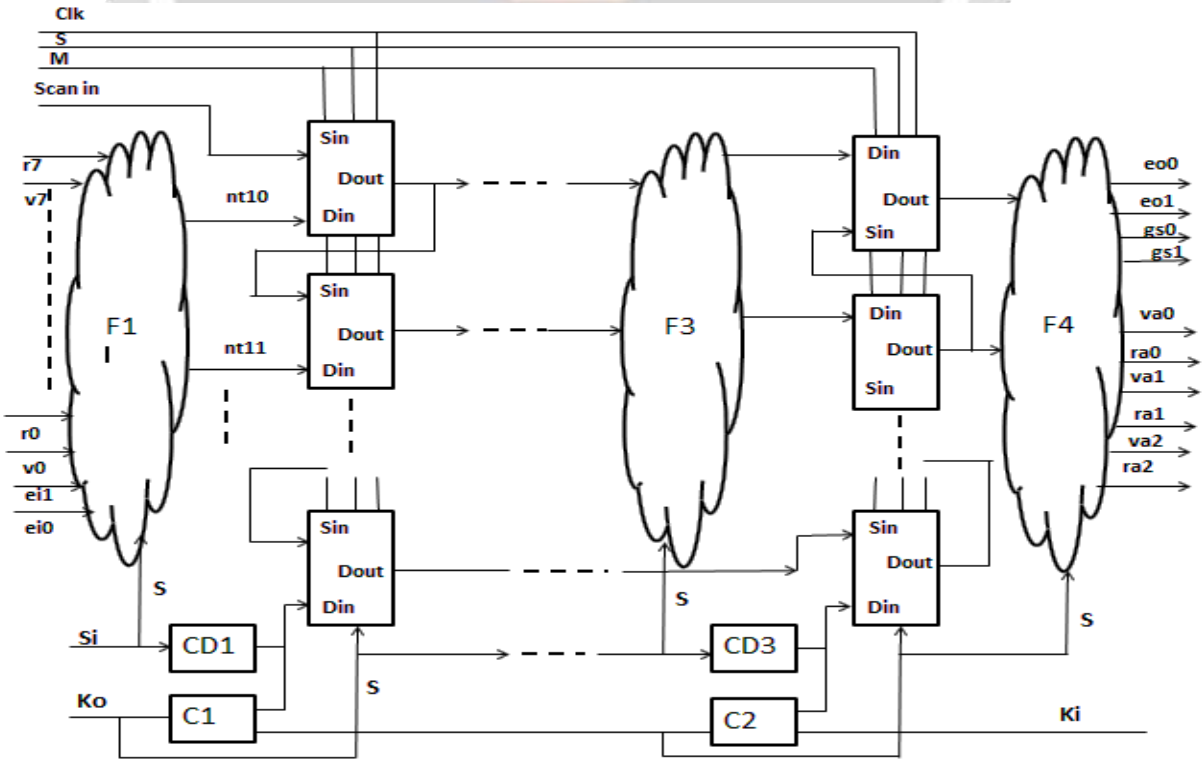


Fig- 7: Functional block diagram of 8- to- 3 bit priority encoder.

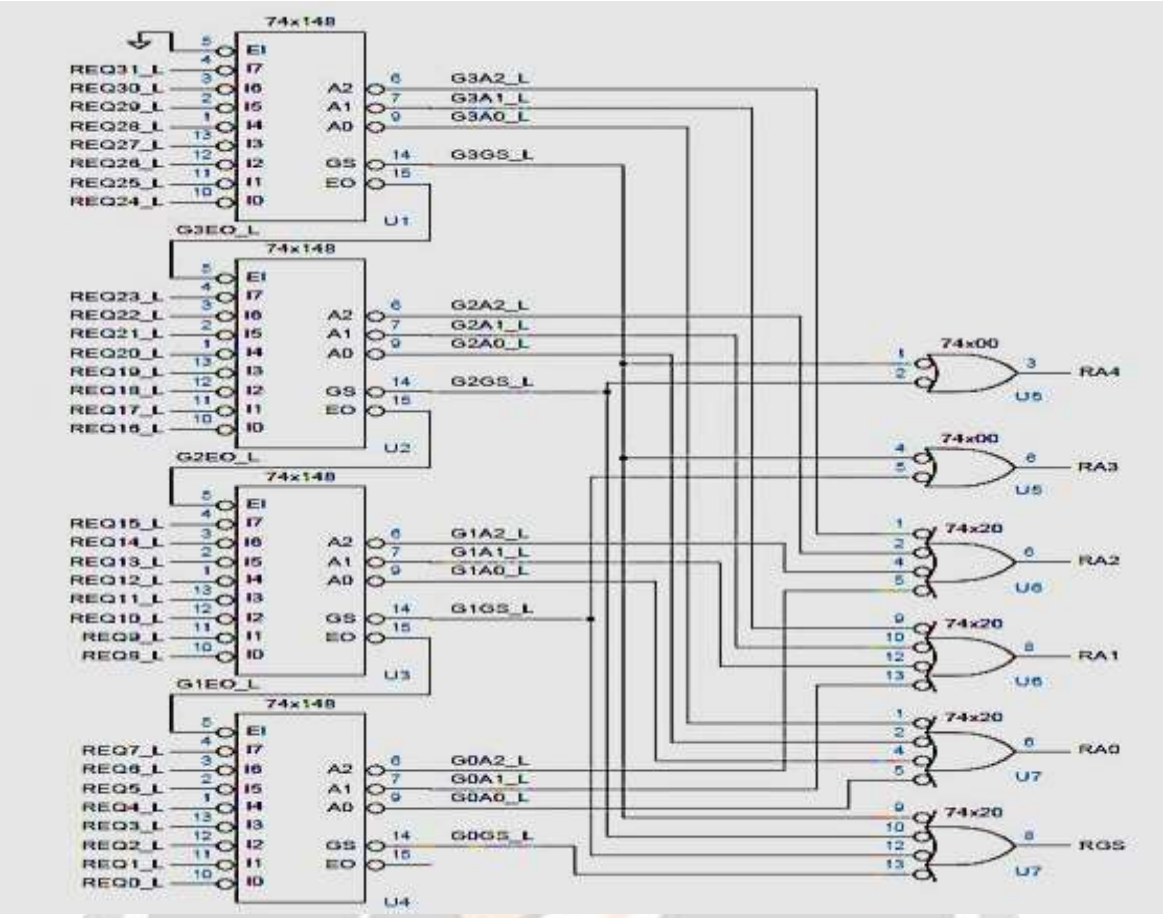


Fig- 8: Circuit diagram of 32- to- 5 bit priority encoder.

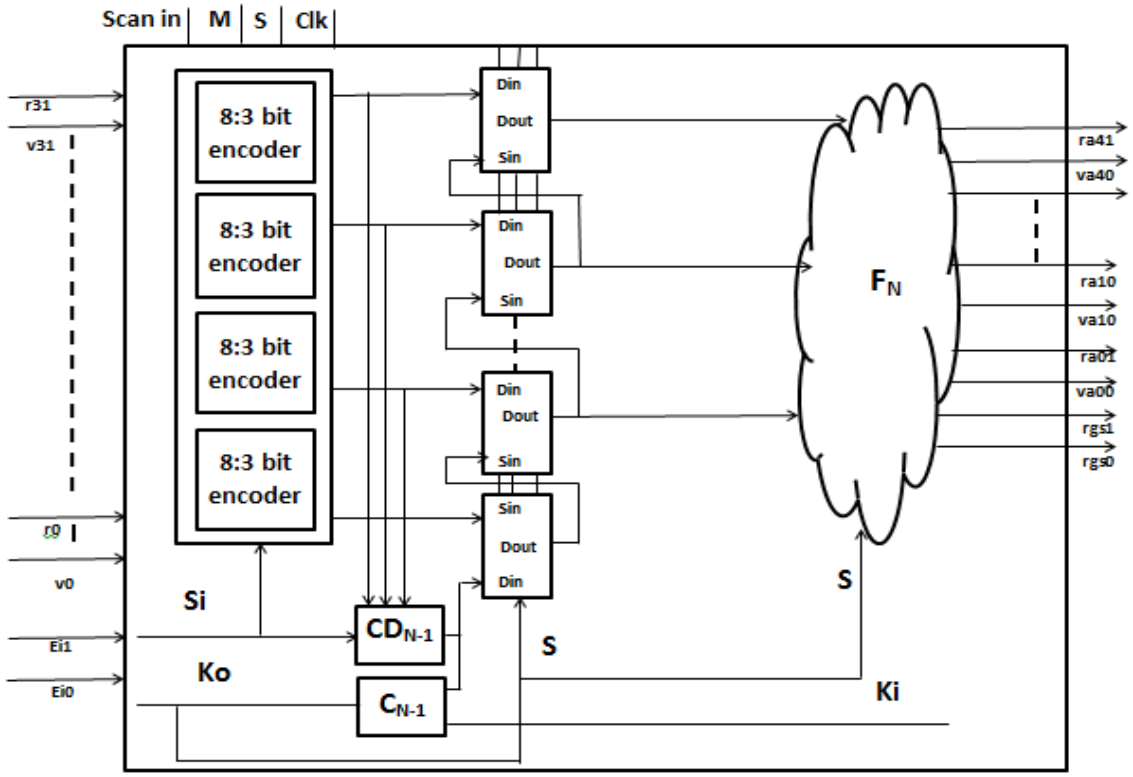


Fig-9: Functional block diagram of 32- to- 5 bit priority encoder.

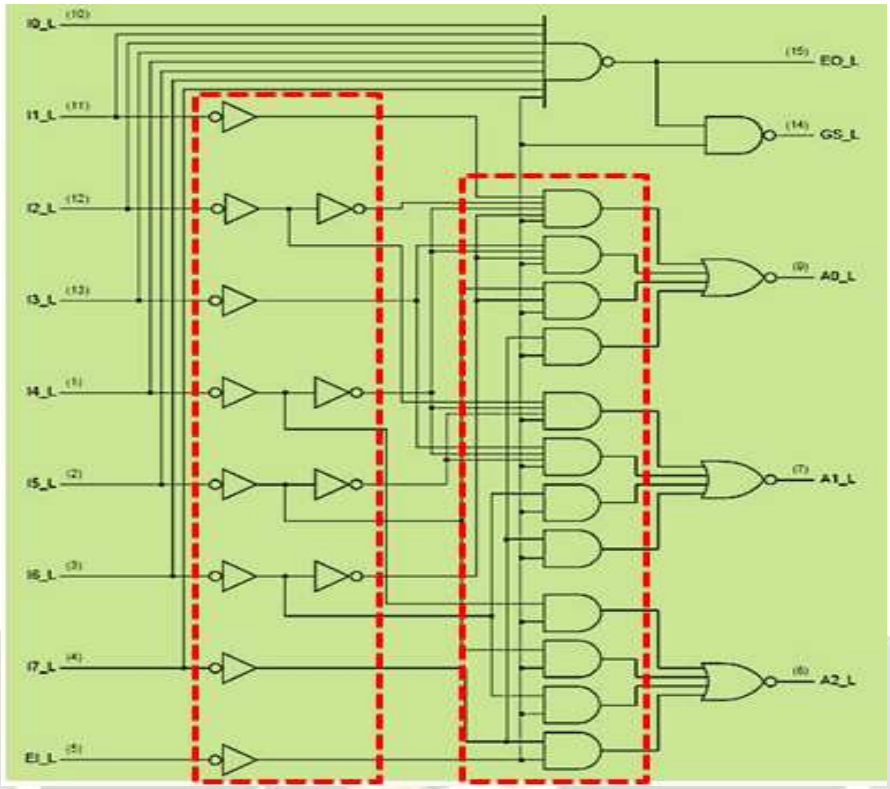


Fig-10: Area in which faults are made.

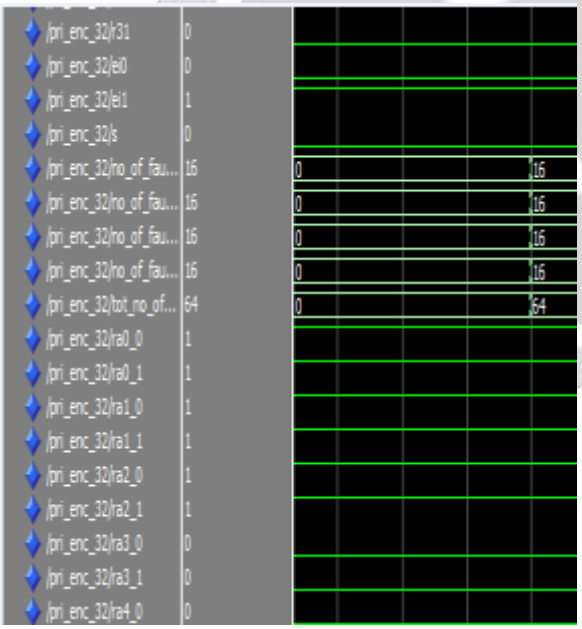


Fig-11: Output waveform of the faulty 32- to- 5 bit priorityencoder without test point insertion.

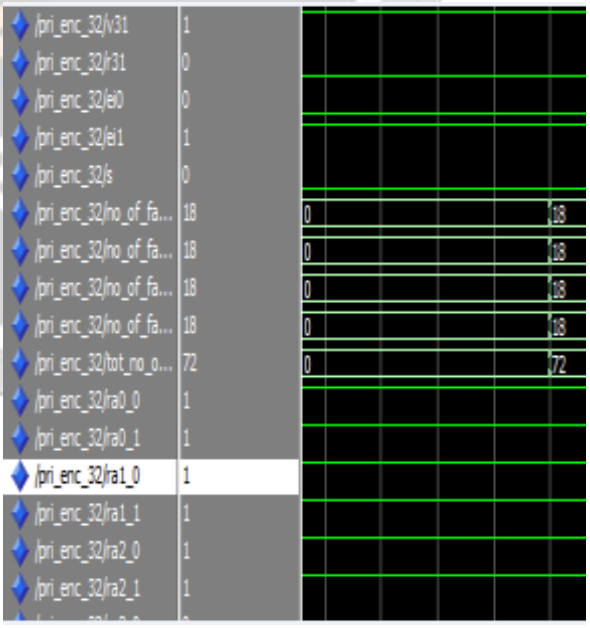


Fig-12: Output waveform of the faulty 32- to -5 bit priority encoder with test point insertion

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