INVESTIGATION OF DC-DC CONVERTER FOR POWER FACTOR IMPROVEMENT USING MODIFIED SEPIC CONVERTER

L Vijaya[1], K Nagaraju[2]
[1] Student, Dept of EEE, Kshatriya College of Engineering, Telangana, India
[2] Asst.Prof, Dept of EEE, Kshatriya College of Engineering, Telangana, India

ABSTRACT

This paper is proposed on analysis of a modified SEPIC dc–dc converter used as pre regulator operating in discontinuous conduction mode (DCM) is presented. The proposed converter presents a low input current ripple operating in DCM, and the switch voltage is lower than the output voltage for efficiency point of view. The switch voltage reduction increases the converter reliability and a low drain-to-source on-resistance (R_{DSon}) MOSFET can be used depending on the converter specification. To analyze the performance of the proposed converter MATLAB/SIMULINK software has used. To reduce the third-harmonic input current distortion resultant of the operation in DCM is very helpful. The results shown using proposed software are matching to the theoretical analysis.

Keyword: - *DC-DC Converter, SEPIC Converter*, Mosfet, Power Factor

1. INTRODUCTION

Power supplies are categorized in various ways, including by functional features. For example, a regulated power supply is one that maintains constant output voltage or current despite variations in load current or input voltage. Conversely, the output of an unregulated power supply can change significantly when its input voltage or load current changes. Adjustable power supplies allow the output voltage or current to be programmed by mechanical controls (e.g., knobs on the power supply front panel), or by means of a control input, or both. An adjustable regulated power supply is one that is both adjustable and regulated. An isolated power supply has a power output that is electrically independent of its power input; this is in contrast to other power supplies that share a common connection between power input and output.

DC-DC converters are electronic devices used whenever we want to change DC electrical power efficiently from one voltage level to another. They are needed because unlike AC, DC cannot simply be stepped up or down using a transformer. In many ways, a DC-DC converter is the DC equivalent of a transformer. Typical applications of DC-DC converters are where 24V DC from a truck battery must be stepped down to 12V DC to operate a car radio, CB transceiver or mobile phone. where 12V DC from a car battery must be stepped down to 3V DC, to run a personal CD player; where 5V DC on a personal computer motherboard must be stepped down to 3V, 2V or less for one of the latest CPU chips, where the 340V DC obtained by rectifying 240V AC power must be stepped down to 5V, 12V and other DC voltages as part of a PC power supply; where 1.5V from a single cell must be stepped up to 5V or more, to operate electronic circuitry, where 6V or 9V DC must be stepped up to 500V DC or more, to provide an insulation testing voltage, where 12V DC must be stepped up to +or -40V or so, to run a car hi-fi Amplifiers circuitry or where 12V DC must be stepped up to 650V DC or so, as part of a DC-AC sine wave inverter.

Since the input inductor of the boost converter operates in DCM, a high-frequency filter composed by an inductor *Lf* and capacitor *Cf* must be used in the preregulator input in order to reduce the input current ripple, as presented in Fig. 1.3 However, a problem presented by the boost preregulator operating in DCM is the input current distortion, presenting a third-harmonic component.

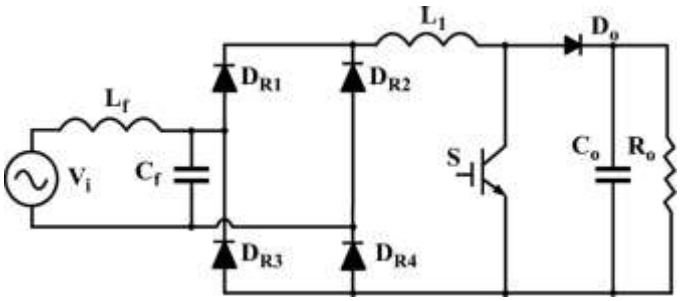

Fig-1: Classical boost preregulator operating in DCM

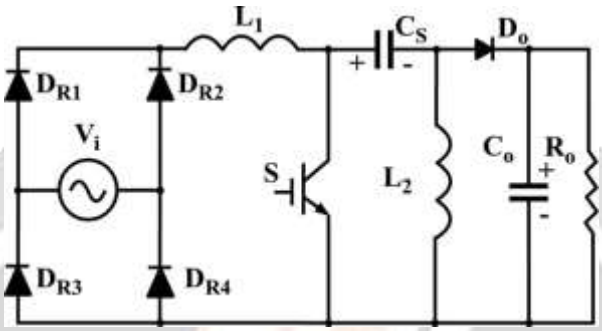

Fig-2: Classical SEPIC preregulator operating in DCM

The voltage applied across the input inductor during its demagnetization is equal to the output voltage minus the input voltage; hence, the current distortion increases when the difference between the output voltage and the peak input voltage is reduced. Therefore, the output voltage can be increased, reducing the third-harmonic input current distortion and improving the power factor. Also a variable duty-cycle control can be used in order to reduce the input current distortion as presented in Section V. The boost converter can operate with unitary power factor independently of the difference between the output and input voltage operating at the boundary of the DCM and continuous conduction mode (CCM) with a variable switching frequency modulation. The classical SEPIC converter, shown in Fig. 2 presents a step-up/step-down static gain and usually is used as an HPF preregulator in applications where the output voltage must be lower than the peak of the ac input voltage [3], [4]. The implementation of the preregulator using the classical SEPIC converter in DCM presents two additional operation characteristics.

[1]. Firstly, the converter operates as a voltage follower when designed in DCM with a low value for the inductor *L*2 and using a high value for the inductor *L*1 , but the input current presents a low current ripple just as a boost rectifier operating in CCM with current-control loop. Consequently, the *Lf –Cf* filter used in the boost converter input operating in DCM is not necessary using the SEPIC converter operating in DCM. Therefore, the number of components for both converters operating in DCM is equal. However, in a practical application, an electromagnetic interference (EMI) filter is necessary as in any rectifier topology.

[2]. The second important characteristic using the SEPIC converter in DCM is that the input current follows the input voltage waveform without input current distortion. The third-harmonic distortion is not presented because the inductor *L*2 is demagnetized with the output voltage.

Nevertheless, the boost converter is the preferred topology used for the preregulator application where the output voltage must be higher than the peak of the input voltage, given that the switch voltage of the SEPIC converter is equal to the sum of the input and output voltages. The SEPIC converter can be successfully used in applications where the output voltage is lower than the input voltage. Several high-efficiency bridgeless configurations using the SEPIC and CUK converters are presented in [5]–[10].

2. PROPOSED TECHNIQUE

A modified SEPIC dc–dc converter was proposed in [11] with the inclusion of an additional diode (*DM*) and capacitor (*CM*) at the classical SEPIC converter, changing several characteristics such as the operation with a switch voltage lower than the output voltage. However, only the operation as dc–dc converter in CCM was analyzed in [11]. This converter was also used in [12] as a preregulator operating in CCM presenting some advantages when

compared with the classical boost preregulator operating in CCM for universal line input application (90 *V*rms – 260 *V*rms). Notwithstanding, the theoretical and experimental analyses of the modified SEPIC converter operating in DCM as a dc–dc converter and preregulator were not presented yet, which is focus of this paper. The proposed topology presents the same limitations of the classical boost converter when compared with the classical SEPIC converter because its operation is solely possible as a non isolated converter with step-up static gain. Differently from the classical SEPIC converter, an auxiliary inrush limitation circuit must be included for the rectifier start-up. Also, the power factor is lower than the classical SEPIC converter due to the third-harmonic component in the input current. However, the power factor and the input current distortion of the modified SEPIC converter can be significantly improved applying a simple open-loop action using the input and output voltage information. The use of the boost and modified SEPIC rectifiers are only possible in applications with an output voltage higher than the peak of the input voltage, and these rectifiers are more appropriated than the SEPIC converter with the same specification, since the SEPIC converter presents a high switch voltage. The lowest switch voltage level is presented by the modified SEPIC topology.

2.1 ADVANTAGES OF PROPOSED CONVERTER

[1]. The modified SEPIC converter operates as a voltage follower and the input current presents low current ripple such as a classical SEPIC converter.
[2]. Designing the converter in DCM and using a low value for the inductor *L*2 and a high value for the inductor *L*1.
[3]. the power factor is lower than the classical SEPIC converter.
[4]. the third-harmonic component in the input current is minimized.
[5]. Output voltage higher than the peak of the input voltage.

3. PRINCIPLE OF OPERATION

The circuit of the preregulator using the modified SEPIC converter operating in DCM is presented in Fig. 5.1. The main difference from the preregulator presented in [12] is the operation mode and the control system that is composed by only a voltage control loop due to the DCM operation. Also, the non dissipative current snubber used in [12] is not necessary because the reverse recovery current of the diodes and the turn-on switching losses operating in CCM are reduced with the DCM operation. The modified SEPIC dc–dc converter operating in DCM presents three operation stages. The theoretical analysis is initially developed considering the operation as a dc–dc converter at steady state and all circuit components are considered ideal. The voltages across all capacitors are considered constant during a switching period, as an ideal voltage source. The DCM operation occurs when there is the third operation stage, where the power switch is turned off and the currents in all diodes of the circuit are null. Therefore, the DCM operation occurs when *Do* and *DM* diodes are blocked before the switch turn-on. The analysis and design procedure is also developed for the operation as a preregulator with a diode bridge at input and an ac input voltage, based on the study as dc–dc converter.

The circuit presents two inductors, thus, different inductor values combination can be adopted for the DCM operation. In order to reduce the input current ripple of the preregulator, a relative high value for the inductor *L*1 is considered. A relative low value of the inductor *L*2 is used for the converter operation in DCM as a voltage follower, where the input current follows the input voltage waveform. As a result, the preregulator input current follows the input voltage waveform with low current ripple, without input filter and without current-control loop. An important equation for the operation analysis of the converter is presented.

Considering the operation at steady state, the average voltage across the inductors *L*1 and *L*2 are null and the sum of the input voltage *Vi* and capacitor *CS* voltage is equal to the capacitor *CM* voltage.

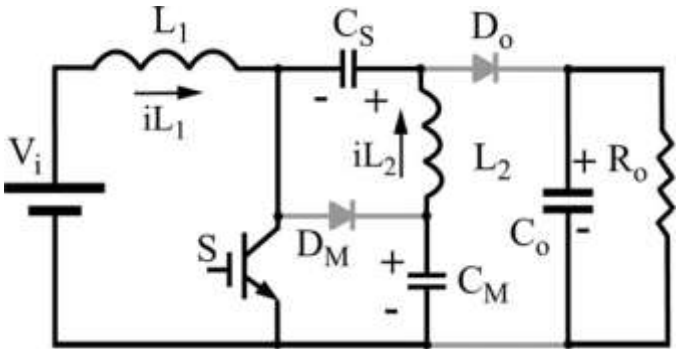

Fig-3: First operation stage.

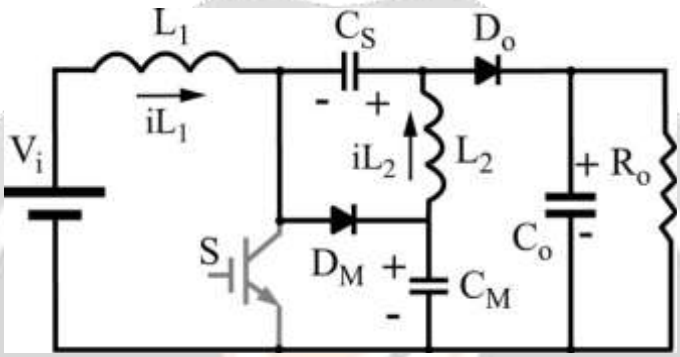

Fig-4: Second operation stage.

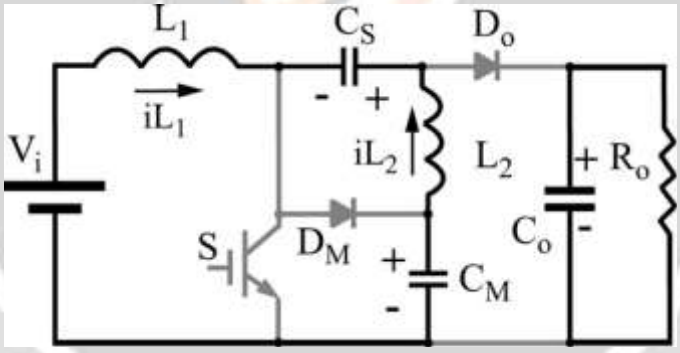

Fig-5: Third operation stage.

The operation stages in DCM are presented as follows:

$$V_{CM} = V_i + V_{CS}. \qquad (1)$$

1) First Stage [t0 − t1] (see Fig. 5.2): During the conduction of the power switch *S*, the input inductor stores energy with the input voltage applied across *L*1 (V_{L1}). The voltage applied across *L*2 (V_{L2}) is equal to the voltage of capacitor *CM* minus the voltage of capacitor *CS*. As presented in (1), this voltage difference is equal to the input voltage. Therefore, inductors *L*1 and *L*2 store energy in this operation stage and the same voltage is applied across these inductors. The currents through inductors *L*1 and *L*2 increase following (3) and (4), respectively, but since *L*2 is lower than *L*1 , the current variation in *L*2 is higher than in *L*1 , as presented in the theoretical waveforms shown in Fig. 5.5. The diodes *DM* and *Do* are blocked during this operation stage

$$V_{L_1} = V_{L_2} = V_i$$
$$\Delta i_{L_1} = \frac{V_i \cdot D}{L_1 \cdot f}$$
$$\Delta i_{L_2} = \frac{V_i \cdot D}{L_2 \cdot f} \quad \text{.....(2)}$$

Where *f* is the switching frequency and *D* is the converter duty cycle.

2) Second Stage [t1 − t2] (see Fig. 5.3): At the instant *t*1 , switch *S* is turned off and the energy stored in the input inductor *L*1 is transferred to the output through the *CS* capacitor and output diode *Do* . There is also energy transference to *CM* capacitor through diode *DM* and the maximum switch voltage is equal to the *CM* capacitor voltage. The energy stored in inductor *L*2 is also transferred to the output and capacitor *CS* through diodes *Do* and D_M . The voltage applied across *L*1 is equal to *CM capacitor* voltage minus the input voltage and this difference is equal to the *CS* capacitor voltage as calculated by (1). The voltage across the inductor *L*2 is equal to the negative capacitor *C*S voltage. Thus, the voltage applied across the inductor *L*1 and *L*2 are equal to the negative capacitor *CS* voltage during this operation stage and the inductor current variation is calculated
by (6) and (7), respectively.

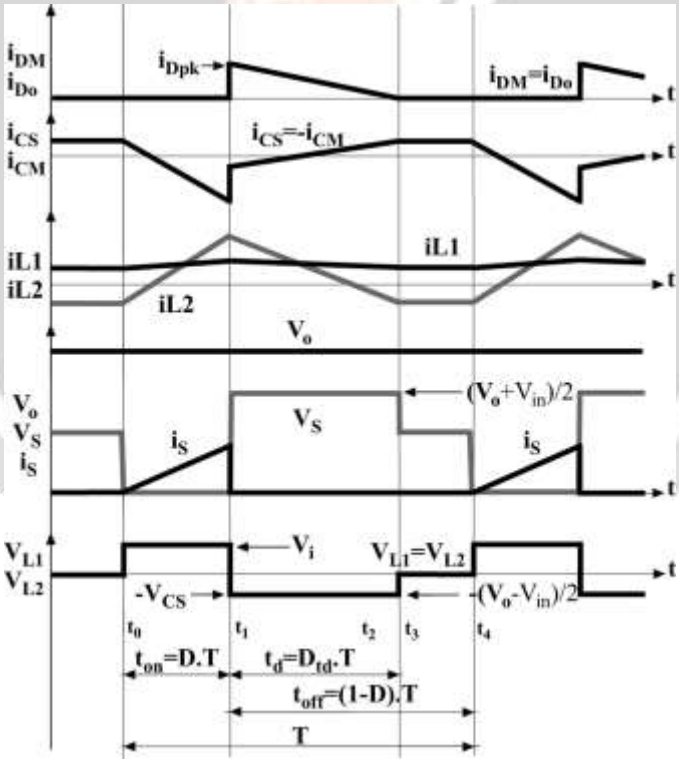

Fig-6: Main theoretical waveforms.

As presented in Fig. 6, the time interval (*t*2–*t*1) of the second operation stage is defined as *td* and is equal to the transference period of the energy stored in inductors *L*1 and *L*2 through diodes *Do* and *DM* . When *L*2 current value becomes equal to *L*1 current value with the same direction, the currents at diodes *Do* and *DM* becomes null, finishing this operation stage. Therefore, *td* is the conduction time of diodes *DM* and *Do* , when the energy stored in the inductors *L*1 and *L*2 is transferred.

$$V_{L_1} = V_{L_2} = -V_{C_S}$$
$$-\Delta i_{L_1} = \frac{-V_{C_S} \cdot D_{t_d}}{L_1 \cdot f}$$
$$-\Delta i_{L_2} = \frac{-V_{C_S} \cdot D_{t_d}}{L_2 \cdot f} \quad \text{.....(3)}$$

$$D_{t_d} = \frac{t_d}{T} = t_d \cdot f. \quad \text{.....(4)}$$

3) Third Stage [t3 − t4] (see Fig. 6): When diodes *Do* and *DM* are blocked at the instant *t*3 , the voltage applied across the inductors *L*1 and *L*2 are null, maintaining the inductors currents constant as presented in (9) and (10). The currents through the inductors *L*1 and *L*2 present the same value, operating as a freewheeling stage. This operation stage is finished when the power switch is turned on at the instant *t*4, returning to the first operation stage. The main theoretical waveforms are presented in Fig.6. The switch turn-on occurs with ZCS such as a classical dc–dc converter operating in DCM and the diodes do not present reverse recovery current. The maximum switch voltage is equal to the capacitor *CM* voltage, and this voltage is lower than the output voltage. The *L*1 inductor average current is equal to the input current and the *L*2 inductor average current is equal to the output current. The average current in the capacitors *CS* and *CM* are null at steady state; thus, the average current of diodes *DM* and *Do* are equal to the output current. The preregulator operation in DCM allows obtaining HPF without a current-control loop and only a voltage control loop is necessary [14]. The output voltage control algorithm used in the proposed converter is based on the classical PI controller. The design procedure can be simplified using a design procedure similar to the classical boost converter.

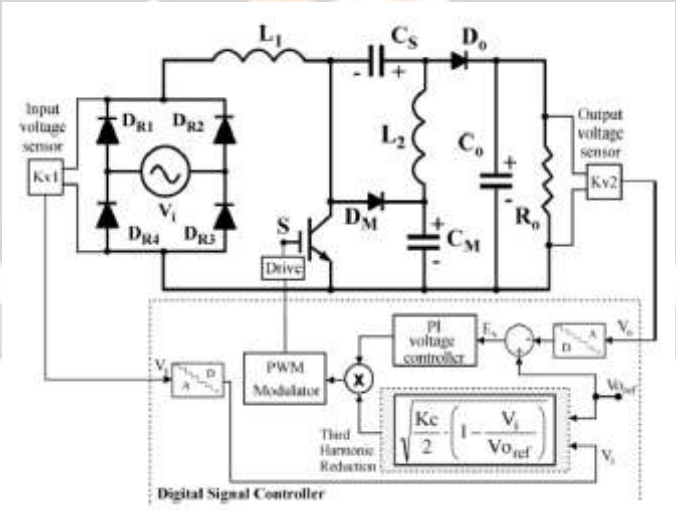

Fig-7: Block diagram of the preregulator control system.

Also, the 120 Hz ripple of the preregulator output voltage must be rejected by the voltage control loop in order to maintain the HPF operation. Therefore, the voltage control loop presents a very slow dynamic response such as any classical pre regulators. The block diagram of the digital control implementation is presented in Fig. 18, including the third-harmonic reduction technique. Only the output and input voltages are necessary to control the preregulator. The control algorithm was developed using a digital signal processor TMS320F2812, operating with sampling rate equal to 30 kHz. The sampled output voltage signal is compared to an output voltage reference and the error is applied to a PI voltage controller. Simultaneously, the sampled rectified input voltage and the output voltage reference are applied to (63) in order to calculate the duty-cycle variation for the third-harmonic reduction. The result of the PI output voltage controller and the result of the third-harmonic reduction are multiplied obtaining the preregulator duty cycle and generating the PWM signal that controls the switch *S*.

TABLE-I: PREREGULATOR COMPONENTS

Parameter	Preregulator with modified SEPIC converter
Inductor L_1	$L_1 = 6.8$ mH, ESR $= 692$ mΩ
Inductor L_2	$L_2 = 540\ \mu$H, ESR $= 98$ mΩ
Capacitor C_S	$C_S = 220$ nF, ESR $= 10$ mΩ
Capacitor C_M	$C_M = 220$ nF, ESR $= 10$ mΩ
Output capacitor C_o	$C_o = 120\ \mu$F, ESR $= 390$ mΩ
Diodes $D_M - D_o$	$D_M = D_o =$ UF5408 $V_f = 1.7$V
Power switch S	$S =$ FQA28N50 $V_{DSS} = 500$ V $R_{DSon} = 0.16\Omega$ (25 °C)

4 SIMULATION RESULTS

The preregulator operation with nominal output power and input voltage equal to *Vi* = 127 V_{rms} are presented from Figs. 23 to 30, considering the operation with the third-harmonic reduction technique. The *L*1 and *L*2 currents are presented in Fig. 23 and its current ripple is close to the theoretical values 0.3 and 3.56 A, respectively The *CS* and *CM* capacitor voltages are presented in Fig. 24. The theoretical value of the *CS* and *CM* capacitor voltages at the peak of the input voltage, considering the capacitor voltage ripple null, is equal to 110 and 290 V, respectively The switch voltage and current are presented in Figs. 25 and 26. The maximum switch voltage is close to 300 V for an input voltage equal 127 *V*rms and output voltage equal to 400 V.

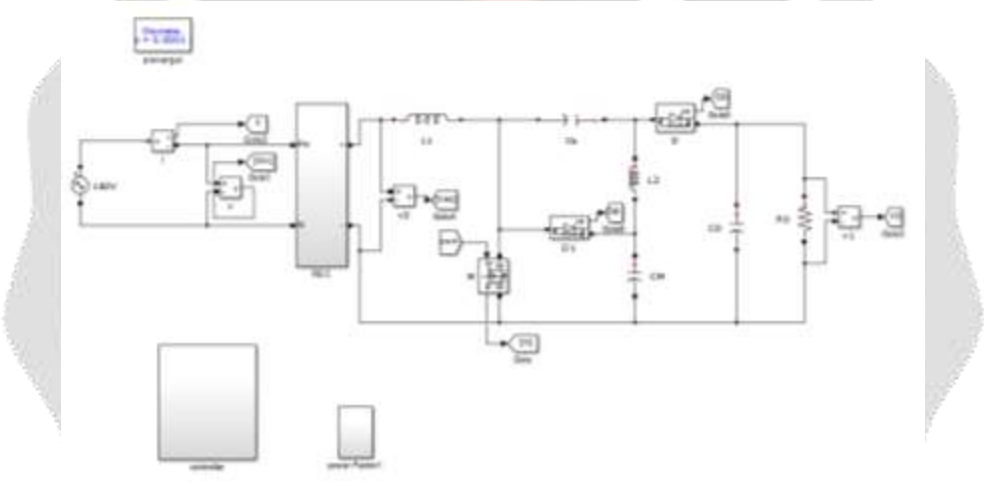

Fig-8: Simulation diagram of the proposed system

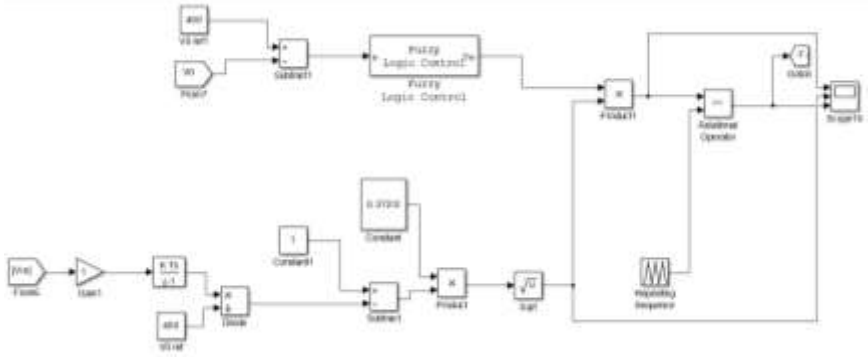

Fig-9: Proposed third harmonic based controller with fuzzy logic controller

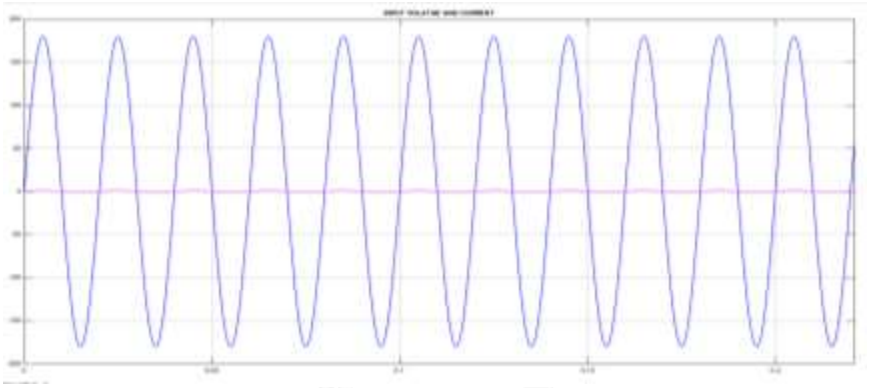

Fig-10: Input voltage and current using proposed controller

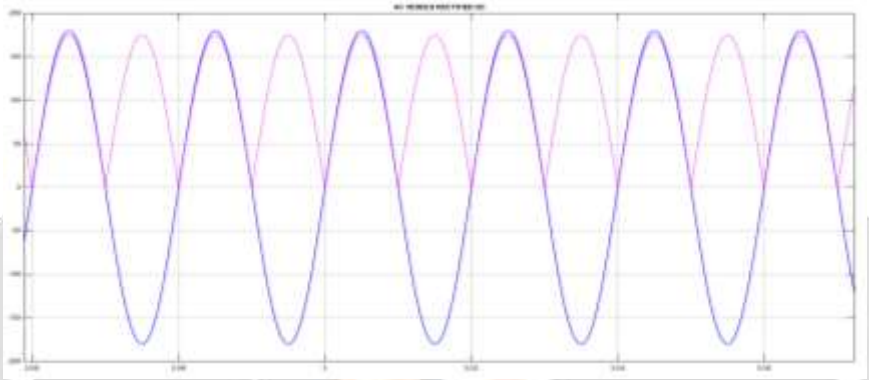

Fig-11: Input voltage(blue) and rectified voltage(pink)

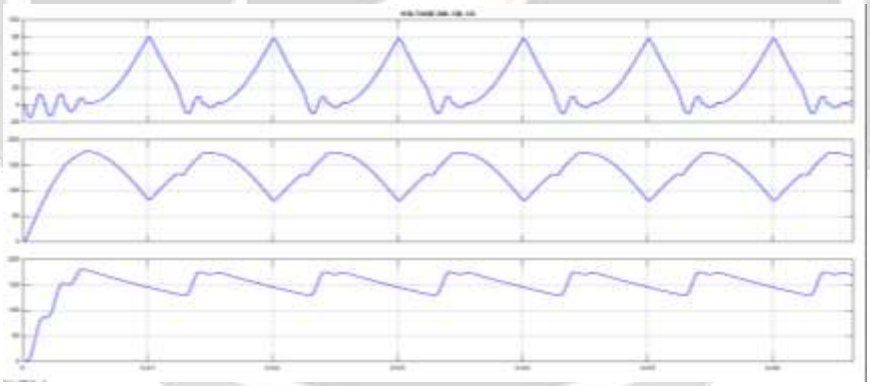

Fig-12: voltage across capacitors C_M, C_S, C_0

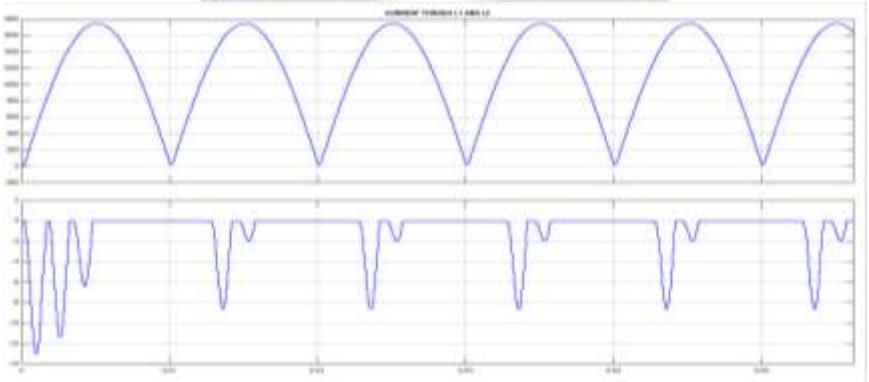

Fig-13: current through L_1 and L_2

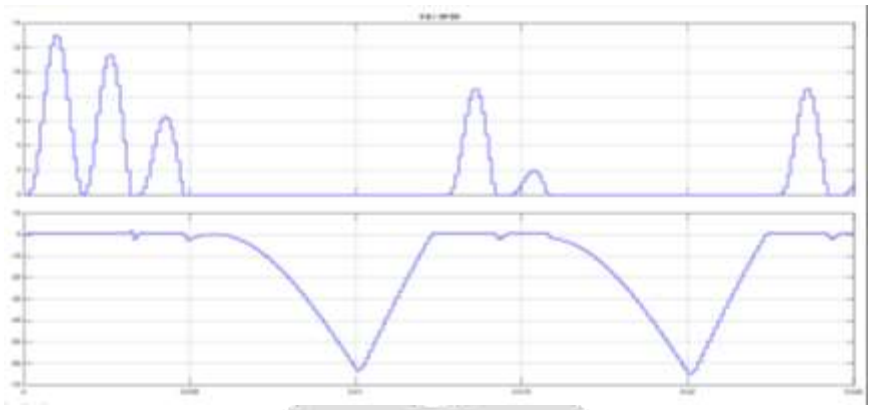

Fig-14: voltage and current of diode D_0

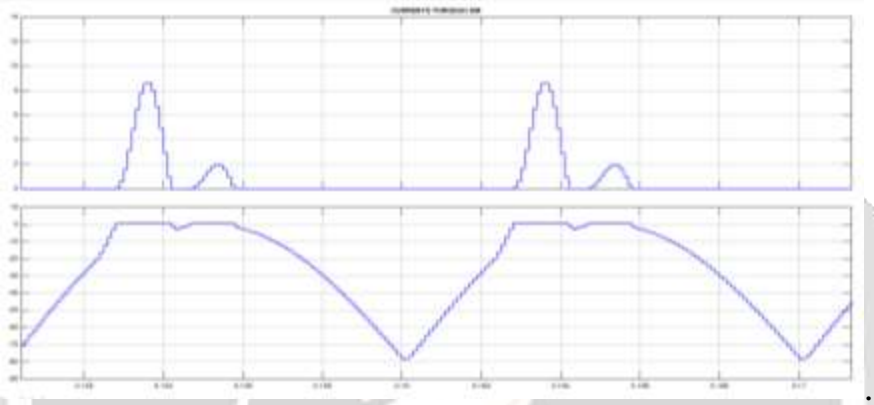

Fig-15: voltage and current of D_M

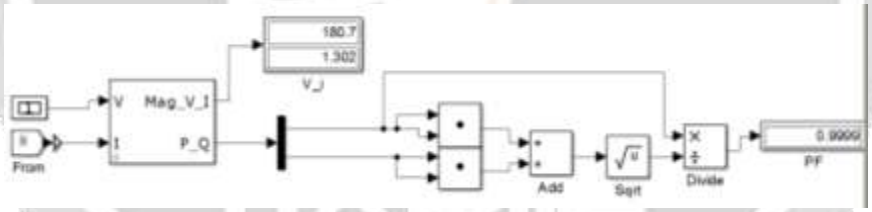

Fig-16: power factor when using Fuzzy logic controller

5. CONCLUSIONS

The analysis of the modified SEPIC converter used as preregulator operating in DCM is presented in this paper. The proposed converter presents low input current ripple operating in DCM and the switch and diodes voltages are lower than the output voltage. The switch voltage reduction increases the converter reliability and a lower $R_{DSon.}$ MOSFET can be used depending on the converter specification The simulation results presented operating with the third harmonic reduction technique and fuzzy controller shows that the total input current harmonic distortion is reduced from 13% to 5.3% operating with an input voltage equal 127 *V*rms, considering a total input voltage harmonic distortion equal to 3.1%. The power factor is higher than 0.998 with the third harmonic reduction in all input voltage range. The efficiency operating with input voltage equal to 127 *V*rms and output power equal to 108 W is equal to 95.6%. The simulation results show that there is also an increment in the converter efficiency operating with the third-harmonic reduction modulation that mainly occurs at light load operation in 127 *V*rms. The fuzzy logic controller is instead for PI for performance analysis.

6. REFERENCES

[1] O. Garc´ıa, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: A survey," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 749–755, May 2003.

[2] M.M. Jovanovic andY. Jang, "State-of-the-art, single-phase, active power factor-correction techniques for high-power applications—An overview," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 701–708, Jun. 2005.
[3] D. S. L. Simonetti, J. Sebastian, and J. Uceda, "The discontinuous conduction mode SEPIC and CUK power factor pre regulators: Analysis and design," *IEEE Trans. Ind. Electron.*, vol. 44, no. 5, pp. 630–637, Oct.1997.
[4] M. Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC rectifier with reduced components and conduction losses," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4153–4160, Sep. 2011.
[5] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "New efficient bridgeless Cuk rectifiers for PFC applications," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3292–3301, Jul. 2012.
[6] E. H. Ismail, "Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1147–1157, Apr. 2009.
[7] B. Su, J. Zhang, and Z. Lu, "Totem-pole boost bridgeless pfc rectifier with simple zero-current detection and full-range zvs operating at the boundary of DCM/CCM," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 427–435, Feb. 2011.
[8] J. Zhang, B. Su, and Z. Lu, "Single inductor three-level bridgeless boost power factor correction rectifier with nature voltage clamp," *IET Power Electron.*, vol. 5, no. 3, pp. 358–365, Mar. 2012.
[9] Y. Cho and J.-S. Lai, "Digital plug-in repetitive controller for single-phase bridgeless pfc converters," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 165–175, Jan. 2013.
[10] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "Bridgeless resonant pseudo boost PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5949–5960, Nov. 2014.
[11] R. Gules, W. M. Santos, F. A. Reis, E. F. R. Romaneli, and A. A. Badin, "A modified SEPIC converter with high static gain for renewable applications," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5860–5871, Nov. 2014.
[12] P. F. de Melo, R. Gules, E. F. R. Romaneli, and R. C. Annunziato, "A modified SEPIC converter for high-power-factor rectifier and universal input voltage applications," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 310–321, Feb. 2010.