INVESTIGATION OF VARIOUS PWM TECHNIQUES FOR SOLAR PV INVERTER

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ABSTRACT

In this paper various PWM techniques for solar Inverter are investigated for performance analysis of the system interms of the output RMS voltage, total harmonic distortion, output current and common mode voltages. The concept of virtual bus has proposed in order to eliminate the common-mode (CM) leakage current in the transformerless photovoltaic (PV) systems. By connecting the grid neutral line directly to the negative pole of the dc bus, the stray capacitance between the PV panels and the ground is bypassed. As a result, the CM ground leakage current can be suppressed completely. Meanwhile, the virtual dc bus is created to provide the negative voltage level for the negative ac grid current generation. Consequently, the required dc bus voltage is still the same as that of the full-bridge inverter. Based on this concept, a novel transformerless inverter topology is derived. This topology is fed from solar, fuel cell and wind systems and modulation techniques such as PD, VFPWM and COPWM with the unipolar sinusoidal pulse width modulation and the double frequency SPWM were investigated to reduce the output current ripple using MATLAB/SIMULINK software

Keyword: - *Inverter, virtual DC bus, Photovoltaic, PD.*

1. INTRODUCTION

Hybrid renewable energy systems (HRES) are becoming popular for remote area power generation applications due to advances in renewable energy technologies and subsequent rise in prices of petroleum products. A hybrid energy system usually consists of two or more renewable energy sources used together to provide increased system efficiency as well as greater balance in energy supply. A grid-tie inverter is a power inverter that converts direct current (DC) electricity into alternating current (AC) with an ability to synchronize to interface with a utility line. Its applications are converting DC sources such as solar panels or small wind turbines into AC for tying with the grid. Inverters take DC power and invert it to AC power so it can be fed into the electric utility company grid. The grid tie inverter must synchronize its frequency with that of the grid (e.g. 50 or 60 Hz) using a local oscillator and limit the voltage to no higher than the grid voltage. A high-quality modern GTI has a fixed unity power factor, which means its output voltage and current are perfectly lined up, and its phase angle is within 1 degree of the AC power grid. However, supplying reactive power to the grid might be necessary to keep the voltage in the local grid inside allowed limitations. In the traditional grid-connected PV inverters, either a line frequency or a high-frequency transformer is utilized to provide a galvanic isolation between the grid and the PV panels. Because of Transformer isolation is there but circuit density, cost and losses is more. The efficiency is reduced. Grid-tie inverters that are available on the market today use a number of different technologies. The inverters may use the newer high-frequency transformers, conventional low-frequency transformers, or without transformer. Instead of converting direct current directly to 120 or 240 volts AC, high-frequency transformers employ a computerized multi-step process that involves converting the power to high-frequency AC and then back to DC and then to the final AC output voltage. Transformerless inverters, lighter and more efficient than their counterparts with transformers, are popular in Europe.

This paper presents an overview of a new virtual DC bus topology with Transformer less Grid Tie Inverter. This topology requires less number of components compared to conventional topologies. It is also more efficient since the inverter has a component which operates one additional switching power device is used to eliminate the leakage current. Therefore, there is no need for Transformer which leads to simpler and more reliable control of the inverter.

2 VIRTUAL DC BUS CONCEPTS

The concept of the virtual dc bus is depicted. By connecting the grid neutral line directly to the negative pole of the PV panel, the voltage across the parasitic capacitance *C*PV is clamped to zero. This prevents any leakage current flowing through it. With respect to the ground point N, the voltage at midpoint B is either zero or +*V*dc, according to the state of the switch bridge. The purpose of introducing the virtual dc bus is to generate the negative output voltage, which is necessary for the operation of the inverter. If a proper method is designed to transfer the energy between the real bus and the virtual bus, the voltage across the virtual bus can be kept the same as the real one.The positive pole of the virtual bus is connected to the ground point N, so that the voltage at the midpoint C is either zero or −*V*dc. The dotted line in the figure indicates that this connection may be realized directly by a wire or indirectly by a power switch. With points B and C joined together by a smart selecting switch, the voltage at point A can be of three different voltage levels, namely +*V*dc, zero, and −*V*dc. Since the CM current is eliminated naturally by the structure of the circuit, there is not any limitation on the modulation strategy, which means that the advanced modulation technologies such as the unipolar SPWM or the double-frequency SPWM can be used to satisfy various PV applications.

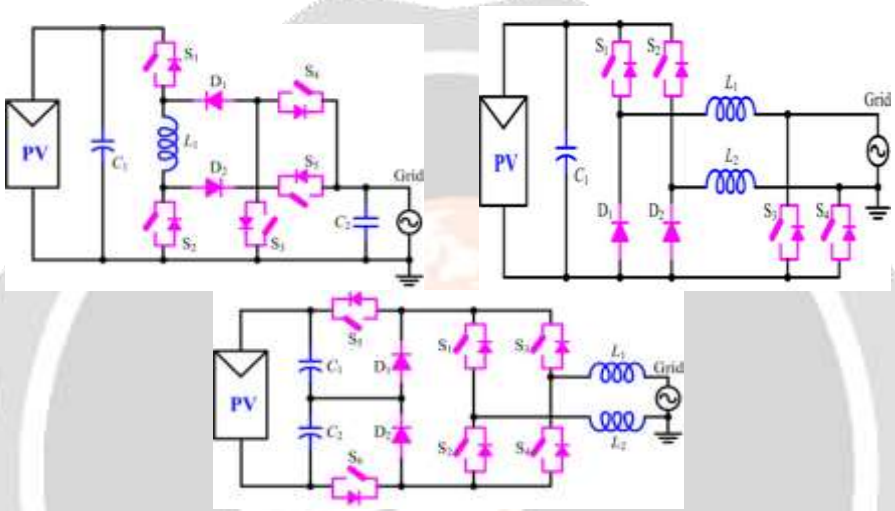

Fig.1: various PV Inverter topologies

3 DERIVED TOPOLOGY AND MODULATION STRATEGY

Based on the virtual dc bus concept, a novel inverter topology is derived as an example to show the clear advantages of the proposed methodology. It consists of five power switches S_1–S_5 and only one single filter inductor L_f. The PV panels and capacitor C_1 form the real dc bus while the virtual dc bus is provided by C_2.With the switched capacitor technology, C_2 is charged by the real dc bus through S_1 and S_3 to maintain a constant voltage. This topology can be modulated with the unipolar SPWM and double-frequency SPWM. The detailed analysis is introduced as follows.

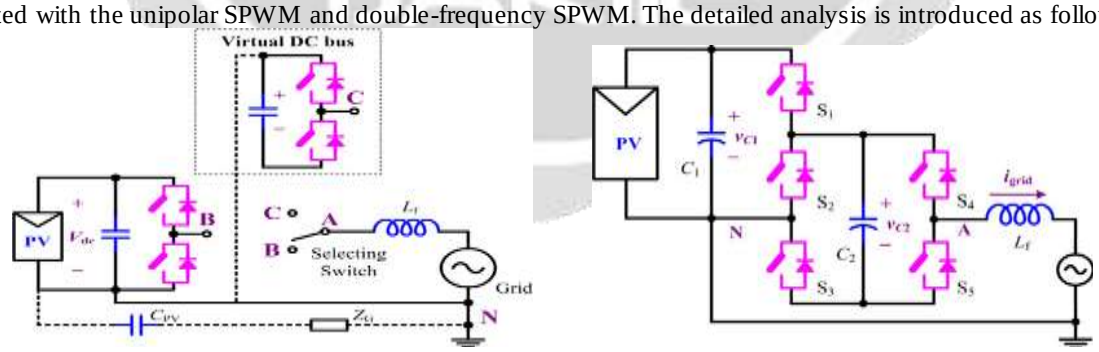

Fig.2: Proposed virtual bus topology

Unipolar SPWM

The waveform for the unipolar SPWM of the proposed inverter is displayed. The gate drive signals for the power switches are generated according to the relative value of the modulation wave u_g and the carrier wave u_c . During the positive half grid cycle, u_g >0. S_1 and S_3 are turned ON and S_2 is turned OFF, while S_4 and S_5 commutate complementally with the carrier frequency. The capacitors C_1 and C_2 are in parallel and the circuit rotates between states 1 and 2.

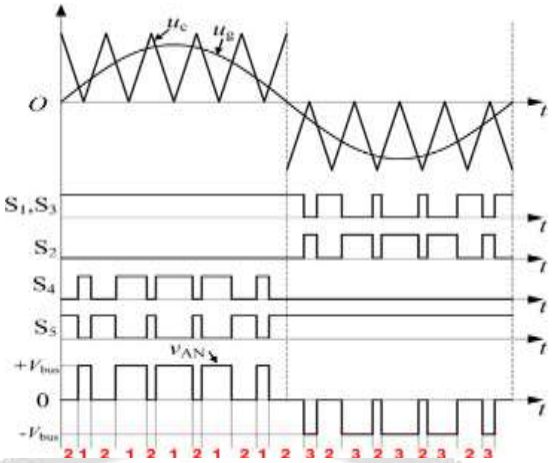

Fig.3: unipolar PWM

Unipolar Waveform

During the negative half cycle, u_g <0. S_5 is turned ON and S_4 is turned OFF. S_1 and S_3 commutate with the carrier frequency synchronously and S_2 commutates in complement to them. The circuit rotates between states 3 and 2. At state 3, S_1 and S_3 are turned OFF while S_2 is turned ON. The negative voltage is generated by the virtual dc bus C_2 and the inverter output is at negative voltage level. At state 2, S_1 and S_3 are turned ON while S_2 is turned OFF. The inverter output voltage v_{AN} equals zero; meanwhile, C_2 is charged by the dc bus through S_1 and S_3.

Carrier based PWM Techniques

Multilevel carrier-based PWM uses several triangular carrier signals, which can be modified in phase and/or vertical position in order to reduce the output voltage harmonic content. Modulation techniques for multilevel inverters are based on carrier arrangements. There are two common carrier modifications applied to the multilevel inverters. The carriers shifted horizontally are Phase Shifted Carrier PWM (PSCPWM). The carriers shifted vertically are Phase Disposition. The carrier disposition PWM strategies are commonly of three types are

1) Phase Disposition (PD)
2) Phase Opposition Disposition (POD)

Phase Disposition Technique

Phase disposition (PD), where all carriers are in phase shown. The arrangement of carriers and modulating wave for PD is shown in Fig 4 The PD strategy is now well accepted as achieving the lowest line-to-line harmonic voltage distortion.

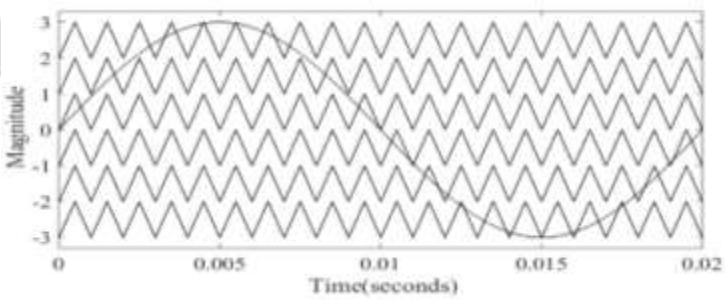

Fig 4Reference and carrier waveforms for PD

PD modulation achieves its superior line-to-line harmonic performance. In the harmonic spectra for one phase leg the most significant harmonic is the first carrier harmonic. This harmonic cancels between phase legs in the line-to-line output. Therefore, PD modulation places significant harmonic energy into a carrier component for each phase leg, and then relies on common-mode cancellation between the phase legs to eliminate this from the final line-to-line output voltage.

Phase Opposition Disposition Technique

Phase Opposition Disposition (POD), where the carriers above the sinusoidal reference zero are 180^0 out of phase with below zero point. The arrangement of carriers and modulating wave for POD is shown in Fig 5.

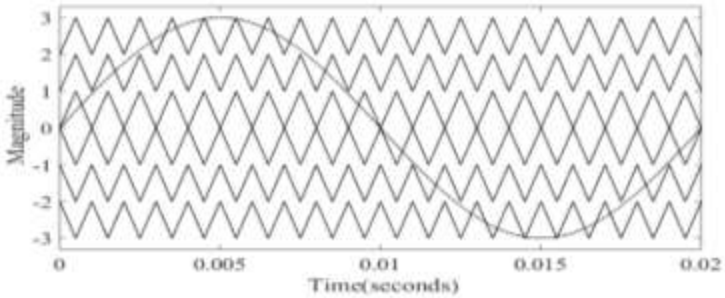

Fig 5 Reference and carrier waveforms for POD

The two outer carriers are used to generate the switching signals for one power cell, and the two inner carriers are used for the other. It can be clearly appreciated that the cell output voltages have completely different switching pattern, and that the power delivered by both cells is also uneven. This will, avoid the input current harmonics mitigation and produce undesirable distortion.

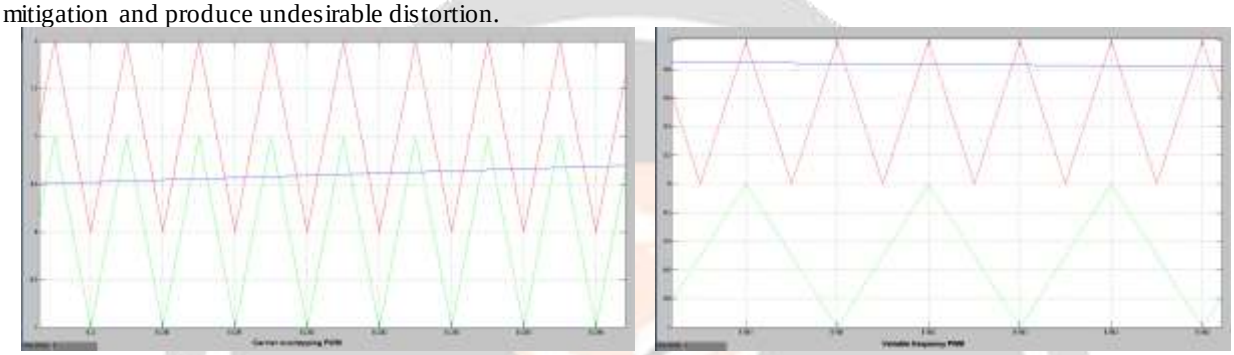

Fig.6 Carrier Overlapping PWM and Variable frequency PWM

Double-Frequency SPWM

The proposed topology can also work with double-frequency SPWM to achieve a higher equivalent switching frequency, as shown in Fig. 7. In the double-frequency SPWM, the five power switches are separated into two parts, and are modulated with two inverse sinusoidal waves respectively. S1, S2 , and S3 are modulated with *u*g1, while S4 and S5 are modulated with *u*g2. During the positive half grid cycle, the circuit rotates in the sequence of "state 4 – state 1 – state 2 – state 1," and the output voltage *v*AN varies between +*V*dc and the zero with twice of the carrier frequency. During the negative half grid cycle, the circuit rotates in the sequence of "state 4 – state 3 – state 2 –state 3," and the output voltage *v*AN varies between –*V*dc and zero.

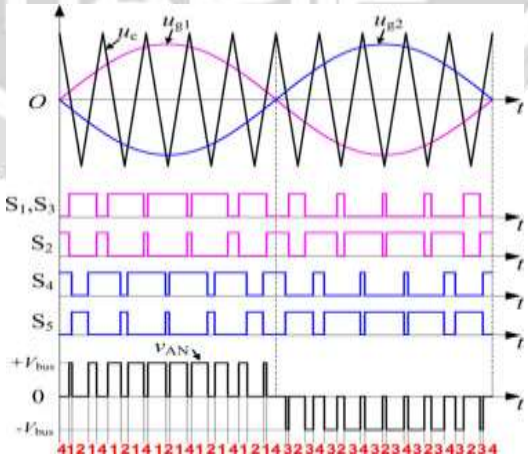

Fig. 7 Double Frequency SPWM

The aforementioned two modulation strategies both have their own advantages. The double-frequency SPWM can provide a higher equivalent switching frequency so that the size and weight of the filter inductor can be reduced. On the other hand, the unipolar SPWM can guarantee that the virtual dc bus *C*2 is charged by the real bus every switching cycle, so that the current stress on S1 and S3 caused by the operation of the switched capacitor can be

reduced. In this paper, the unipolar SPWM is chosen as an example for the performance evaluation and experimental verification. For all of the four operation states, there is no limitation on the direction of the output current *i*grid, since the power switches with antiparallel diodes can achieve bidirectional current flow. Therefore, the proposed topology has the capability of feeding reactive power into the grid to help support the stability of the power system.

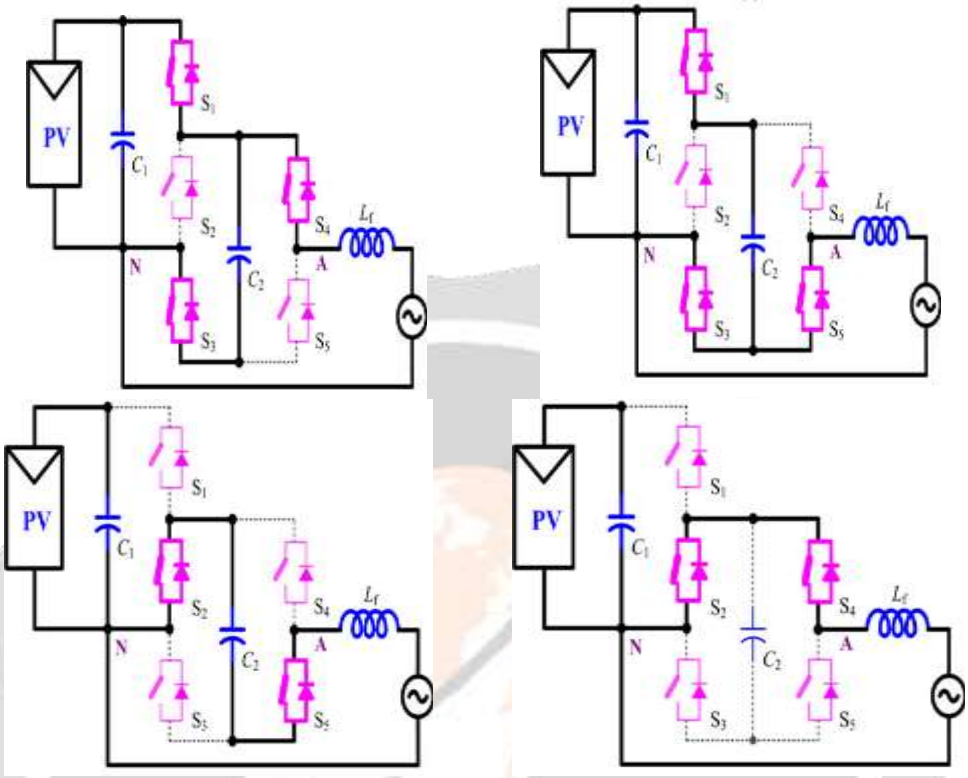

Fig.8: switching of proposed topology

The proposed topology is also immune against transient overvoltage of the grid. During the mains positive voltage spikes, the voltage at point A is clamped at *V*dc by *C*1 and the anti-parallel diodes of S1 and S4. Similarly, during the negative voltage spikes, the voltage at point A is clamped at −*V*dc by *C*2 and the anti-parallel diodes of S2 and S5. Therefore, the mains transient overvoltage does not pose a safety threat for the inverter.

4 SIMULATION RESULTS

A simulation design modulation technique as shown in Fig.9 & Fig.10 is implemented in MATLAB SIMULINK with the help of pulse generators where the Unipolar & Double polar frequency is varied. A modified circuit of the system ie a Unipolar and Double polar frequency Grid Tie inverter is also designed which is shown in Fig.9. The THD analysis is also compared for all the three simulations which is shown.

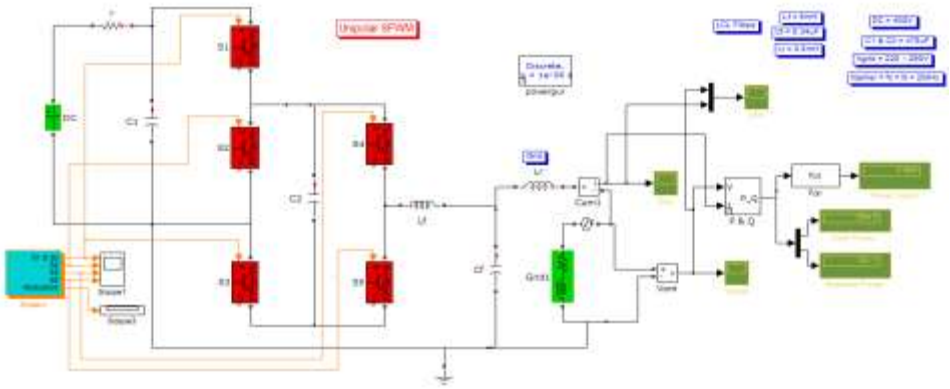

Fig.9. Proposed Unipolar Frequency Grid Tie Inverter

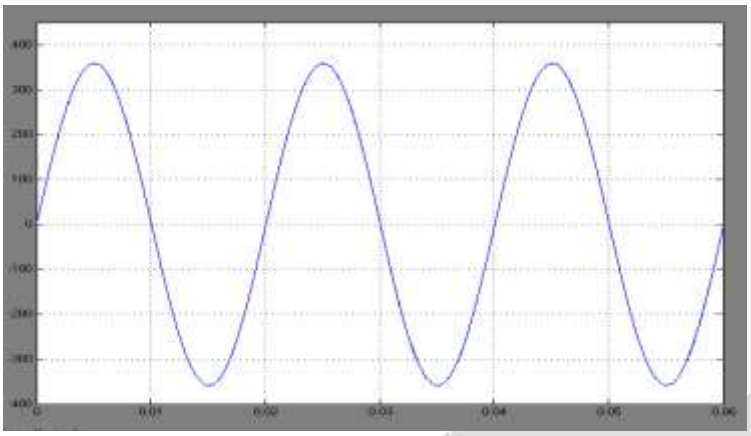

Fig.10. Output Voltage Waveform

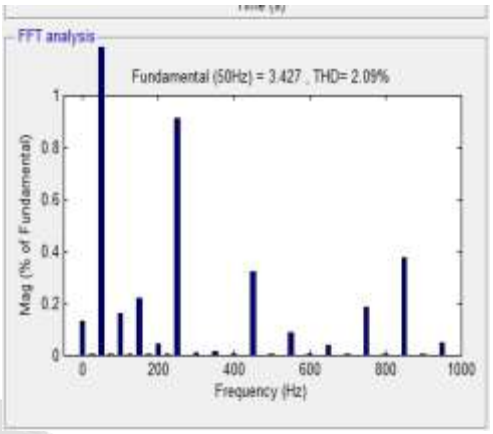

Fig.11. O/P Current Distortion

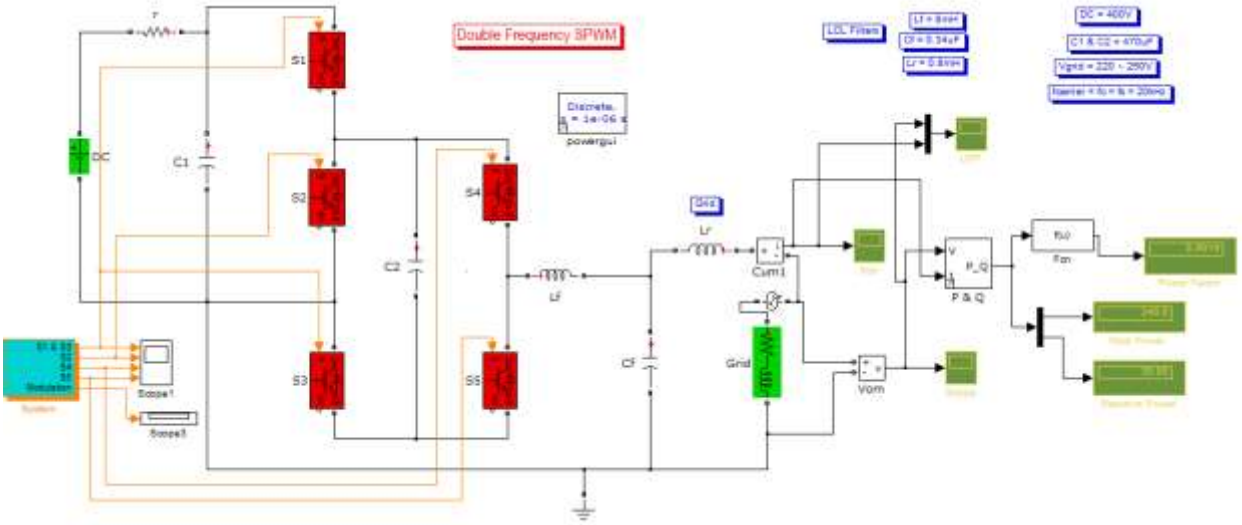

Fig.12. Proposed Double SPWM GTI

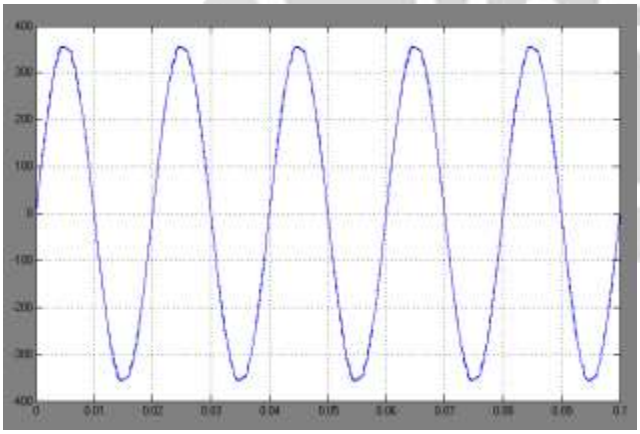

Fig.13. O/P Double SPWM Voltage Waveform

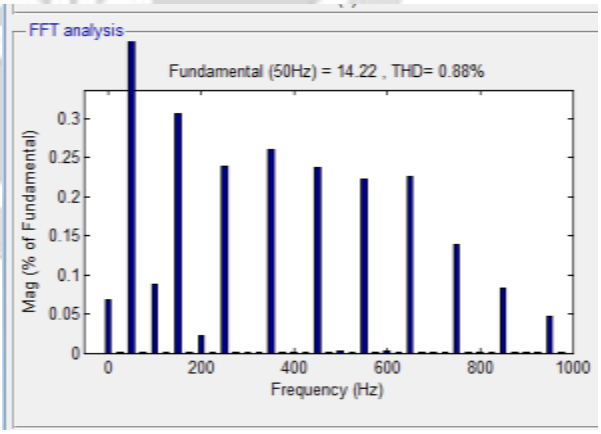

Fig.14. O/P Current Distortion

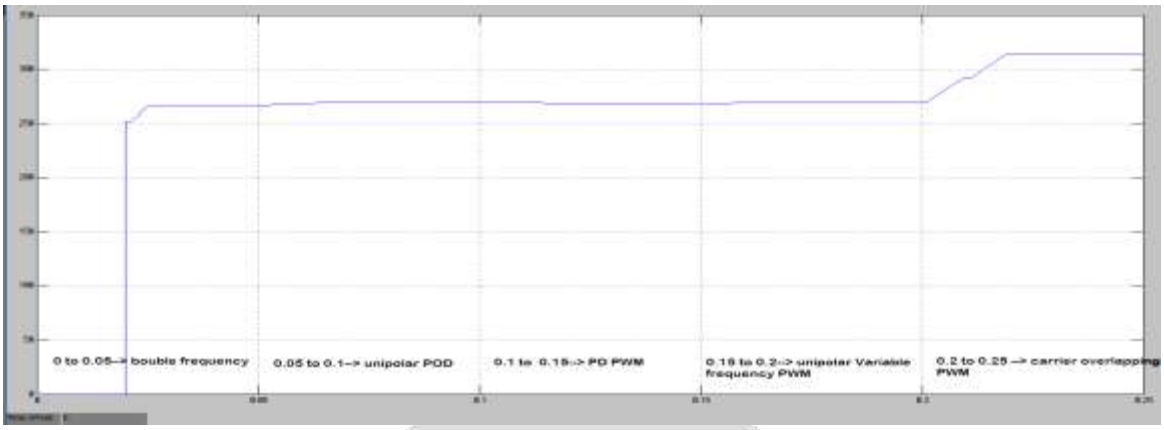

Fig.15 Output voltages when simulated using five types of PWM techniques

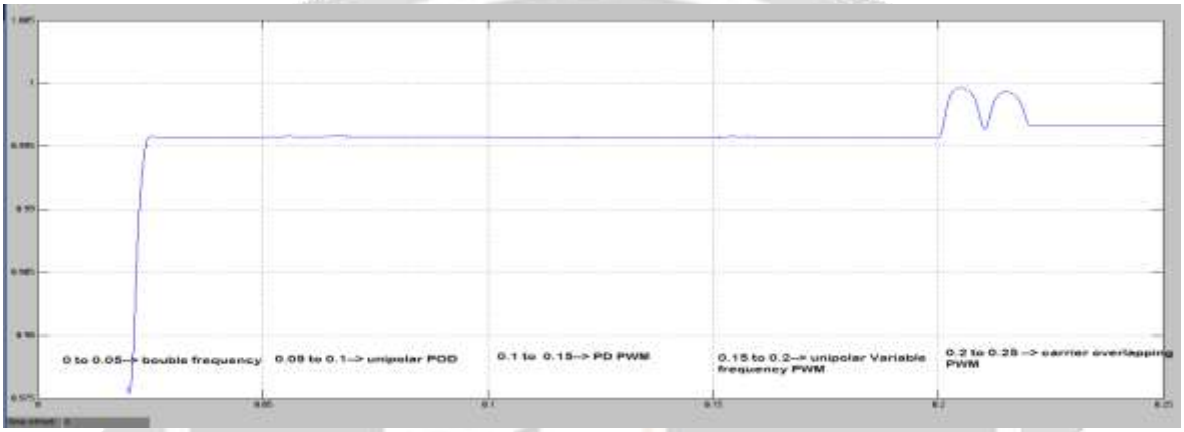

Fig.16 Power factor of network when simulated using five types of PWM techniques

5. CONCLUSIONS

Various PWM techniques for solar Inverter are investigated for performance analysis of the system interms of the output RMS voltage, total harmonic distortion, output current and common mode voltages are discussed in this paper. The concept of virtual bus has proposed in order to eliminate the common-mode (CM) leakage current in the transformerless photovoltaic (PV) systems. By connecting the grid neutral line directly to the negative pole of the dc bus, the stray capacitance between the PV panels and the ground is bypassed. As a result, the CM ground leakage current can be suppressed completely. Meanwhile, the virtual dc bus is created to provide the negative voltage level for the negative ac grid current generation. Consequently, the required dc bus voltage is still the same as that of the full-bridge inverter. Based on this concept, a novel transformerless inverter topology is derived. This topology is fed from solar, fuel cell and wind systems and modulation techniques such as PD, VFPWM and COPWM with the unipolar sinusoidal pulse width modulation and the double frequency SPWM were investigated to reduce the output current ripple using MATLAB/SIMULINK software

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