IMPLEMENTATION OF FPGA BASED SPWM CONTROLLER FOR SINGLE PHASE SOLAR INVERTER

Ramanantsihoarana H. Nathalie[1], Rastefano Elisée[2]

[1] *PhD Student, Dept. Embedded System, Instrumentation and Electronic System Modeling, Doctoral School of Science and Technics of Engineering and Innovation, University of Antananarivo, Madagascar*

[2] *Professor, Dept. Embedded System, Instrumentation and Electronic System Modeling, Doctoral School of Science and Technics of Engineering and Innovation, University of Antananarivo, Madagascar*

ABSTRACT

This paper presents the implementation of an efficient FPGA based SPWM control, for a single phase off-grid solar inverter. The principle and algorithm of SPWM is presented followed by the structure of the design of the SPWM. The proposed design is flexible allowing the change of the SPWM switching frequency and modulation index externally. The SPWM is intended to be implemented in a single chip FPGA, in order to reduce the complexity of the control of the inverter and reducing cost. The VHDL language is used to model the system and simulation is carried out using ModelSim 10.1c and Xilinx Vivado ISE Design Suite 14.7.

Keyword: *SPWM, FPGA, Single Phase Inverter , VHDL*

1. INTRODUCTION

Photovoltaic (PV) systems produce clean electrical energy since they can be dimensioned for a wide range of power ratings in both stand-alone and grid-connected applications. A typical PV system is composed by a PV array, a DC/DC converter to transform the power provided by the PV source and an inverter. The function of an inverter is to convert the DC voltage to a symmetric AC output voltage of desired magnitude frequency. The output voltage can be varied either by varying the DC input voltage or by controlling the gain of the inverter with Pulse Width Modulation (PWM). The Pulse Width Modulation (PWM) is a technique which is characterized by the generation of constant amplitude pulse by modulating the pulse duration by modulating the duty cycle. Analog PWM control requires the generation of both reference and carrier signals that are feed into the comparator and based on some logical output, the final output is generated. The reference signal is the desired signal output maybe sinusoidal or square wave, while the carrier signal is either a sawtooth or triangular wave at a frequency significantly greater than the reference.

The output voltage waveforms of ideal inverters should be sinusoidal, however the practical inverters will have non-sinusoïdal waveforms due to harmonics. Sinusoidal PWM (SPWM) is practically used in power conversion applications due to its simplicity in implementation. SPWM techniques are characterized by constant amplitude pulses with different duty cycle for each period. The width of these pulses are modulated to obtain inverter output voltage control and to reduce its harmonic content.

From the literatures, a comparison between DSP and FPGA based control capabilities for PWM power converters has been demonstrated and given that the FPGA based digital control is better than the DSP [1][2][3]. Most of the SPWM controllers are implemented with a host processor to perform arithmetic computations and an FPGA to generate PWM gating signals. The signal processing is a key issue in the performance of a digital system to achieve a single chip solution with reduced FPGA resource utilization.

The SPWM architecture proposed here minimize the use of host processor and reduce FPGA resource utilization.

2- PRINCIPLE AND ALGORITHM OF SPWM

2.1. Sinusoidal Pulse Width Modulation

The switches in the power source inverter (see Fig. 1) can be turned on and off as required. The sinusoidal pulse width modulation is widely used in power electronics to digitize the power so that a sequence of voltage pulses can be generated by the ON and OFF of the power switches. This technique reduces power loss, produce high accuracy of output waveform, and easy to implement.

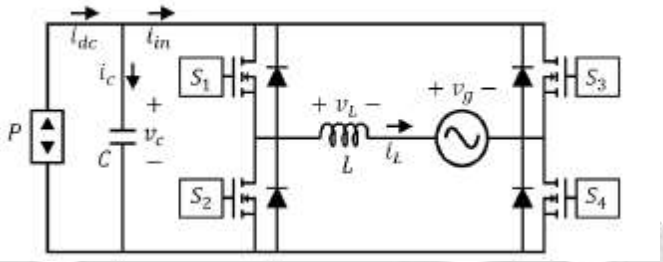

Fig-1: H-bridge inverter

In the most straightforward implementation, generation of the desired output voltage is achieved by comparing the desired reference waveform (modulating signal) with a high-frequency triangular 'carrier' wave as presented in Fig.2. Depending on whether the signal voltage is larger or smaller than the carrier waveform, either the positive or negative DC voltage is applied at the output. Over the period of one triangle wave, the average voltage applied to the load is proportional to the amplitude of the signal (assumed constant) during this period [4].

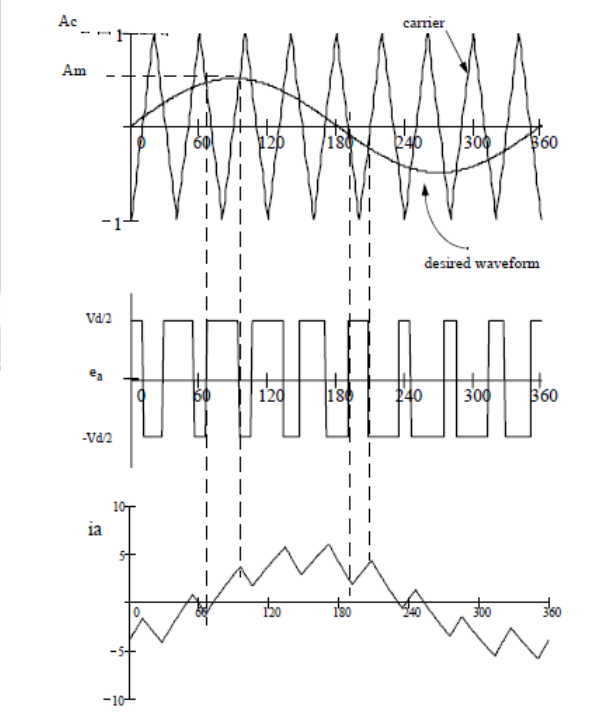

Fig -2: Principle of Sinusoidal Pulse Width Modulation

The resulting chopped square waveform contains a replica of the desired waveform in its low frequency components, with the higher frequency components being at frequencies of a close to the carrier frequency. The root

mean square value of the AC voltage waveform is still equal to the DC voltage, and the total harmonic distortion is not affected by the PWM process.
The harmonic components are merely shifted into the higher frequency range and are automatically filtered due to inductances in the ac system.

When the modulating signal is a sinusoid of amplitude Am, and the amplitude of the triangular carrier is Ac, the ratio M=Am/Ac is known as the modulation index. Note that controlling the modulation index therefore controls the amplitude of the applied output voltage. With a sufficiently high carrier frequency, see Fig. 3 drawn for fc/fm = 48 and t = L/R = T/3; T = period of fundamental, the high frequency components do not propagate significantly in the load due the presence of the inductive elements. However, a higher carrier frequency does result in a larger number of switching per cycle and hence in an increased power loss. Typically switching frequencies in the 2-15 kHz range are considered adequate for power systems applications.

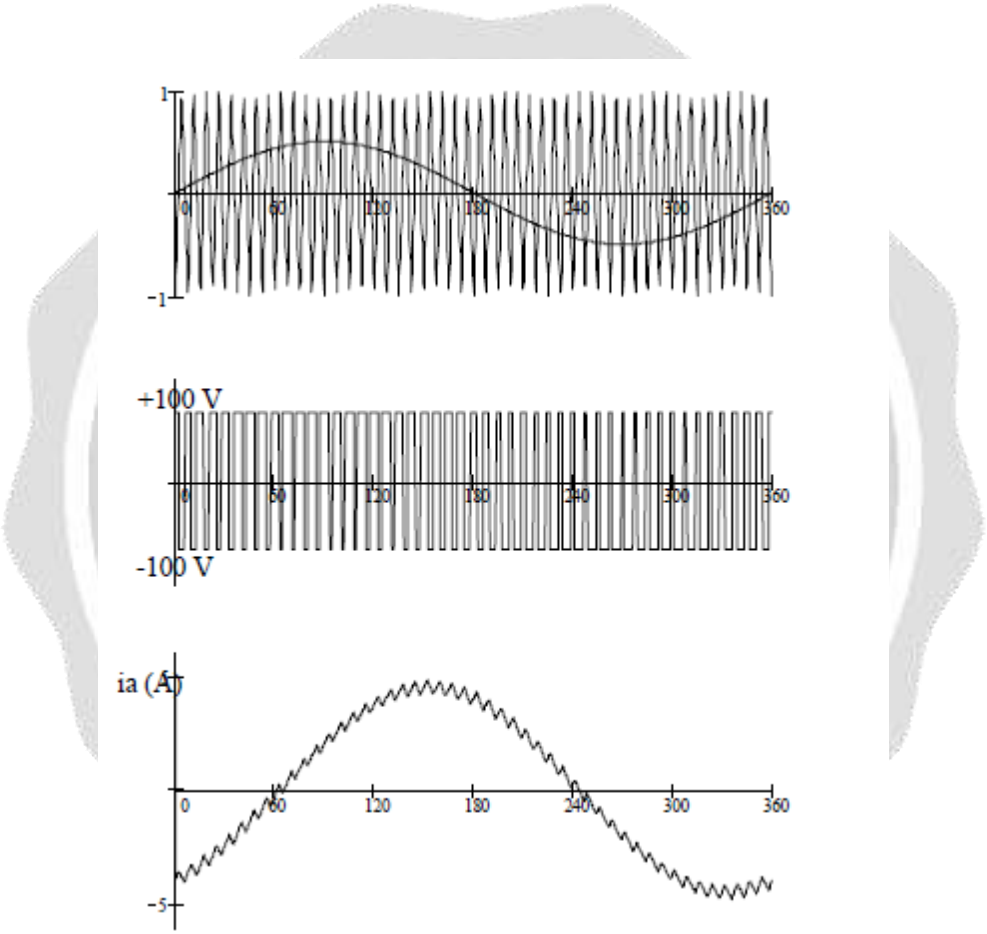

Fig-3: SPWM with fc/fm=48, L/R=T/3

The process works well for m ≤ 1 . For m>1 , there are periods of the triangle wave in which there is no intersection of the carrier and the signal as in Fig. 4. However, a certain amount of this "over modulation" is often allowed in the interest of obtaining a larger AC voltage magnitude even though the spectral content of the voltage is rendered somewhat poorer.

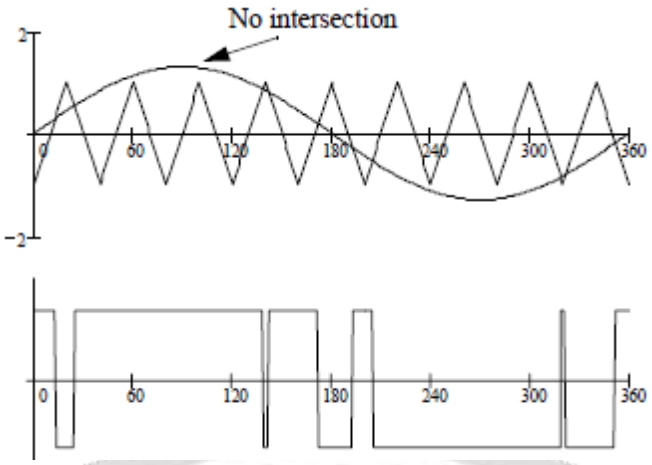

Fig -4: Over modulation m=1.3

2.2. Algorithm of SPWM

Step 1: Generate the sinusoidal signal reference using

$$V_{sin} = A_m sin\omega t \quad (1)$$

The frequency that the sine wave will be modulated can be calculated from the following formula [5]:

$$f(step) = \frac{step}{T_S * 2^n} \quad (2)$$

where, f(step) = desired frequency, T_S = the time period between each update i.e. the PWM period, n = the number of bits in the counter register and, step = the step size used.

Step 2: Generation of triangular carrier wave with desired fs.

Step 3: Comparator function of the sinusoidal and triangular waves, i.e. the intersections between the reference voltage and the carrying wave gives the time of opening and closing instants of the switches.

2.3. Switching strategy for single phase inverter

The unipolar operation of an H-bridge inverter is obtained forcing a leg to switch at high frequency while the other one switches at lower frequency. Also, it is possible to switch the high side switches of both legs at high frequency while the low side switches commute at lower frequency [5].

The power switches of the converter are set to the on or off state according to the result of the SPWM generator. The SPWM technique is used to adjust the inverter output voltage, amplitude and frequency to the desired value . In this technique the generated pulses are either positive or negative during each half period of the SPWM signal, V_{SPWM}.

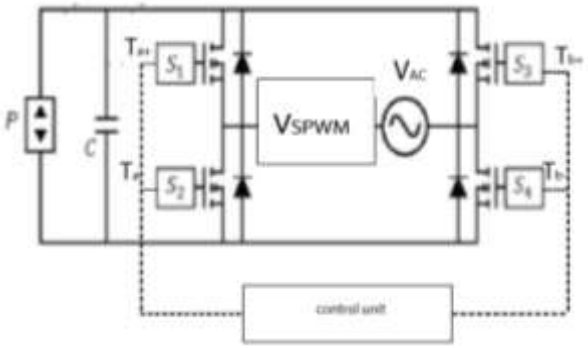

Fig-5: Switching strategy for single phase H-bridge inverter

3. IMPLEMENTATION OF THE SPWM CONTROLLER

The implementation of the SPWM controller is shown in Fig-5. The internal modules of the architecture consist of five modules. The system architecture is based on 8-bit fixed point arithmetic. Each module is described with VHDL for simulation and implementation.

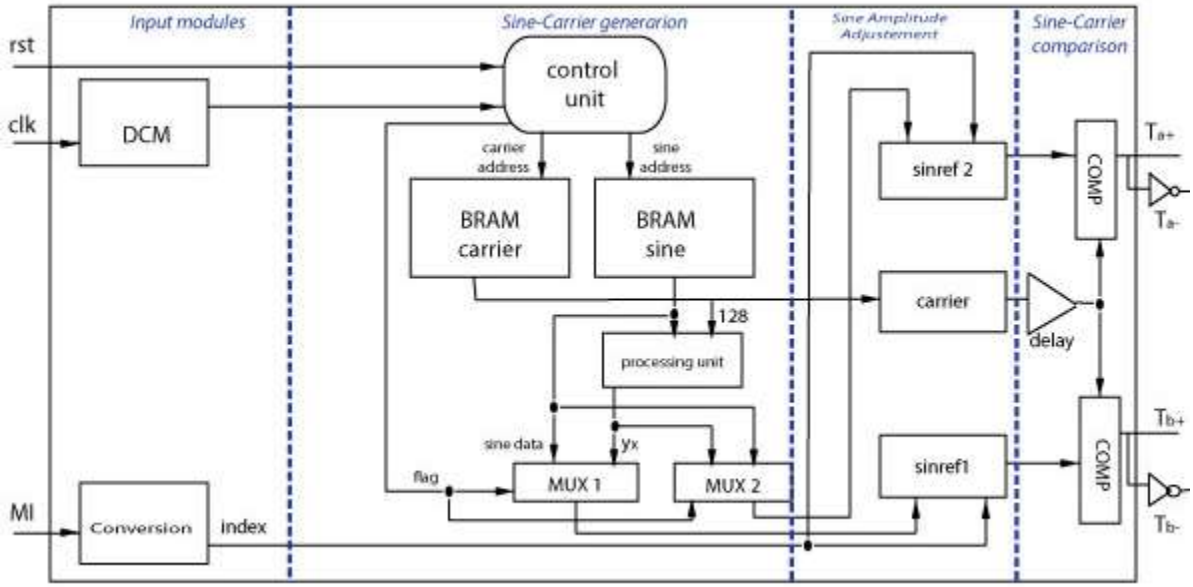

Fig -5: Block diagram of the hardware implementation of the SPWM controller

3.1. Digital Clock Manager

With the FPGA development board, a common clock of 10 MHz is provided by the oscillator. But, the operation speed or clock for each module in the design is varying. Therefore clock generator, takes as input the FPGA's clock and produces a new one that allows the whole system to operate in the desired switching frequency. This clock generator consists of a Digital Clock Manager (DCM).The DCM plays the role of exactly adapting the external clock to the desired switching frequency by either increasing or decreasing the corresponding FPGA clock frequency.

3.2. Modulation index

The input of the system is the modulation index in single precision floating point arithmetic, while the system architecture is based on 8-bit fixed point arithmetic. The modulation index (MI) is taken as input which ranges from 0 to 1. This value is converted to fixed point arithmetic. Assuming there is an n-bit wide architecture, the equation to convert a floating point value to a given fixed-point architecture is given by (3).

$$Y_M = M * (2^{n-1}) + (2^{n-1}) \quad (3)$$

3.3. Sine-Carrier Module

The third module consists of the control unit, two BRAMs, which contain the sinusoidal and the triangular values, respectively and two multiplexers which produce the two reference sine-waves either on a positive, or a negative cycle.
Block RAM (BRAM) is internal storage which is embedded inside the chip of FPGA for potential application like local storage, buffers, stack. BRAM offers advantages over off-chip memory, such as reducing the number of chips required to implement the system , faster clock rate as external pins and PCB tracks are not needed to access memory, saving of pins of the chip as no external address or data bus is required.
In order to minimize the FPGA resource utilization, the memories were organized as follows; both the sinusoidal and the triangular pulses were sampled and quantized with the same sampling frequency, in order to produce the discrete values used for the BRAMs initialization over the corresponding sampling period. The sinusoidal memory contains the values of the first quarter of the sine-wave period. The values of the sine-wave in the other three quarters are calculated by mirroring and inverting the values of the first quarter. The carrier memory contains the values of one period of the triangular wave.

The sine-wave and the carrier BRAMs operate as lookup tables (LUTs). A LUT is a set of memory locations which contains some precalculated value. The memory locations of a sine LUT store binary value which are calculated using the following relation at different angle *ω*:

$$LUT(n) = A * \sin \omega \qquad (4)$$

where n is memory word length used for LUT . The angular resolution Δωfor an LUT with memory words equal to L is given by :

$$\Delta\omega = \omega(i) - \omega(i-1) = \frac{2\pi}{L} \qquad (5)$$

where i varies from 0 to L-1. When input clock frequency is fixed, varying L produces sinusoid of different frequency. Angle ω at any sample instance can be expressed as:

$$\omega(i) = \Delta\omega * i \qquad (6)$$

Substituting ω(i) in (4), we get :

$$LUT\ (n) = A * \sin\frac{2\pi}{L} * i \qquad (7)$$

The resolution can be varied by changing L. The amplitude of output waveform depends on'A'.

The control unit also produces a flag signal, which is responsible for the retrieval of the sine wave values on a negative cycle. The sinusoidal-wave BRAM is scanned up and down four times, since this memory contains only the first quarter of a sinusoidal period. Memory up/down counting determines the value of the flag signal. When the flag is set to 0, the multiplexer outputs the data read from the sinusoidal memory (Sine Data). Otherwise, the multiplexer outputs the sinusoidal values on the negative cycle that correspond to the values read from the memory after processing [Negative Value (y)]. The conversion of the positive values stored in the sinusoidal memory to the corresponding negative values is performed according to the following equation:

$$Y_x = X - [(X - 2^{n-1}) * 2] \qquad (8)$$

Where X is the positive value stored and n is the digital word length (n=8 in the proposed architecture). The second multiplexer is used for the production of the second reference Sine-wave operating exactly on the opposite mode from the one analyzed above.

3.4. Sinusoid Reference Generator Module

This module outputs the two reference sinusoidal and triangular values (SineRef1, SineRef2 and CarrierData), respectively, synchronized in every clock cycle over a sinusoidal sampling period. The adjustable amplitude sine

subsystem, takes as input the reference sinusoidal values [”SineRef (y)”] produced by the subsystems described above and generates a sinusoidal digital signal [”sineAdjustable (x)”], with amplitude adjustable according to the modulation index value, which is also input of this subsystem.

The phase legs of the inverter have to be protected from short circuit. Therefore, a programmable delay-time is introduced in the designed SPWM architecture. The turn-off time of power devices is usually longer than its turn-on time, and, therefore, an appropriate delay time must be inserted between these two gating signals. The length of this delay time is usually about 1.5 to 2 times the maximum turn-off time.

3.5. Comparator Module

The comparison subsystems implement the comparison between the high frequency, constant-amplitude triangular wave, the carrier-wave, with the two low-frequency reference sine-waves of adjustable amplitude, using a simple comparator. The control signals Ta+ and Tb+ of the H-bridge inverter power switches, comprising the SPWM pattern, are generated from the outputs of the corresponding comparators. The output of each comparator is equal to one when the output of the corresponding adjustable amplitude sine subsystem is equal to or greater than the digital value of the carrier signal. Moreover, the inverted SPWM pulses are generated in order to control the inverter power switches Ta- and Tb-.

4. SIMULATION AND DISCUSSION

All the modules are modeled using VHDL in Xilinx Vivado ISE Design Suite 14.7 and the simulation of the design is performed using Modelsim SE to verify the functionality of the design.

4.1. Input waveform

The input of the SPWM generator is the FPGA input clock and produces a new clock signal used by the digital circuits of the proposed SPWM generator, such that the desired SPWM switching frequency F_c is generated. The Digital Clock Manager module adapts the frequency to the desired value. The simulation of clock generator result is shown in Fig-7.

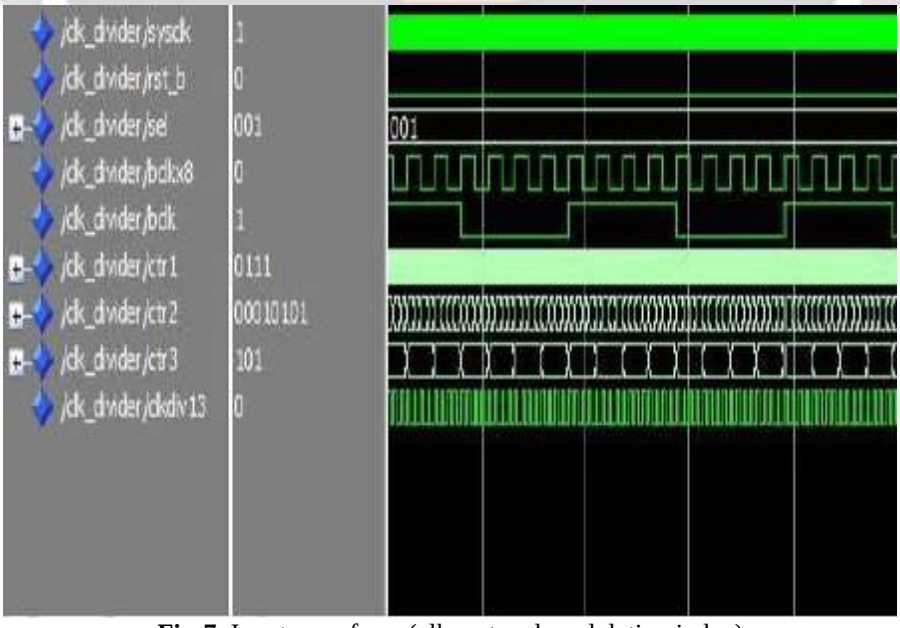

Fig-7: Input waveform (clk , rst and modulation index)

4.2. SPWM output

The SPWM output is generated at the intersection of the sinusoidal and triangular waveforms at certain sampling instants. When the value of each sine-wave is higher than the triangular wave value, the output pulse is set to logical 1, else it is set to logical 0. The Comparison subsystem implements the comparison between the high-frequency constant-amplitude triangular wave (carrier) with the two low-frequency reference sine waves, using two comparators. The control signals s1, s2, s3, and s4 of the single phase inverter power switches are generated from the outputs of the corresponding comparators of this subsystem, thus forming the SPWM wave at the inverter output terminals. The H-bridge inverter control signals S2 and S4 are produced by inverting S1 and S3, respectively.

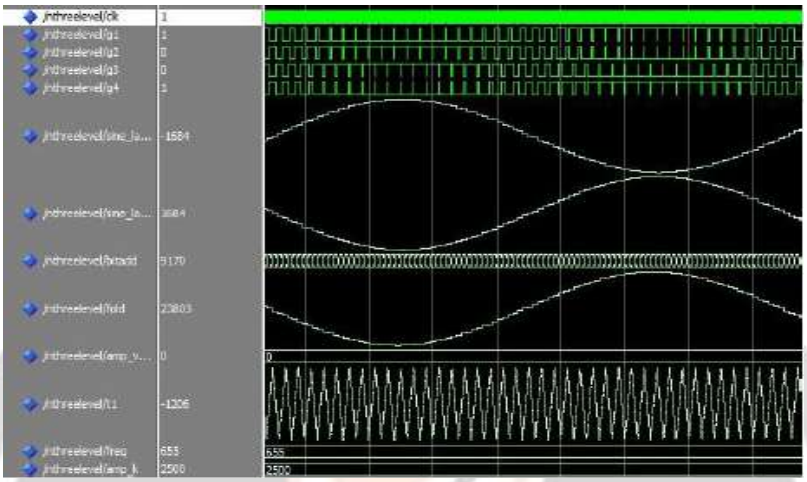

Fig-8: SPWM output waveform

4. CONCLUSION

The single phase SPWM FPGA-based controller for solar inverter is developed. All the modules in the SPWM architecture are designed with VHDL. The developed SPWM is suitable for single chip FPGA implementation for inverter control algorithm. SPWM technique offers multiple advantages, such as low power loss, high accuracy of output waveform. In addition the proposed architecture presented here is easy to implement and reduce the use of host processor and FPGA resource.

5. REFERENCES

[1] L. Mihalache. "DSP Control Method of Single -Phase Inverters for UPS Applications ". IEEE Trans. On Industry Application. 2002, pp 590-595.

[2 M.N.Md Isa et al "FPGA Based SPWM Bridge Inverter Published in American journal of Applied Sciences, page 584-586,2007

[3] R.K. Pongiannan, P. Selvabharathi, N. Yadaiah, "FPGA based three-phase sinusoidal PWM VVVF controller", 1st International Conference on Electrical Energy Systems, pp. 34-39, 2011.

[4] Matina Lakka, Eftichios Koutroulis, Apostolos Dollas , "An FPGA-based SPWM Generator for High-Frequency DC/AC Inverters", 2nd Pan-Hellenic Conference on Electronics and Telecommunications - PACET´12, March 16-18, 2012.

[5] Muhammad, H. Rashid. Power Electronics Circuits, Devices andApplication. Upper Saddle River, NJ: Prentice Hall, 2004.