MITIGATION OF VOLTAGE SAG/SWELL UISNG MODIFIED DVR

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ABSTRACT

This paper deals with improving the voltage quality of sensitive loads from voltage sags using a dynamic voltage restorer (DVR). The higher active power requirement associated with voltage phase jump compensation has caused a substantial rise in size and cost of the dc link energy storage system of DVR. The existing control strategies either mitigate the phase jump or improve the utilization of dc link energy by the following: 1) reducing the amplitude of the injected voltage or 2) optimizing the dc bus energy support. In this paper, an enhanced sag compensation strategy is proposed, which mitigates the phase jump in the load voltage while improving the overall sag compensation time. An analytical study shows that the proposed method significantly increases the DVR sag support time (more than 50%) compared with the existing phase jump compensation methods. This enhancement can also be seen as a considerable reduction in dc link capacitor size for new installation. The performance of the proposed method is evaluated using simulation for five-level inverter instead of two-level in DVR. The Simulation results more efficient incase of Five-level DVR is shown.

Keyword: - *Power Quality, FACT Controllers, DVR*

1. INTRODUCTION

The fulfillments of the industrial goals were possible only because the modern industries were able to find innovative technologies that have successfully become technological developments. Continuous production throughout the period is ensured only when the final objective is to optimize the production while achieving maximum profits and achieving minimized production costs. The reason for demanding high quality un-interruptible power during production process is mainly because of the modern manufacturing and process equipments that operate at high efficiency requires stable and defect free power supply for the successful operation of their machines. Machines, sensitive to power supply variations are to be designed more precisely. For instance, some instruments like adjustable speed drives, automation devices, power electronic components etc. fall into the above category. Cessation to provide the required quality power output may sometimes cause complete shutdown of the industries which will make a significant financial loss to the industry concerned. However blame due to degraded quality cannot be simply put on to the hands of the utility itself. It has been observed that in industries, most of the conditions that can disrupt the process are generated within the industry itself. For example, most of the non-linear loads cause transients which can affect the reliability of the power supply. Following mentioned are some aberrant electrical conditions that can disrupt a process caused both at the utility and the customer end.

Manufacturing cost and the reliability of those solid state devices have been improved as new technologies emerged. So, the protection devices which include such solid state devices can be purchased at a reasonable price with superior performance than the conventional electrical or pneumatic devices available in the market. Uninterruptible Power Supplies (UPS), Dynamic Voltage Restorers (DVR) and Active Power Filters (APF) are examples for commonly used custom power devices. Among those APF is used to mitigate harmonic problems occurring due to non-linear loading conditions, whereas UPS and DVR are used to compensate for voltage sag and surge conditions. Voltage sag may occur from single phase to three phases. But it has been found that single phase voltage sags are routine and most frequent in the power industry. Thus, the industries that use single and three phase supply will undergo several interruptions during their production process and they are forced to use some form of voltage compensation equipment.

As soon as the fault occurs the action of DVR starts. On event of fault which results in voltage sag, the magnitude reduction is accompanied by phase angle shift and the remaining voltage magnitude with respective phase angle shift is provided by the DVR. Employing minimum active voltage injection mode in the DVR with some phase angle shift in the post fault voltage can result in miraculous use of DVR. If active voltage is less prominent in DVR then it can be delivered to the load for maintaining stability. Considering this, a transition process is proposed such that voltage restoration is achieved by injecting the voltage difference between the pre sag and the in sag (source side) voltages during the initial first cycle or so the sag. When the sag voltage phasor is available, the injection voltage is controlled to move progressively from the in phase injection point to the corresponding minimum active voltage injection point. The initial voltage injection magnitude and phase angle of DVR can be categorized into different cases considering the injection limit that will be discussed further.

The simulation of various 1 phase and 3 phase faults are done using MATLAB. The present project deals with only voltage sag, voltage swell can be simulated in same way. The simulation results show the very good performance of the controller theoretically. The performance of DVR theoretically is tested. Therefore this project has contributed a strong knowledge to the research and development targeting industrial application to compensate the single-phase voltage sags and 3 phase balanced voltage sags.

2. PROPOSED TECHNIQUE

Generally voltage sag can be very expensive and cause severe problems for the customers as it may lead to production damage and downtime. By using power electronics devices also known as customer power device a certain amount of voltage and power can be injected into the distribution system and this severe problem of voltage sag can be minimized. Out of the various approaches that have been have been proposed to limit the cost causes by voltage sag, dynamic voltage restorer (DVR) is one of the best methods to address voltage sag problems. This method is briefly discussed in our thesis and it can be used to correct voltage sag at distribution level.

2.1 PRINCIPLES OF DVR OPERATION

A DVR is a solid state power electronics switching device which comprises of either GTO or IGBT, a capacitor bank as energy storage device and injection transformers. From the figure it can be seen that DVR is connected in between the distribution system and the load. The basic idea of DVR is that by means of an injecting transformer a control voltage is generated by a forced commuted convertor which is in series to the bus voltage. A regulated DC voltage source is provided by a DC capacitor bank which acts an energy storage device.

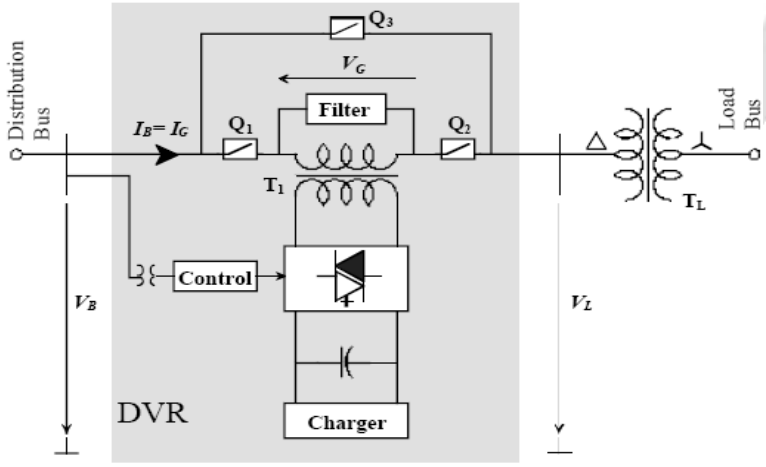

Fig-1: Principle of DVR with a Response Time of Less Than One Millisecond

Under normal operating conditions when there is no voltage sags, DVR provides very less magnitude of voltage to compensate for the voltage drop of transformer and device losses. But when there is a voltage sag in distribution system, DVR will generate a required controlled voltage of high magnitude and desired phase angle which ensures that load voltage is uninterrupted and is maintained. In this case the capacitor will be discharged to keep the load supply constant. [3] Note that the DVR capable of generating or absorbing reactive power but the reactive power

injection of the device must be provided by an external energy source or energy storage system. The response time of DVD is very short and is limited by the power electronics devices and the voltage sag detection time. The expected response time is about 25 milliseconds, and which is much less than some of the traditional methods of voltage correction such as tap-changing transformers.

2.2 CONSTRUCTION OF DVR

Power circuit and the control circuit are the 2 main parts of the DVR. There are various critical parameters of control signals such as magnitude, phase shift, frequency etc. which are injected by DVR. These parameters are derived by the control circuit. This injected voltage is generated by the switches in the power circuit based on the control signals. Furthermore the basic structure of DVR is described by the power circuit and is discussed in this section. The 5 main important parts of power circuit, their function and requirements are discussed ahead.

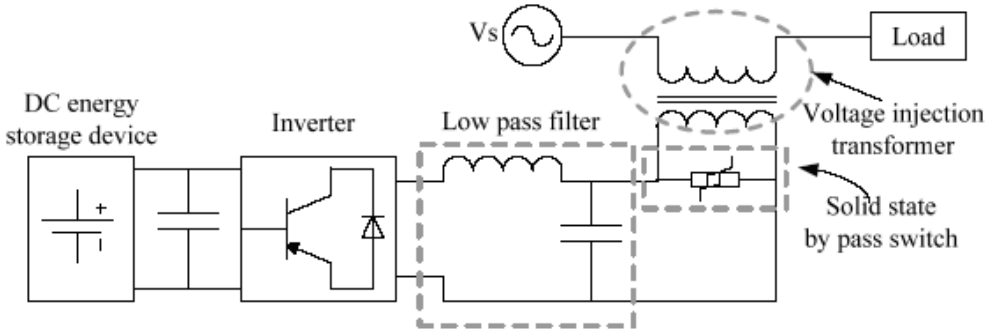

Fig-2: DVR Power Circuit [20]

2.2.1 ENERGY STORAGE UNIT

Various devices such as Flywheels, Lead acid batteries, Superconducting Magnetic energy storage (SMES) and Super-Capacitors can be used as energy storage devices. The main function of these energy storage units is to provide the desired real power during voltage sag. The amount of active power generated by the energy storage device is a key factor, as it decides the compensation ability of DVR. Among all others, lead batteries are popular because of their high response during charging and discharging But the discharge rate is dependent on the chemical reaction rate of the battery so that the available energy inside the battery is determined by its discharge rate.

2.2.2 Voltage Source Inverter

Generally Pulse-Width Modulated Voltage Source Inverter (PWMVSI) is used. In the previous section we saw that an energy storage device generates a DC voltage. To convert this DC voltage into an AC voltage a Voltage Source Inverter is used. In order to boost the magnitude of voltage during sag, in DVR power circuit a step up voltage injection transformer is used. Thus a VSI with a low voltage rating is sufficient.

2.2.3 Passive Filters

To convert the PWM inverted pulse waveform into a sinusoidal waveform, low pass passive filters are used. In order to achieve this it is necessary to eliminate the higher order harmonic components during DC to AC conversion in Voltage Source Inverter which will also distort the compensated output voltage. These filters which play a vital role can be placed either on high voltage side i.e. load side or on low voltage side i.e. inverter side of the injection transformers. We can avoid higher order harmonics from passing through the voltage transformer by placing the filters in the inverter side. Thus it also reduces the stress on the injection transformer. One of the problems which arise when placing the filter in the inverter side is that there might be a phase shift and voltage drop in the inverted output. So this could be resolved by placing the filter in the load side. But this would allow higher order harmonic currents to penetrate to the secondary side of the transformer, so transformer with higher rating is essential

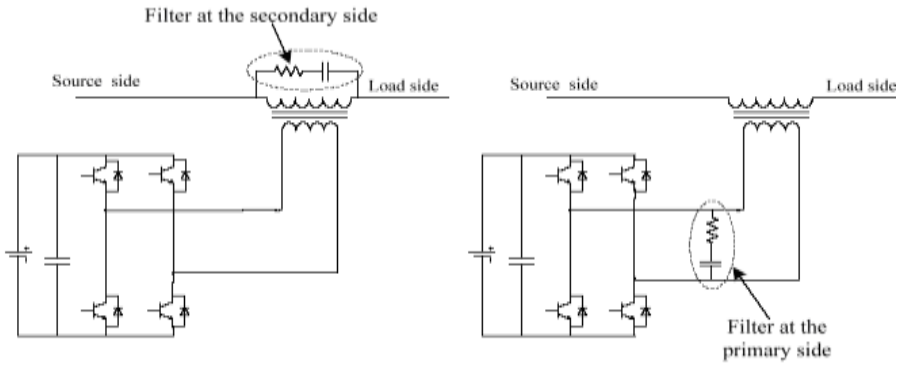

Fig-3: Different Filter Placements [18]

.3. ANALYSIS AND DESIGN OF PROPOSED WORK

In this paper proposes enhanced sag compensation method to extend the DVR compensation time. It optimizes the gradient of the dc link voltage (*dvdc/dt*) by regulating the amount of active power injected by DVR. In the proposed method, the controller restores both phase and amplitude of the load voltage to the Presag value and then initiates a transition toward the minimum active power (MAP) mode. The overall operation sequence and implementation of the proposed compensation method is discussed in the following subsections

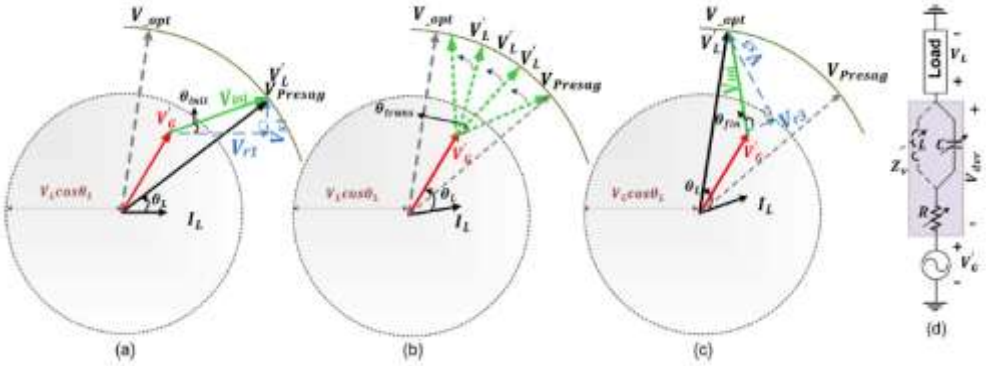

Fig-4: Phasor diagram for the proposed sag compensation method. (a) Presag restoration, (b) intermediate transition, (c) final load voltage with MAP injection, and (d) DVR visualization as the variable virtual impedance changes from resistive to dominant capacitive (for sag) or inductive (for swell).

A. Phase Jump Detection and Presag Restoration

For detecting the phase jump, two PLLs are employed (one over the load voltage and another over the source voltage), giving θVL and θVg, respectively. As soon as the sag is detected, the first step is to determine the DVR initial injection angle that avoids the phase jump at the load side. This is done by freezing the load voltage PLL that gives the presag angle (θVLp). On the other hand, the unrestricted grid voltage PLL gives the grid voltage phase (θVg). The difference between these two angles gives the initial angle of injection

$$\left.\begin{aligned}\theta_{\text{init}} &= \theta_L + (\theta_{VLp} - \theta_{Vg}) \\ &= \theta_L + \delta\end{aligned}\right\}. \qquad \text{..... 6.1}$$

Note that, in the steady state, both angles will be identical, and thus, the difference will be zero. For sag detection, the absolute difference between the reference load voltage (1 p.u.) and the actual grid voltage (p.u.) in synchronous reference frame is calculated as follows [7], [19]–[22]:

$$\Delta V_{\text{sag}} = \left|1 - \sqrt{V_{gd}^2 + V_{gq}^2}\right|. \quad \text{..... 6.2}$$

As soon as $\Delta V\text{sag} > 0.1$, it is recognized as a voltage sag [23].

B. ***Controlled Transition toward the MAP Mode***

Once the presag voltage is successfully restored, after one cycle, a smooth transition toward the MAP mode is initiated and completed over the next one to two cycles. The final injection angle of DVR (θfin) is given as

$$\theta_{\text{fin}} = \begin{cases} \frac{\pi}{2} + \gamma, & \text{if } \Delta V_{\text{sag}} \le (1 - \cos\theta_L) \\ \pi - \tan^{-1}\left(\frac{V_L(\sin\theta_L)}{V_L\cos\theta_L - V_g'}\right), & \text{if } \Delta V_{\text{sag}} > (1 - \cos\theta_L) \end{cases}. \quad \text{..... 6.3}$$

A detailed derivation of (18) is given in Appendix C. The first part of (18) represents the self-supporting mode of operation in which the DVR absorbs active power (relatively very small amount) from the grid to overcome the system losses and thus maintains a constant voltage across the dc link capacitor. The term γ indicates the reduction in θfin due to loss component and is determined by the dc link (PI) controller. The second part of

(18) represents a case where the self-supported dc link cannot be maintained due the constraint in (5). To ensure a smooth changeover, a transition ramp is defined between the initial and final operating points, as given in the following:

$$\theta_{\text{trans}} = \theta_{\text{init}} + \frac{\theta_{\text{fin}} - \theta_{\text{init}}}{\Delta T}(t) \quad \text{..... 6.4}$$

where ΔT determines the slope of the transition curve and is chosen as 30 ms.

C. Iterative Decrement in Injection Angle

In self-supporting mode, the DVR can compensate the sag for an indefinitely long time. However, for deeper sag depths, there is certain nonzero active power injected by DVR. This causes a reduction in the energy stored in the dc link capacitor, and consequently, its voltage reduces (gradually). To maintain the required voltage at the inverter output side, the controller increases the modulation index *mi* until it reaches *mi*−max. This is the limiting case as explained by (12), beyond which the controller goes into over modulation and cannot maintain the rated load voltage. To avoid this over modulation condition, an iterative control loop is used, which constantly monitors the dc link voltage and decreases θfin in (18) to keep $V\text{dc} > V\text{dc}-\text{min}$ and is given as

$$\theta_{\text{fin}} = \theta_{\text{fin}} - \epsilon \quad \text{..... 6.5}$$

where _ is chosen as 0.01 rad.

D. Operation Sequence

Fig. 5.2(a)–(c) depicts the overall operation sequence of the proposed phase jump compensation scheme. The transition from high active power mode (presag) to MAP mode is shown in three steps. The illustration is for the case where the sag depth is more than the limit in (5) and there is a positive phase jump associated with the sag. As discussed previously and shown in Fig. 5(a), DVR initiates the compensation by supplying high active power to the load ($Vr1$ _ $Vx1$) and restores both magnitude and phase of the load voltage to presag values. After one cycle, the transition toward the MAP mode is initiated, and DVR gradually increases the contribution of reactive power. As seen from Fig. 5(b) and (c), the injected voltage magnitude and its phase angle are gradually increasing until V_L reaches $VL-\text{opt}$. Note that at the final operating point $Vr1$ _ $Vx1$. The aforementioned DVR operation can be viewed as an equivalent variable impedance Zv where the operation begins with dominant resistive impedance $Zv = R$ (high active power) and completes as dominant capacitive impedance $Zv \approx XC$ (high reactive power).

5.2 ANALYTICAL STUDY ON COMPENSATION TIME WITH DIFFERENT APPROACHES

In this section, a comparative study is presented to determine the maximum compensation time achieved using the aforementioned phase jump compensation methods. These include the following: 1) the Presag; 2) the method given in [16], named as Presag–in-phase in this paper; and 3) the proposed method. Table I shows the various design parameters used for the comparison. The maximum compensation time of 200 ms(10 cycles) with a phase jump of +45◦ is taken as reference. Using (15), the value of the dc link capacitor is obtained as 9000 μF.

The sag depth is varied over a range of values from 10% to 80% of nominal grid voltage, keeping the power factor and phase jump fixed at 0.7 lagging and +45◦, respectively. Analytically computed DVR-injected magnitude and maximum compensation times are provided in Fig. 5.4. Note that the DVR voltage magnitudes are shown after the first one cycle of compensation as all of the three methods perform identically for the first cycle. As seen from Fig. 5.4 both the presag and proposed methods have the same *V*DVR magnitude for a sag depth greater than the limit in (6), i.e., 30%. However, as noticed from Fig. 5.5, *tc*−max is highest for the proposed method for all values of sag depths. For the designed range of 50% sag depth, it can be seen that the presag–in-phase method improves the compensation time from 10 to 16 cycles over the presag method. The proposed method further improves it to 22 cycles. Moreover, for the sag depth lower than 30%, the proposed method can withstand any sag duration by operating in the self-supporting mode. The significant improvement in the compensation time is due to the least possible utilization of dc link active power, thus resulting in the slowest discharging of the dc link capacitor. Note that the proposed method does not result in higher injection voltage magnitude than the design limit of 0.7 p.u., which is clear in Fig.5.6. Fig. 5.8 depicts the scenario where the phase jump is varied from −90◦ to +90◦ for a sag depth of 0.5 p.u. and other boundary conditions from Table I. As seen from the graph, the maximum compensation time is highest for the proposed method. It can also be noted that the presag method becomes unable to correct the phase jump beyond −60◦ and +60◦ due to violation of (12).

5.3. OVERALL DVR SYSTEM CONTROL SCHEME

Fig. 5.6 depicts the detailed block diagram of the proposed phase jump compensation method. A logic unit is employed to constantly monitor the grid voltage for sag detection using (17). To obtain the reference load voltage, the control system is divided into two sub modules: 1) phase jump detection plus DVR injection angle calculation and (2) MAP injection. To achieve a decoupled active and reactive power control, the phase of the line current is considered as the reference and is obtained by the PLL.

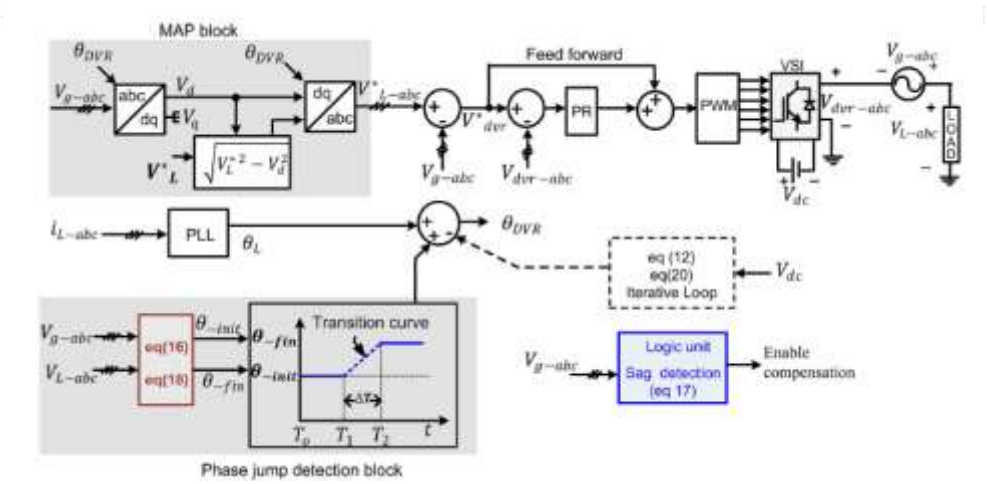

Fig-5: Detailed block diagram of the proposed phase jump compensation method with MAP injection.

The phase jump detection block computes the DVR initial (presag injection) angle and final (MAP injection) angle. Once the transition is over, the MAP block gives the reference voltage $V_{L-abc} = V_{opt}$.

As shown in Fig. 5.6, the obtained DVR reference voltage *V* dvr is compared with the actual voltage in the stationary reference frame. A proportional-resonant (PR) controller with a large gain at the grid fundamental frequency is used for accurate tracking of *V*dvr. To compensate for DVR system losses, *V*dvr is added as a feed forward signal to the output of the PR controller. The dc link voltage is constantly monitored in an iterative control loop to regulate the injected voltage angle, thus avoiding over modulation. Note that this block is only required when the sag depth is close to the system design limit.

4 SIMULATION RESULTS

The simulation of proposed system is shown in figures from fig.6 to fig.13

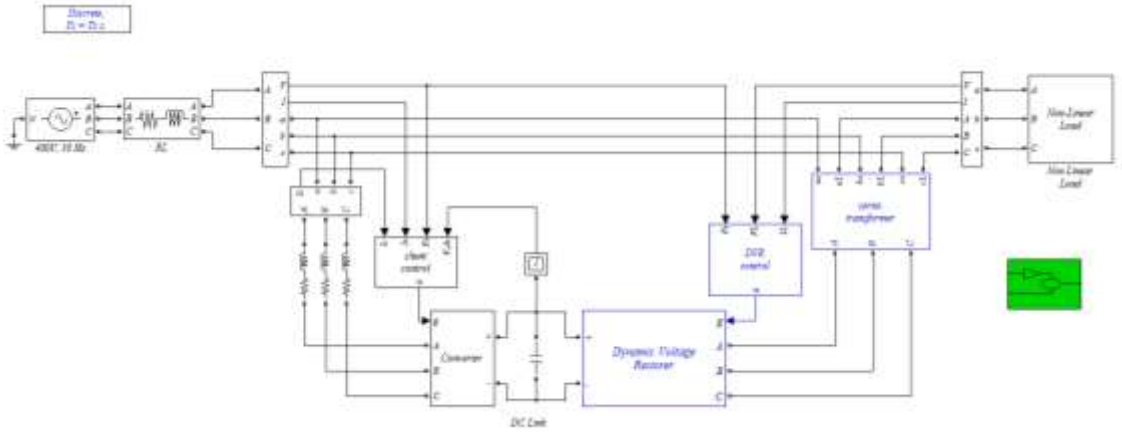

Fig-6: Proposed system design using MATLAB

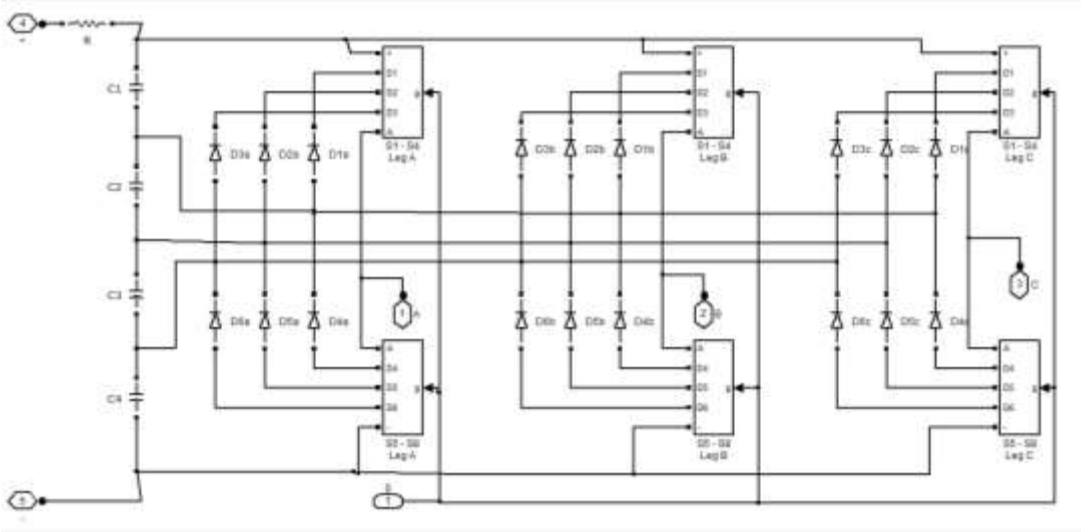

Fig-7: five-level inverter instead of two-level employed in DVR

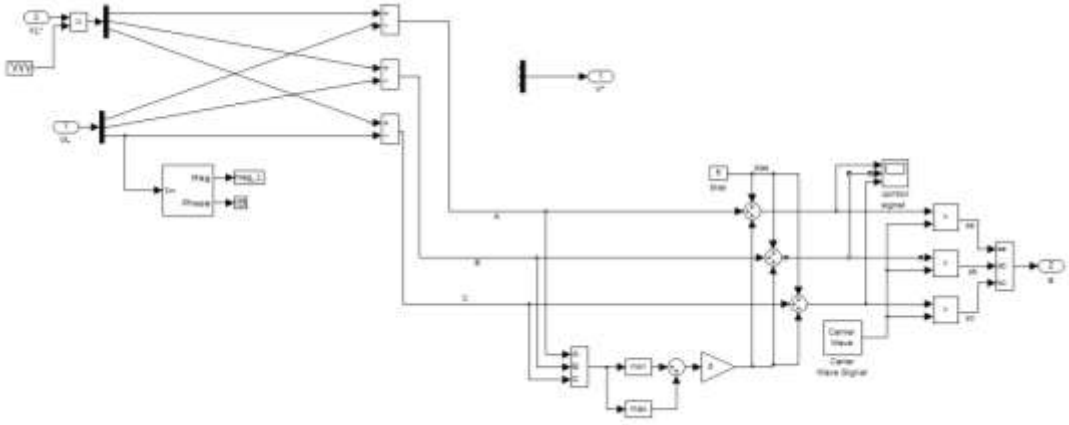

Fig-8: PWM pulse generation for five-level DVR inverter

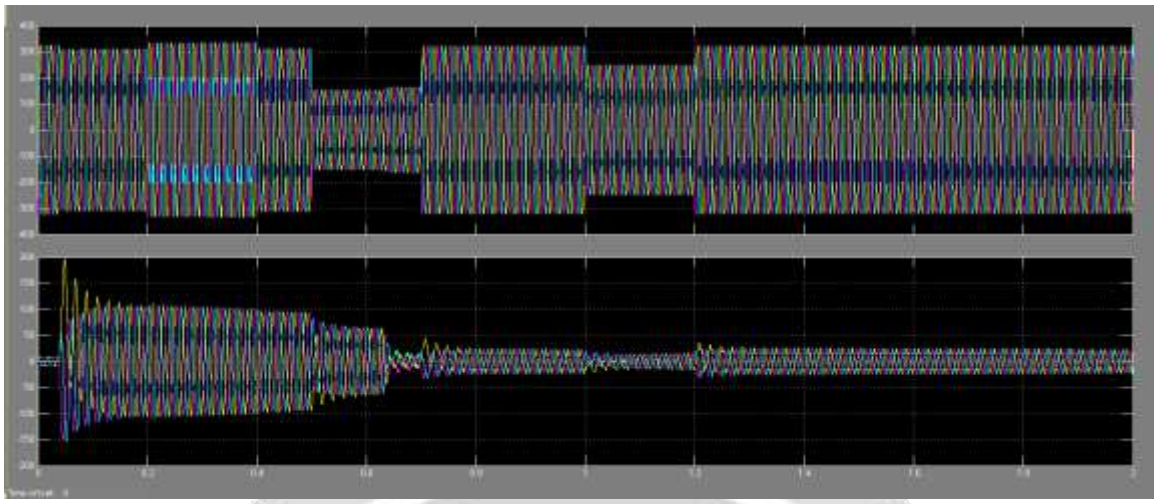

Fig-9: source voltage and current waveforms

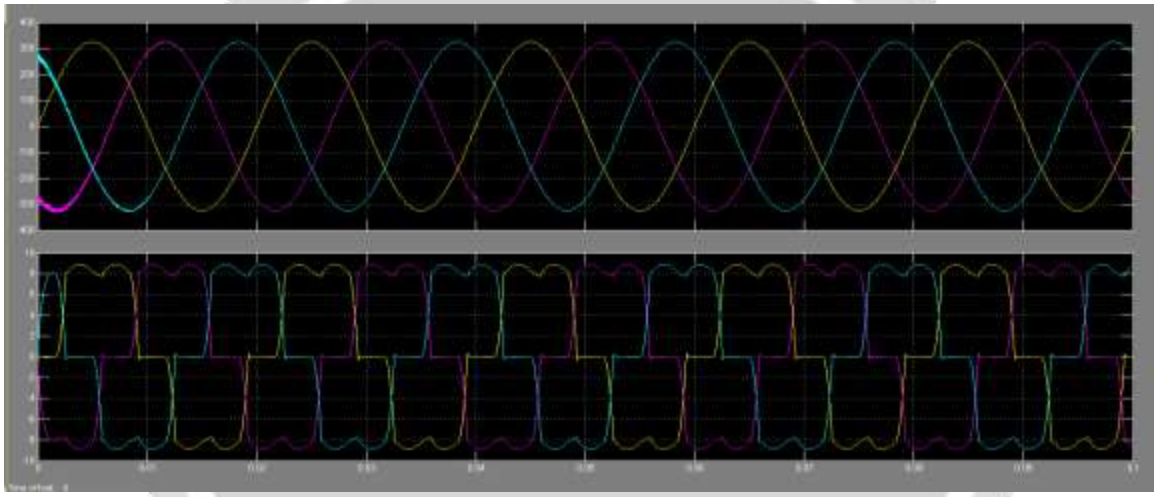

Fig-10: load voltage and current waveforms

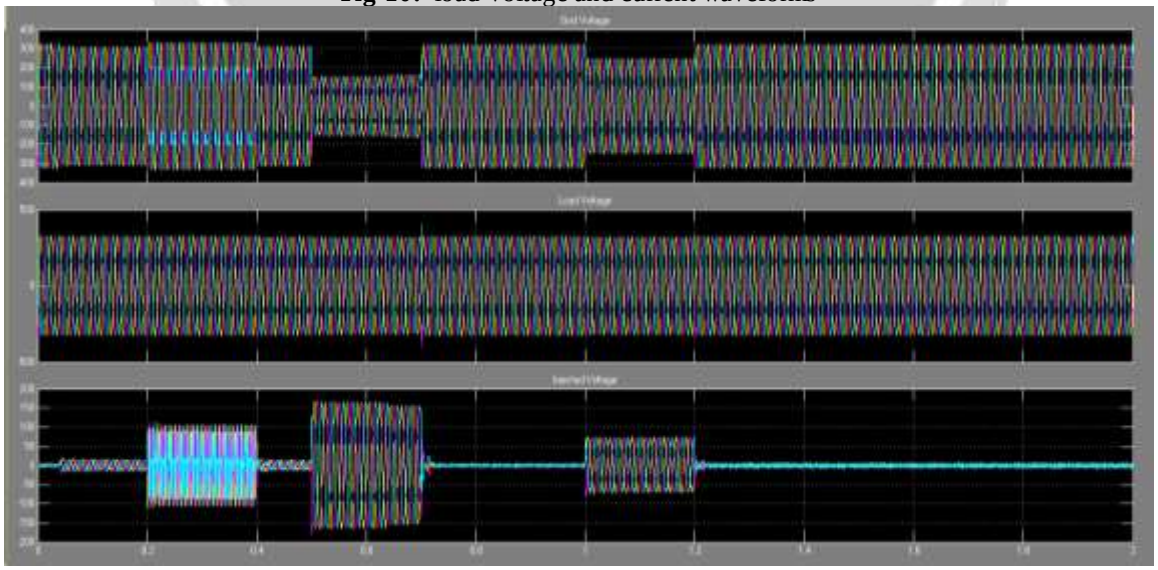

Fig-11: waveforms of source voltage, load voltage and injected voltage

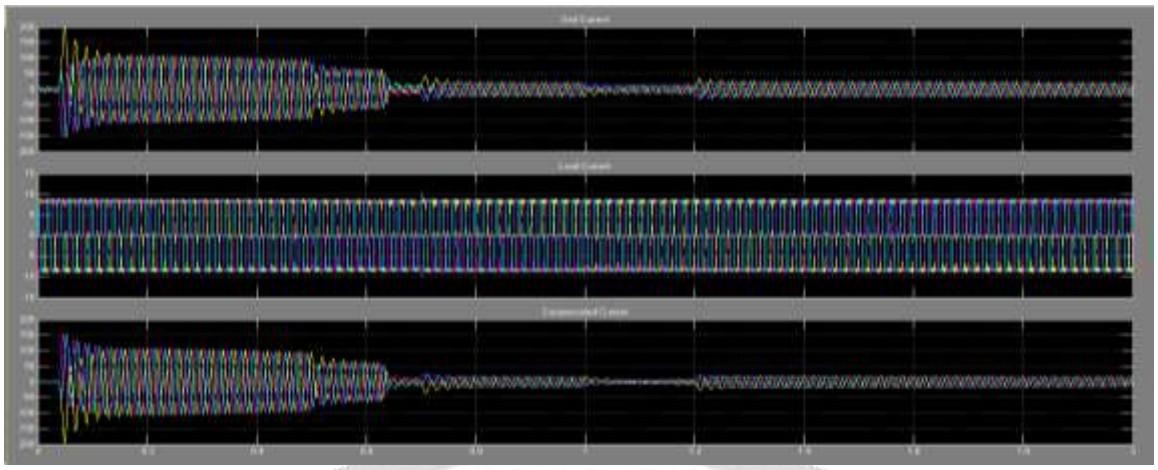

Fig-12: source current, load current and injected current

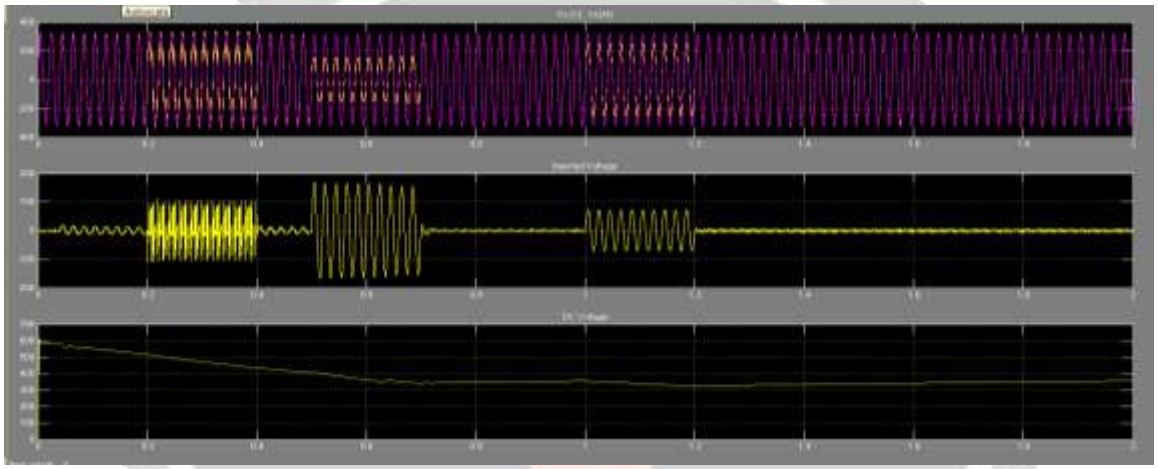

Fig-13: (i) source voltage, load voltage, (ii) injected voltage, (iii) dc-link

5. CONCLUSIONS

In this paper, an enhanced sag compensation scheme has been proposed for the capacitor-supported DVR. The proposed strategy improves the voltage quality of sensitive loads by protecting them against the grid voltage sags involving the phase jump. It also increases compensation time by operating in MAP mode through a controlled transition once the phase jump is compensated. To illustrate the effectiveness of the proposed method, an analytical comparison has been carried out with the existing phase jump compensation schemes. It is shown that the compensation time can be extended from 10 to 25 cycles (considering Presag injection as the reference method) for the designed limit of 50% sag depth with 45◦ phase jump. Further extension in compensation time can be achieved for intermediate sag depths. This extended compensation time can be seen as a considerable reduction in dc link capacitor size (for the studied case more than 50%) for the new installation. The effectiveness of the proposed method has been evaluated through extensive simulations in MATLAB. The extension of proposed work is done by replacing two-level inverter with five-level results demonstrate the feasibility of the proposed phase jump compensation method for efficiently for power quality applications.

6. REFERENCES

[1] O. Garc´ıa, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: A survey," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 749–755, May 2003.

[2] M.M. Jovanovic andY. Jang, "State-of-the-art, single-phase, active power factor-correction techniques for high-power applications—An overview," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 701–708, Jun. 2005.
[3] D. S. L. Simonetti, J. Sebastian, and J. Uceda, "The discontinuous conduction mode SEPIC and CUK power factor pre regulators: Analysis and design," *IEEE Trans. Ind. Electron.*, vol. 44, no. 5, pp. 630–637, Oct.1997.
[4] M. Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC rectifier with reduced components and conduction losses," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4153–4160, Sep. 2011.
[5] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "New efficient bridgeless Cuk rectifiers for PFC applications," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3292–3301, Jul. 2012.
[6] E. H. Ismail, "Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1147–1157, Apr. 2009.
[7] B. Su, J. Zhang, and Z. Lu, "Totem-pole boost bridgeless pfc rectifier with simple zero-current detection and full-range zvs operating at the boundary of DCM/CCM," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 427–435, Feb. 2011.
[8] J. Zhang, B. Su, and Z. Lu, "Single inductor three-level bridgeless boost power factor correction rectifier with nature voltage clamp," *IET Power Electron.*, vol. 5, no. 3, pp. 358–365, Mar. 2012.
[9] Y. Cho and J.-S. Lai, "Digital plug-in repetitive controller for single-phase bridgeless pfc converters," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 165–175, Jan. 2013.
[10] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "Bridgeless resonant pseudo boost PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5949–5960, Nov. 2014.
[11] R. Gules, W. M. Santos, F. A. Reis, E. F. R. Romaneli, and A. A. Badin, "A modified SEPIC converter with high static gain for renewable applications," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5860–5871, Nov. 2014.
[12] P. F. de Melo, R. Gules, E. F. R. Romaneli, and R. C. Annunziato, "A modified SEPIC converter for high-power-factor rectifier and universal input voltage applications," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 310–321, Feb. 2010.