MODELING AND SIMULINK OF SWITCHED CAPACITOR H-BRIDGE MULTILEVEL INVERTER TOPOLOGY FOR SINGLE SOURCE LOAD

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ABSTRACT

A proprietary capacitor based on a multilevel inverter that uses asymmetric source configuration is proposed. Multilevel inverters are widely used to enhance the harmonic profile of a product by increasing the number of levels. Due to the development of renewable energy, asymmetrical DC voltage sources are very common. Significant reductions in the number of converters for multilevel inverters have served as a major advantage over the years. Various voice modification systems have been proposed to increase the efficiency of multilevel inverters. These include Sinusoidal PWM (SPWM), Space Vector Modulation (SVM), Selective Harmonic Elimination (SHE) etc. Switching techniques used to control switches affect the harmonic content of the output power. Most flexibility strategies, however, have little to do with reducing output disruption. In order to control sound signals, low-level harmonics should be controlled. Reduced network operator PWM is proposed to control the harmonic content of the output power and thus reduce the total Harmonic deviation. The simulation of the proposed system is simulated and evaluated with the desired results in MATLAB / Simulink.

Keyword: - *Switched-capacitor, H-Bridge, multilevel inverter, high frequency inverter, Total Harmonic Distortion, Reduced carrier PWM.*

1. TITLE-1

Various renewable energy strategies, rapid technological advances and increasing environmental pressures have made renewable energy resources meet future energy needs. The availability of resources such as wind, solar, photovoltaic, biofuels, geothermal and hydel energy are important components of many energy systems. As more and more of these resources have become economically viable, their acceptance and integration into today's power networks is becoming increasingly widespread. Anxiety about the environment and the need to build a sustainable energy supply, will improve the use of renewable energy resources in power generation. However, the sustainability of available resources is a major factor to consider, therefore, the use of these resources should be the most efficient. Locally available resources can be integrated to generate energy, so that these resources can share the existing load. Where the load cannot be met by a single source, resources can be used to generate effective energy production.

Among the renewable energy sources available, solar power has become one of the most active areas in the study, both grid applications connected and independent. The rapid rate of growth in solar energy generation is mainly due to different inverter topologies. Inverters therefore play a very important role in power generation, distribution and transmission systems including renewable resources. The AC output power is created by changing the full bridge in the correct sequence. Inverter topologies can be mainly divided into single and multi-stage inverter. Although single-stage inverters are less common, the efficiency is very low due to the high rate of power output and the increase in harmonic content. High-level inverters have replaced single-stage inverter circuits due to high voltage power, low frequency switching, and low power losses. Typical multilevel topologies include diode clamp, flying capacitor, and cascaded H-bridge converters.

In the past, multilevel switching was achieved by phase switches of multiple single-phase waveforms of mechanical transformers that are put together manually using a series connected to transformer windings. As the number of levels increased it became difficult to see the way due to the needs of many transformer windings. Another solution was to replace multi-winding transformers with a multilevel dc bus. This is achieved by connecting multiple controlled cells in a series on the basis of a single device connection to a multilevel source. The result of this approach was a common reinforced neutral stand, a flying capacitor and Cascaded H top topologies. The biggest problem has been the increase in the exchange rate which is why the loss of exchange as rates increase. Thus new technologies in the literature have been developed to reduce the number of items and the associated losses.

Various modulation techniques for multilevel inverters are developed to reduce harmonic disturbances during extraction. In order to control acoustic noise, lower order harmonics should be controlled and control electro - magnetic interference, higher harmonics should be reduced [8]. Voice-changing techniques are selected according to the frequency. Typical voice modulation techniques include sinusoidal PWM, Space vector modulation, space vector control, Selective Harmonic Elimination (SHE) etc. SHE is a method of determining the appropriate angle of semiconductor switch in the inverter, the set angle should be less than 90 degrees. In SHE, only one (2m + 1) inverter (m-1) of the harmonics can be controlled. A standard inverter that uses a separate voltage is controlled by a PI controller to avoid input variables. In this paper a seven-level inverter is proposed using the reduced system of the network company PWM with the main purpose of reducing the harmonization of low order.

2. PROPOSED SYSTEM

A seven level inverter consisting of a front end DC-DC converter and H-bridge inverter is proposed. The front end converter is capable of producing multiple levels on a DC bus which when filled with the H bridge produces parallel bipolar levels and zero levels. The front-end switch consists of a capacitor called a switched capacitor. A modified capacitor in the converter converts the input power into integrated output levels. This is done by charging the capacitor at the input volume first, and then connecting the input source and capacitor to the series on the dc bus. A common feature of the circuit is the H-bridge inverter used in the output of the dc-dc converter. Therefore, a seven-level output can be obtained with a smaller amount of material compared to the standard seven inverter topologies.

Multiple input sources can be used to fall into the proposed seven inverter. In standard systems, if there are multiple sources, the sources must be connected to a series or inverters using each source must be connected in parallel to achieve high power levels. When input sources must be connected to a series, it requires complex power measurement schemes and the switching rate must be increased. Complex control algorithms should be used when inverters work in parallel. Both methods therefore add to the increase in costs and reduce the efficiency of the system.

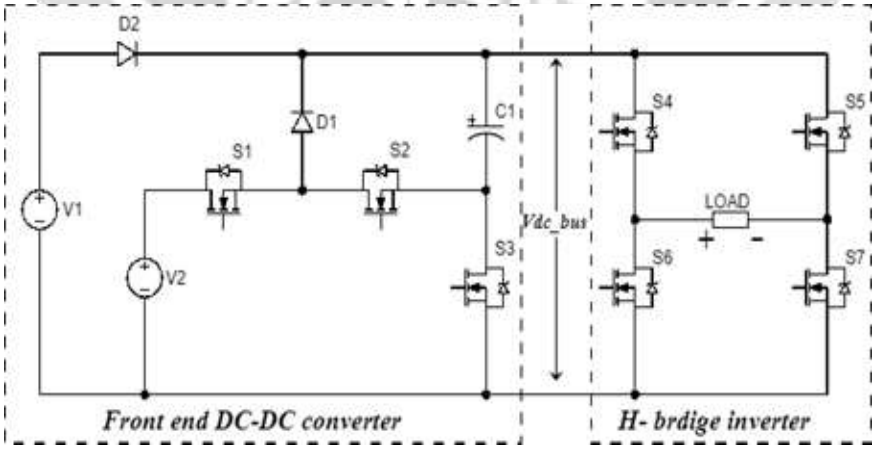

Fig -1: Proposed seven level inverter

The proposed system consists of seven switches from S1 to S7 as shown in fig. 1. The front end DC-DC converter employs two input sources (V1 and V2), three switches (S1, S2 and S3), two diodes (D1 and D2), and a switching capacitor C1. The converter produces three output DC levels: V1, V2 and (V1+V2). The H bridge circuit at the output produces corresponding six bipolar level ±V1, ±V2 and ±(V1+V2) and the zero level, which is to be required as the output of the seven level inverter circuit.

3. OPERATION OF THE PROPOSED CIRCUIT

The proposed seven level inverter works in different operating modes to obtain different voltage levels at the output. The switches are switched sequentially to obtain the desired seven level output voltage.

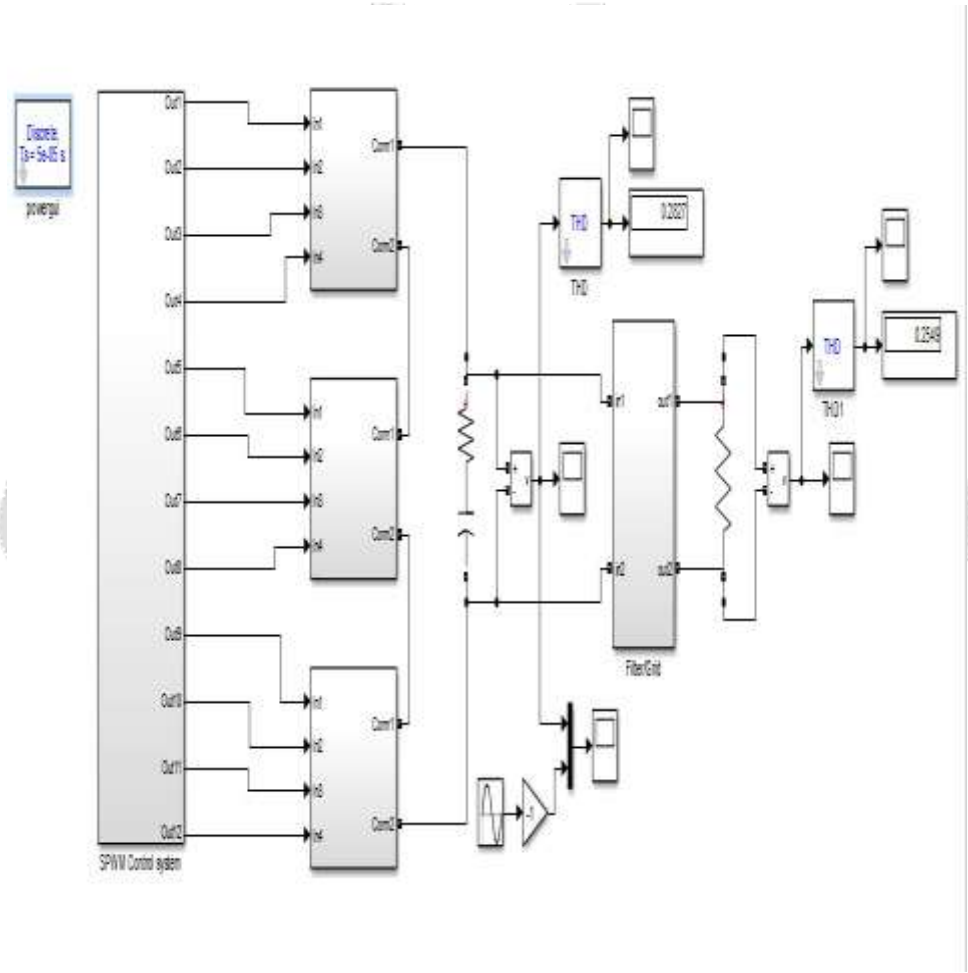

Fig -2: System Simulation

3.1 Output voltage ± V1

At first, in order to obtain +V1 at the output, the switches S3, S4 and S7 are turned on simultaneously so that the source V1 will be connected across the load. In the meantime the switching capacitor C1 gets charged to the input voltage V1. To obtain –V1, switch S3 is turned on along with S5 and S6.

3.2 Output voltage ± V2

The voltage level +V2 can be obtained by operating the switches S1, S4 and S7 and to obtain the corresponding negative part can be obtained by turning on S1 of the front end converter and S5 and S6 of the H- bridge inverter.

3.3 Output voltage ± (V1+V2)

By turning on the switches S1, S2, S4 and S7 the output voltage level of (V1+V2) can be obtained as the capacitor was initially charged to V1 during the first stage. By the operation of S5 and S6 along with S1 and S2 voltage level – (V1+V2) can be obtained.

3.4 Output voltage = 0 V

To obtain zero level at the output after positive half cycle S4 alone of the H – bridge inverter is turned on. The diode of switch S5 act as the freewheeling diode during that time. Similarly after the negative half cycle switch S6 alone is turned on and the diode of S7 is used for freewheeling. During both the cycles switches of front end converter remain in their previous states. The switching logic of the seven level inverter circuit is shown in table 1.

TABLE 1 Switching logic for the seven level inverter

S1	S2	S3	S4	S5	S6	S7	Vout
0	0	1	1	0	0	0	0
0	0	1	1	0	0	1	V1
1	0	0	1	0	0	1	V2
1	1	0	1	0	0	1	V1+V2
0	0	1	0	1	1	0	-V1
1	0	0	0	1	1	0	-V2
1	1	0	0	1	1	0	-(V1+V2)
0	0	1	0	0	1	0	0

4. Modulation Technique

Several modulation strategies can be adopted to detect the proposed seven inverter. These strategies form the basis for determining harmonic content in the form of wave emissions. The voice modulation method used to detect the proposed inverter aims to reduce the harmonics of the low-order order in the wavelength form and thus reduce THD. Here a Carrier Pulse Width Reduction Width modem is used with the Unified expression process. This method is one of the simplest PWM methods. The basic PWM method involves a larger number of carriers to detect the inverter switch. In addition, conventional PWM schemes lead to poor THD line performance. The proposed method varies with the inverter topology as rationale comments have not been made. According to the sequence of the changes of the various transformation's logical discourses of the different transformations are made. The system uses four carriers and a unipolar reference to detect seven shift switches.

Reduced PWM network company system, as the name suggests using a smaller number of carriers compared to conventional PWM methods. The main advantage of the proposed system is that topology is independent, this switching logic can control any decrease in the number of multilevel switches, regardless of the power source configuration. When the proposed topology is expanded to higher levels, the reduced PWM scheme provides less

computer load and improvements to the THD power line. The time to redesign the proposed PWM system is short and almost always the same for different inverter systems using the same number of levels. High frequency switching can be done with the proposed system due to the low computer load. The switching signals for a different switch for the proposed inverter circuit are shown in Figs. 3.

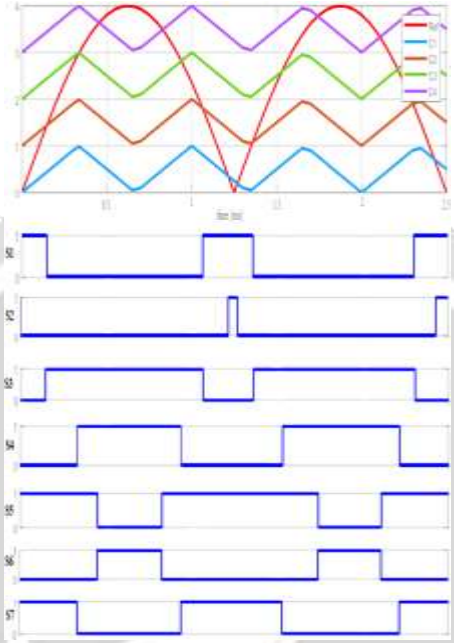

Fig -3: Switching scheme of the seven level inverter

5. CONCLUSION

A new 7-level used capacitor is proposed using a reduced PWM scheme inverter. The inverter can operate with multiple sources. Such situations arise when large corporations use a variety of renewable energy sources for power generation. Since multi-source network connections are not used, the problem of balancing power can be eliminated. The high frequency of output makes it easy to be hired for special applications such as aerospace. The reduced PWM network method with sensible integrated speakers helped in the proper transformation of the elements and was able to reduce THD. Structural harmonics are completely eliminated and low-level harmonics are reduced. If more resources are available, the system can be expanded to get more levels and therefore more efficient results can be obtained.

6. RESULT

Simulation of the proposed topology is performed by using MATLAB/SIMULINK software. The simulation for a nine level cascaded multilevel inverter with single dc source is shown in Fig.2 with two different input voltages with pure resistive load. By using PI controller the harmonic present in output voltage is reduced. The parameter used in the simulation for proposed topology.

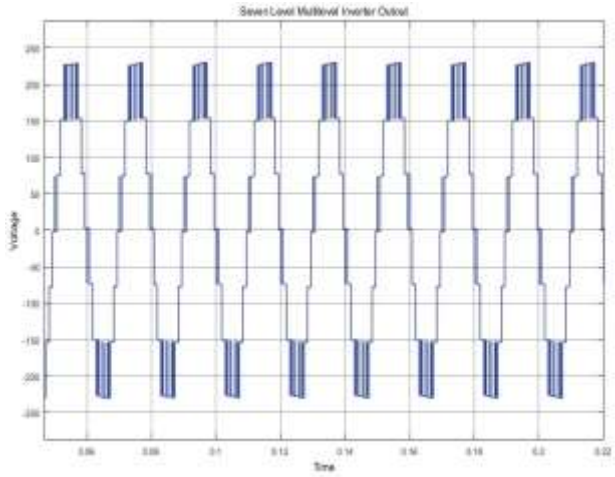

Fig -4: Seven Level Inverter Output

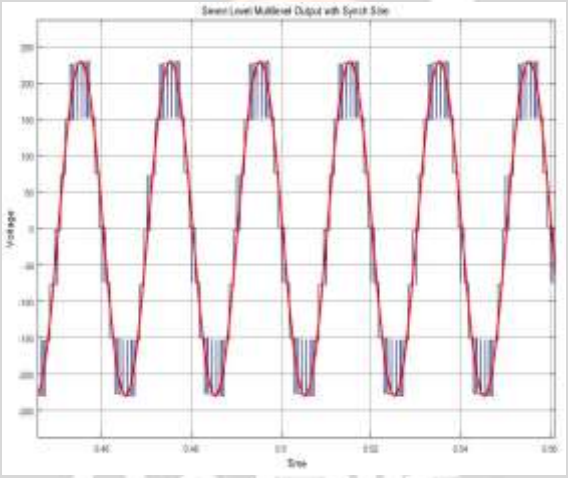

Fig -5: Seven Level Multilevel Output with Synch Sine

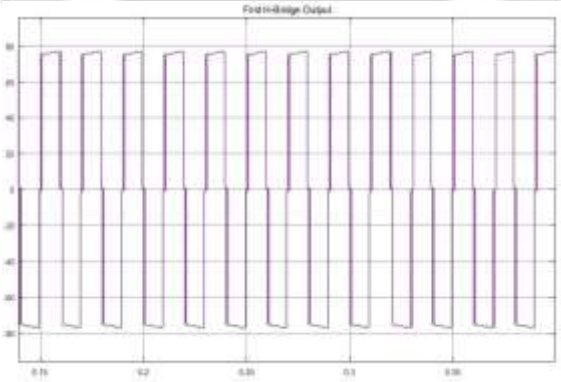

Fig -6: First H-Bridge output

Fig -7: First H-Bridge Switches signal

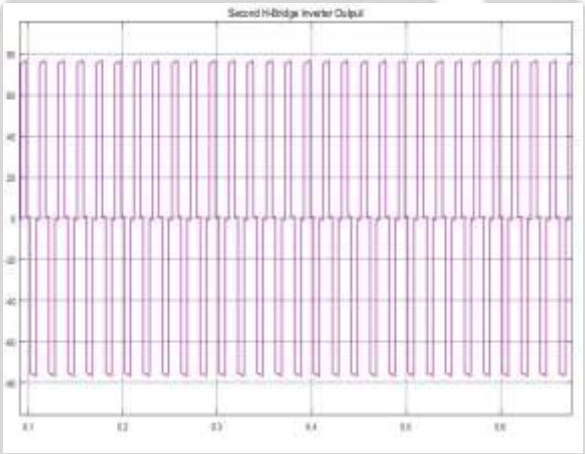

Fig -8: Second H-Bridge Output

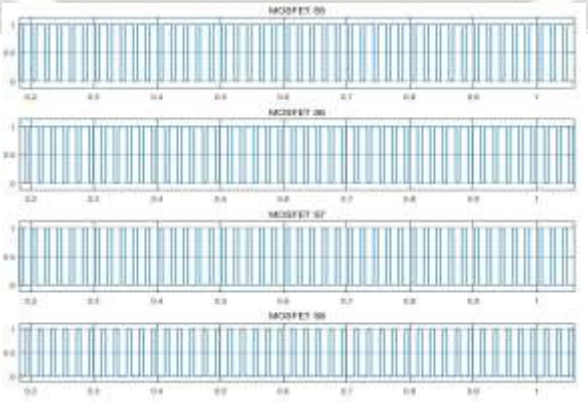

Fig -9: Second H-Bridge Switches signal

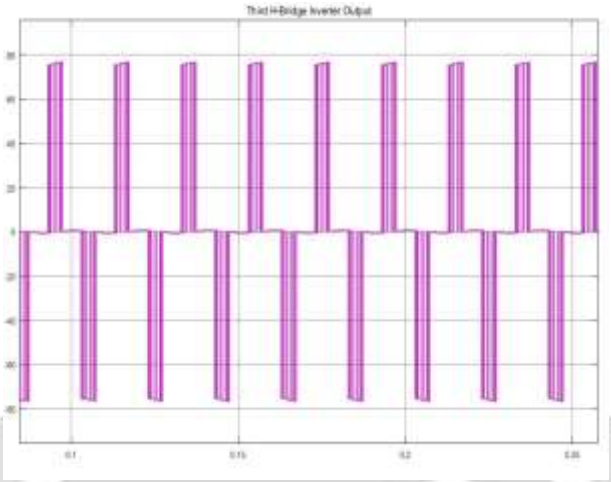

Fig -10: Third H-Bridge Output

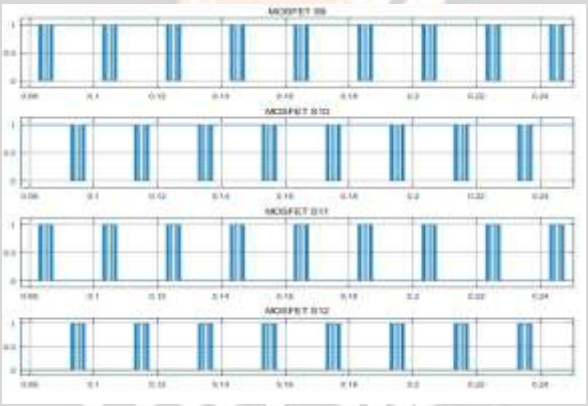

Fig -11: Third H-Bridge Switches signal

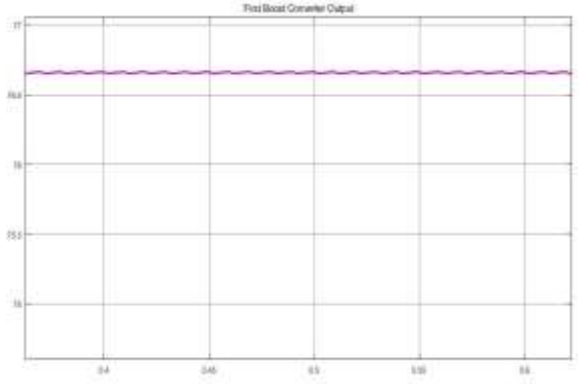

Fig -12: First Boost Converter Output

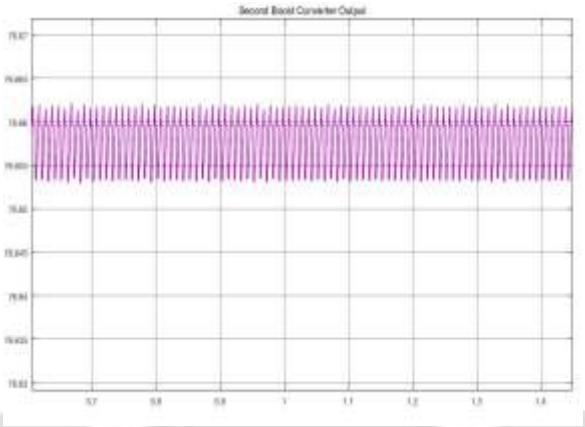

Fig -13: Second Boost Converter Output

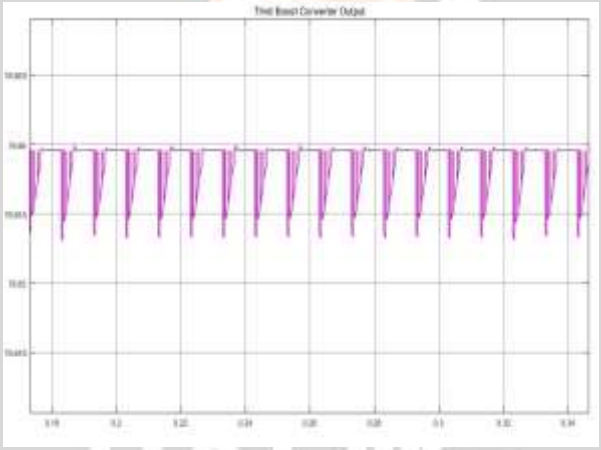

Fig -14: Third Boost Converter Output

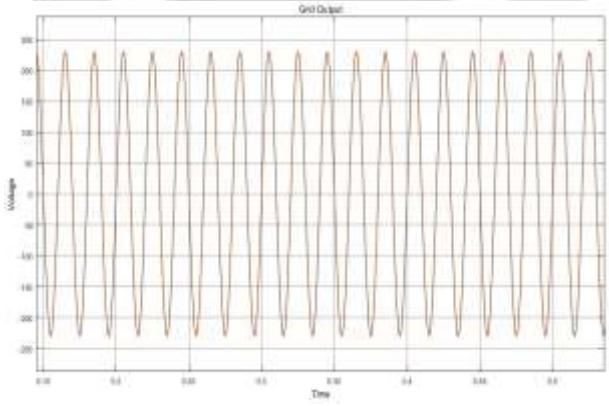

Fig -15: Grid Output

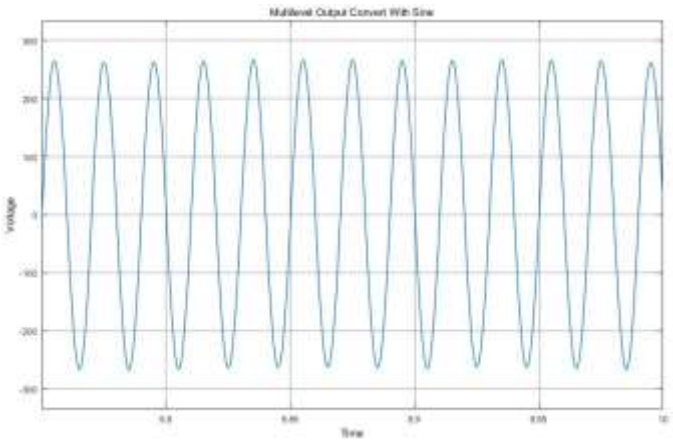

Fig -16: Multilevel Output Convert With Sine

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