# MULTI STANDARD TRANSFORM CORE USING CSDA

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# **ABSTRACT:**

The proposed high throughput multi standard transform it performs high speed compression MPEG, VC-1, and H.264 transformation using VLSI arithmetic calculations. It is optimized compression technique derived from basic compression scheme which results low cost and excellent quality with efficiency. As it makes the use of common sharing distributed arithmetic (CSDA) technique that efficiently reduces number of adders for high hardware sharing capability. Thus CSDA-MST core achieves a high throughput rate supporting multi standard transformation at low cost.

Keywords: Compression Techniques, VLSI design, CSDA, FPGA

#### **1.INTRODUCTION:**

H.264 and VC-1 are popular video compression standards. The VC-1 codec is designed to achieve state-ofthe-art compressed video quality at bit rates that may range from very low to very high. The codec can easily handle 1920 pixel × 1080 pixel presentation at 6 to 30 megabits per second (Mbps) for high-definition video. VC-1 is capable of higher resolutions such as 2048 pixels × 1536 pixels for digital cinema, and of a maximum bit rate of 135 Mbps. An example of very low bit rate video would be 160 pixel × 120 pixel presentation at 10 kilobits per second (Kbps) for modem applications. The basic functionality of VC-1 involves a block-based motion compensation and spatial transform scheme similar to that used in other video compression standards since MPEG-1 and H.261. However, VC-1 includes a number of innovations and optimizations that make it distinct from the basic compression scheme, resulting in excellent quality and efficiency. VC-1 Advanced Profile is also transport and container independent. This provides even greater flexibility for device manufacturers and contents services.

A significant amount of research has been conducted to efficiently combine and implement the transform units for multiple codec's. On the other hand little research is focused on the implementation of multi-quantized unit. Among the multiple-transform units, a unified Inverse Discrete Cosine Transform (IDCT) architecture to support five standards (such as, AVS, H.264, VC-1, MPEG-2/4 and JPEG) is presented. The authors in offer an area efficient architecture to perform a DCT-based transform for JPEG, MPEG-4, VC-1 and H.264 using delta mapping. The design in is an IDCT and IQ circuit for H.264, MPEG-4 and VC-1. The MJPEG standard defines quantization as the division operation of the DCT coefficient coming from the transform unit by the corresponding Q value (specified by the quantization matrix). MJPEG allows specification of Q-matrices that facilitates the allocation of more bits for the representation of coefficients which are visually more significant.

The intercommunications between the video devices using different standards are so much inconvenient, thus video codec supporting multiple standards are more useful and more attractive. In this brief, low cost very large scale integration (VLSI) architecture is designed for multi standard inverse Discrete Cosine transform. It is used in multi standard decoder of MPEG-2, MPEG-4 ASP, and VC-1. Two circuit share strategies, factor share (FS) an adder share (AS) are applied to the inverse transform architecture for saving its circuit resource. Pipelined stages are used in this Multistandard inverse transform to increase the operational speed.

The possibility to employ hierarchical prediction structures for providing temporal scalability with several layers while improving the coding efficiency and increasing the effectiveness of quality and spatial scalable coding. New methods for inter-layer prediction of motion and residual improving the coding efficiency of spatial scalable and quality scalable coding. The concept of key pictures for efficiently controlling the drift for packet-based quality scalable coding with hierarchical prediction structures. Single motion compensation Loop decoding for spatial and quality scalable coding providing a decoder complexity close to that of single-layer coding.

#### 2. MODULE DESCRIPTION:

#### 1-D common sharing distributed arithmetic-MST:

Based on the proposed CSDA algorithm, the coefficients for MPEG-1/2/4, H.264, and VC-1 transforms are chosen to achieve high sharing capability for arithmetic resources. To adopt the searching flow, software code will help to do the iterative searching loops by setting a constraint with minimum nonzero elements. In this paper, the constraint of minimum nonzero elements is set to be five. After software searching, the coefficients of the CSD expression, where 1 indicates –1. Note that the choice of shared coefficient is obtained by some constraints. Thus, the chosen CSDA coefficient is not a global optimal solution. It is just a local or suboptimal solution. Besides, the CSD codes are not the optimal expression, which have minimal nonzero bits. However, the chosen coefficients of CSD expression can achieve high sharing capability for arithmetic resources by using the proposed CSDA algorithm. More information about CSDA coefficients for MPEG-1/2/4, H.264, and VC-1 transforms.



#### Even part common sharing distributed arithmetic circuit:

The SBF module executes for the eight-point transform and bypasses the input data for two four-point transforms. After the SBF module, the CSDA\_E and CSDA\_O execute and by feeding input data a and b, respectively. The CSDA\_E calculates the even part of the eight-point transform, similar to the four-point Trans form for H.264 and VC-1 standards. Within the architecture of CSDA\_E, two pipeline stages exist (12-bit and 13-bit). The first stage executes as a four-input butterfly matrix circuit, and the second stage of CSDA\_E then executes by using the proposed CSDA algorithm to share hardware resources in variable standards.



Fig-2: Even part common sharing distributed arithmetic circuit

#### Odd part common sharing distributed arithmetic circuit:

Similar to the CSDA\_E, the CSDA\_O also has two pipeline stages. Based on the proposed CSDA algorithm, the CSDA\_O efficiently shares the hardware resources among the odd part of the eight-point transform and four-point transform for variable standards. It contains selection signals of multiplexers (MUXs) for different standards. Eight adder trees with error compensation (ECATs) are followed by the CSDA\_E and CSDA\_O, which add the nonzero CSDA coefficients with corresponding weight as the tree-like architectures. The ECATs circuits can alleviate truncation error efficiently in small area design when summing the nonzero data all together.



Fig-3: Odd part common sharing distributed arithmetic circuit

#### 2-D common sharing distributed arithmetic -MST core:

This section provides a discussion of the hardware resources and system accuracy for the proposed 2-D CSDA-MST core and also presents a comparison with previous works. Finally, the characteristics of the implementation into a chip are described.



Fig-4: Block diagram of 2-D CSDA

#### TMEM:

The TMEM is implemented using 64-word 12-bit dual-port registers and has a latency of 52 cycles. Based on the time scheduling strategy and result of the time scheduling strategy, the 1st-D and 2nd-D transforms are able to be computed simultaneously.

#### CSDA:

Distributed Arithmetic (DA) has been wildly adopted for its computational efficiency in many digital signal processing applications such as DCT (Discrete Cosine Transform), DFT (Discrete Fourier Transform), FIR (Finite Impulse Response), and DHT (Discrete Hartley Transform). These applications involve the computation of inner products between two vectors, one of which is a constant. The general method to generate the products is to use a MAC (multiply and accumulate) unit, which is fast but has a high cost in the case of long-length inner-products. In contrast, DA provides an efficient solution to realize the inner products by using memory look-up and accumulation

operations. The idea behind the conventional DA, called ROM-based, is to replace multiplication operations by precomputing all possible values and storing these in a ROM. According to the ROM based DA can reduce the circuit size by 50-80% on average. Custom reconfigurable technology emerged to satisfy the simultaneous demand for flexibility and efficiency. Custom/domain-specific reconfigurable arrays can be programmed to adapt for different applications, so the efficiency of the hardware and flexibility of the whole system is improved. Earlier works, such as, show good performance in area, power consumption and speed. Since a domain-specific reconfigurable architecture targets few application fields, it achieves better performance than a general purpose FPGA device.

#### PROPOSED 2-D CSDA-MST CORE DESIGN

We introduces the proposed 2-D CSDA-MST core implementation. Neglecting the scaling factor, the one dimensional (1-D) eight-point transform can be defined as follows



Where

Because the eight-point coefficient structures in MPEG- 1/2/4, H.264, and VC-1 standards are the same, the eight-point transform for these standards can use the same mathematic derivation. According to the symmetry property, the 1-D eight point transform in (8) can be divided into even and odd two four-point transforms, Ze and Zo, as listed in (9) and (10), respectively

$$\mathbf{Z}_{e} = \begin{bmatrix} Z_{0} \\ Z_{2} \\ Z_{4} \\ Z_{6} \end{bmatrix} = \begin{bmatrix} c_{4} & c_{4} & c_{4} & c_{4} \\ c_{2} & c_{6} & -c_{6} & -c_{2} \\ c_{4} & -c_{4} & -c_{4} & c_{4} \\ c_{6} & -c_{2} & c_{2} & -c_{6} \end{bmatrix} \begin{bmatrix} a_{0} \\ a_{1} \\ a_{2} \\ a_{3} \end{bmatrix}$$
$$= \mathbf{C}_{e} \cdot \mathbf{a}$$
$$\mathbf{Z}_{o} = \begin{bmatrix} Z_{1} \\ Z_{3} \\ Z_{5} \\ Z_{7} \end{bmatrix} = \begin{bmatrix} c_{1} & c_{3} & c_{5} & c_{7} \\ c_{3} & -c_{7} & -c_{1} & -c_{5} \\ c_{5} & -c_{1} & c_{7} & c_{3} \\ c_{7} & -c_{5} & c_{3} & -c_{1} \end{bmatrix} \begin{bmatrix} b_{0} \\ b_{1} \\ b_{2} \\ b_{3} \end{bmatrix}$$
$$= \mathbf{C}_{o} \cdot \mathbf{b}$$

Where

$$\mathbf{a} = \begin{bmatrix} x_0 + x_7 \\ x_1 + x_6 \\ x_2 + x_5 \\ x_3 + x_4 \end{bmatrix}, \quad \mathbf{b} = \begin{bmatrix} x_0 - x_7 \\ x_1 - x_6 \\ x_2 - x_5 \\ x_3 - x_4 \end{bmatrix}.$$

The even part of the operation in (10) is the same as that of the four-point H.264 and VC-1 transformations. Moreover, the even part  $\mathbf{Z}e$  can be further decomposed into even and odd parts:  $\mathbf{Z}ee$  and  $\mathbf{Z}eo$ 

$$\mathbf{Z}_{ee} = \begin{bmatrix} Z_0 \\ Z_4 \end{bmatrix} = \begin{bmatrix} c_4 & c_4 \\ c_4 & -c_4 \end{bmatrix} \begin{bmatrix} A_0 \\ A_1 \end{bmatrix}$$
$$= \mathbf{C}_{ee} \cdot \mathbf{A}$$
$$\mathbf{Z}_{eo} = \begin{bmatrix} Z_2 \\ Z_6 \end{bmatrix} = \begin{bmatrix} c_2 & c_6 \\ c_6 & -c_2 \end{bmatrix} \begin{bmatrix} B_0 \\ B_1 \end{bmatrix}$$
$$= \mathbf{C}_{eo} \cdot \mathbf{B}$$

Where

$$\mathbf{A} = \begin{bmatrix} a_0 + a_3 \\ a_1 + a_2 \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} a_0 - a_3 \\ a_1 - a_2 \end{bmatrix}.$$

#### VLSI:

VLSI stands for "Very Large Scale Integrated Circuits". It's a classification of ICs. An IC of common VLSI includes about millions active devices. Typical functions of VLSI include Memories, computers, and signal processors, etc. A semiconductor process technology is a method by which working circuits can be manufactured from designed specifications. There are many such technologies, each of which creates a different environment or style of design. In integrated circuit design, the specification consists of polygons of conducting and semiconducting material that will be layered on top of each other to produce a working chip.

When a chip is custom-designed for a specific use, it is called an application-specific integrated circuit (ASIC). Printed-circuit (PC) design also results in precise positions of conducting materials, as they will appear on a circuit board; in addition, PC design aggregates the bulk of the electronic activity into standard IC packages, the position and interconnection of which are essential to the final circuit. Printed circuitry may be easier to debug than integrated circuitry is, but it is slower, less compact, more expensive, and unable to take advantage of specialized silicon layout structures that make VLSI systems so attractive.

#### FPGA:

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing—hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). FPGAs can be used to implement any logical function that an ASIC could perform. The ability to update the functionality after shipping, partial re-configuration of the portion of the

Design and the low non-recurring engineering costs relative to an ASIC design (notwithstanding the generally higher unit cost), offer advantages for many applications.

FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together"—somewhat like a one-chip

Programmable breadboard. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

#### Simulation Analysis:

Verilog HDL is a Hardware Description Language (HDL). A Hardware Description Language is a language used to describe a digital system, for example, a computer or a component of a computer. One may describe a digital system at several levels. For example, an HDL might describe the layout of the wires, resistors and transistors on an Integrated Circuit (IC) chip, i. e., and the switch level. Or, it might describe the logical gates and flip flops in a digital system, i. e., the gate level. An even higher level describes the registers and the transfers of vectors of information between registers. This is called the Register Transfer Level (RTL). Verilog supports all of these levels. However, this handout focuses on only the portions of Verilog which support the RTL level.

# Selected Butterfly:



Fig-5- output waveform for selected butterfly

MUX:



Fig-6- mux output waveform

# **Even Part CSDA:**

![](_page_5_Figure_9.jpeg)

# Fig7-Outputwaveform for Evenpart common Sharing distributed Arithmetic

# 1<sup>ST</sup> STAGE:

![](_page_6_Figure_3.jpeg)

![](_page_6_Figure_4.jpeg)

# 2<sup>ND</sup> STAGE SUB0:

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# Fig 9-Second stage sub module0 output waveform

![](_page_6_Figure_8.jpeg)

# Fig 10-Second stage Sub2 module output wave form

2<sup>ND</sup>STAGE SUB2:

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Fig 11-Top module odd part common sharing distributed arithmetic output

![](_page_7_Figure_5.jpeg)

Fig 12-Output waveform of Error -compensated Adder Tree (ECAT-1D)

![](_page_7_Figure_7.jpeg)

Fig 13- Permutation matrix for each of the N\_N M-bit fixed point constants

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Fig 13-output waveform of one dimensional common sharing distributed arithmetic multistandard

transform-1 when s=0

# 1D CSDA MST 1 S=1

![](_page_8_Figure_7.jpeg)

![](_page_8_Figure_8.jpeg)

#### transform-1 when s=1

![](_page_8_Figure_10.jpeg)

Fig 15-output waveform of one dimensional common sharing distributed arithmetic multistandard transform-2 when s=0

## 1D CSDA MST 2 S=1:

![](_page_9_Figure_3.jpeg)

Fig 16-output waveform of one dimensional common sharing distributed arithmetic multistandard

transform-2 when s=1

# **Transpose Memory:**

![](_page_9_Figure_7.jpeg)

# Fig 17-output waveform of Transpose memory

Top module 2D CSDA\_MST CORE SelTx&Rst=0:

![](_page_9_Figure_10.jpeg)

Fig 18-output waveform of 2D Common sharing distributed arithmetic for MST CORE when transmit & receive port is =0

# Top module 2D CSDA\_MST CORE SelTx&Rst=0 Decimal:

![](_page_10_Figure_3.jpeg)

Fig 19-Output waveform of Top module 2D CSDA\_MST core when SE1TX & Rst=0 Top module 2D CSDA\_MST CORE SelTx=1:

![](_page_10_Figure_5.jpeg)

Fig 20- Output waveform of Top module 2D CSDA\_MST core when SE1TX=1 Top module 2D CSDA\_MST CORE SelTx=1 Decimal:

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0.4	S. ID CEDA HET/NZ	2000000001001	000000000011		000111111	20000001	2000000000	2001111111		2000000001		1						
-	E TO FREE METHON	1000000031106.1			SAUGUL	discourse in		Constant of the	Statements.		Conservation of the							
-		8500 re	1977			10 mm		591 mg		100 mg		10		300 m		780		
- 11	Curror 1	2554m	- 100										255	Ans				

Fig 21-Output waveform of Top module 2D CSDA\_MST core when SE1TX=1 Decimal

# **3. DEVICE UTILIZATION SUMMARY:**

## **Proposed:**

oject File:	ITVL26.ise	Current State:	Placed and Rou	uted
odule Name:	S_2D_CSDA_MST	+ Errors:	No Errors	
arget Device:	xc3e400-5fg320	Warnings:	513 Waminga	
oduct Version:	ISE 9.1i	Updated:	Thu Dec 5 14:0	03:55 2013
	ITVL26 Par	tition Summary		
partition information was found.				
	Device Utili	zation Summary		
ogic Utilization	Used	Available	Utilization	Note(s)
umber of Slice Flip Flops	1,259	7,168	17%	
umber of 4 input LUTs	2,095	7,168	29%	
ogio Distribution				
umber of occupied Slices	1,310	3,584	36%	
Number of Slices containing only related log	gic 1,310	1,310	100%	
Number of Slices containing unrelated logic	0	1,310	0%	
ptar Number of 4 input LUTs	2.279	7.168	31%	
imper used as logic	2,095			
mber of bonded IOBs	104	221	95%	
imber of GCLKs	1	8	12%	
ptal equivalent gate count for design	28.606	0	12.11	
ditional JTAG gate count for IOBs	9.024			
odification:				
Iodification:	modi.ise	Current State:	Placed and Ro	uted
Iodification: Project File: Module Name:	modi.ise S_2D_CSDA_MST	Current State: • Errors:	Placed and Ro No Errors	uted
Iodification: Project File: Module Name: Target Device:	modi.ise S_2D_CSDA_MST xc3s400-5fg320	Current State: • Errors: • Warnings:	Placed and Ro No Errors 215 Warnings	uted
Iodification: Project File: Module Name: Target Device: Product Version:	modilise S_2D_CSDA_MST xc3s400-5fg320 ISE 9.1i	Current State: • Errors: • Warnings: • Updated:	Placed and Ro No Errors 215 Warnings Thu Dec 5 19:0	uted 03:35 2013
Iodification: Project File: Module Name: Target Device: Product Version:	modilise S_2D_CSDA_MST xc3s400-5fg320 ISE 9.1i MODI Par	Current State: • Errors: • Warnings: • Updated: tition Summary	Placed and Ro No Errors 215 Warnings Thu Dec 5 19:0	uted 03:35 2013
Iodification: Project File: Module Name: Target Device: Product Version: No partition information was found.	modi.ise S_2D_CSDA_MST xc3e400-5fg320 ISE 9.1i MODI Par	Current State: • Errors: • Warnings: • Updated: tition Summary	Placed and Ro No Errors 215 Warnings Thu Dec 5 19:0	uted 03:35 2013
Iodification: Project File: Module Name: Target Device: Product Version: No partition information was found.	modilise S_2D_CSDA_MST xc3s400-5fg320 ISE 9.1i MODI Par	Current State: • Errors: • Warnings: • Updated: tition Summary	Placed and Ro No Errors 215 Warnings Thu Dec 5 19:0	uted 03:35 2013
Iodification: Project File: Module Name: Target Device: Product Version: Ne partition information was found. Logic Utilization	modi.ise S_2D_CSDA_MST xc3s400-5fg320 ISE 9.1i MODI Par Device Util Used	Current State: • Errors: • Warnings: • Updated: tition Summary ization Summary Available	Placed and Ro No Errors 215 Warnings Thu Dec 5 19:0	uted 03:35 2013 Note(s)
Iodification: Project File: Module Name: Target Device: Product Version: No partition information was found. Logic Utilization Number of Silce File Files	modulse S_2D_CSDA_MST xc3s400-5fg320 ISE 9.1i MODI Par Device Util Used 10	Current State: • Errors: • Warnings: • Updated: tition Summary ization Summary Available	Placed and Ro No Errors 215 Warnings Thu Dec 5 19:0	uted 03:35 2013 Note(s)
Iodification: Project File: Module Name: Target Device: Product Version: No partition information was found. Logic Utilization Number of Silce Filp Flops Number of Alignet ULT=	modi.ise S_2D_CSDA_MST xc3s400-5fg320 ISE 9.1i MODI Par Device Util Used 704 2.048	Current State: • Errors: • Warnings: • Updated: tition Summary ization Summary Available 7,168 7,168	Placed and Ro No Errors 215 Warnings Thu Dec 5 19:0 Utilization 9%	uted 03:35 2013 <b>Note(s)</b>
Iodification: Project File: Module Name: Target Device: Product Version: No partition information was found. Logic Utilization Number of Slice Filp Flops Number of 4 input LUTs Logic Device Statements	modi.ise S_2D_CSDA_MST xc3s400-5fg320 ISE 9.1i MODI Par Device Util Used 2 704 2,048	Current State: • Errors: • Warnings: • Updated: tition Summary ization Summary Available 7,168 7,168	Placed and Ro No Errors 215 Warnings Thu Dec 5 19:0 Utilization 9% 28%	uted 03:35 2013 <b>Note(s)</b>
Iodification: Project File: Module Name: Target Device: Product Version: No partition information was found. Logic Utilization Number of Slice Filp Flops Number of 4 input LUTs Logic Distribution	modi.ise S_2D_CSDA_MST xc3s400-5fg320 ISE 9.1i MODI Par Device Util Used 704 2,048 1	Current State: • Errors: • Warnings: • Updated: tition Summary ization Summary Available 7,168 7,168	Placed and Ro No Errors 215 Wamings Thu Dec 5 19:0 Utilization 9% 28%	uted 03:35 2013 Note(s)
Iodification: Project File: Module Name: Target Device: Product Version: No partition information was found.  Logic Utilization Number of Slice Filp Flops Number of 4 input LUTs Logic Distribution Number of occupied Slices	modi.ise	Current State:         • Errors:         • Warnings:         • Updated:         tition Summary         Ization Summary         Available         7,168         7,168         3,584	Placed and Ro No Errors 215 Wamings Thu Dec 5 19:0 Utilization 9% 28% 28% 34%	uted 03:35 2013 Note(s)
Iodification: Project File: Module Name: Target Device: Product Version: No partition information was found.  Logic Utilization Number of Slice Filp Flops Number of Slice Filp Flops Number of LUTs Logic Distribution Number of Slices containing only related Number of Slices containing only related	modi.ise S_2D_CSDA_MST xc3e400-5fg320 ISE 9.1i MODI Par Device Util 2.048 1.239 logic 1.239	Current State: Errors: Warnings: Updated: tition Summary ization Summary Available 7,168 7,168 7,168 4 1,239	Placed and Ro No Errors 215 Wamingz Thu Dec 5 19:0 Utilization 9% 28% 28% 34% 34% 100%	uted 03:35 2013 Note(s)
Iodification: Project File: Module Name: Target Device: Product Version: No partition information was found.  Logic Utilization Number of Slice Flip Flops Number of Slice Flip Flops Number of A input LUTs Logic Distribution Number of occupied Slices Number of Slices containing only related log Number of Slices containing unrelated log	modi.ise S_2D_CSDA_MST xc3s400-5fg320 ISE 9.1i MODI Par MODI Par 2000 1200 1	Current State: Errors: Warnings: Updated: tition Summary Available 7,168 7,168 7,168 1,239 1,239	Placed and Ro           No Errors           215 Warnings           Thu Dec 5 19:0           Thu Dec 5 19:0           Utilization           9%           28%           34%           100%           0%	uted 03:35 2013 Note(s)
Iodification: Project File: Module Name: Target Device: Product Version: No partition information was found.  Logic Utilization Number of Slice Filip Flops Number of Slice Filip Flops Number of A input LUTs Logic Distribution Number of Scies containing only related log Total Number of 4 input LUTs	modi.ise S_2D_CSDA_MST xc3s400-5fg320 ISE 9.1i MODI Par MODI Par 2.048 1.239 logic 1.239 gic 0 0	Current State:         • Errors:         • Warnings:         • Updated:         tition Summary         Available         7,168         7,168         7,168         1,239         1,239         1,239         7,168	Placed and Ro           No Errors           215 Warnings           Thu Dec 5 19:0           Thu Dec 5 19:0           Utilization           9%           28%           34%           100%           0%           30%	uted 03:35 2013 Note(s)
Iodification: Project File: Module Name: Target Device: Product Version: No partition information was found.  Logic Utilization Number of Slice Filp Flops Number of LUTs Logic Distribution Number of occupied Slices Number of Slices containing only related log Total Number of 4 input LUTs Number of Slices containing unrelated log Total Number of 4 input LUTs Number used as logic	modi.ise S_2D_CSDA_MST xc3s400-5fg320 ISE 9.1i MODI Par Device Util 2.048 1.239 logic 1.239 logic 0 2.158	Current State: • Errors: • Warnings: • Updated: tition Summary ization Summary Available 7,168 7,168 7,168 1,239 1,239 1,239 7,168	Placed and Ro           No Errors           215 Warnings           Thu Dec 5 19:0           Thu Dec 5 19:0           Utilization           9%           28%           34%           100%           30%	Note(s)
Iodification: Project File: Module Name: Target Device: Product Version: No partition information was found.  Logic Utilization Number of Slice Flip Flops Number of Slice Flip Flops Number of ccupied Slices Number of Slices containing only related log Total Number of 4 input LUTs Number used as logic Number used as a route-thru	modi.ise S_2D_CSDA_MST xc3s400-5fg320 ISE 9.1i MODI Par Device Util Used 1.239 logic 1.239 ojic 0 0 2.158 2.048 110	Current State:         • Errors:         • Warnings:         • Updated:         tition Summary         Zation Summary         Available         7,168         3,584         1,239         1,239         7,168	Placed and Ro           No Errors           215 Warnings           Thu Dec 5 19:0           Utilization           9%           28%           34%           100%           0%           30%	Note(s)
Iodification: Project File: Module Name: Target Device: Product Version: No partition information was found.  Logic Utilization Number of Slice Filp Flops Number of A input LUTs Logic Distribution Number of Slices containing only related in Number of Slices containing unrelated log Total Number of 4 input LUTs Number of bonded IoBs	modi.ise S_2D_CSDA_MST xc3s400-5fg320 ISE 9.1i MODI Par Device Util Used 1.239 Iogic 1.239 pic 0 2,158 2,048 1.239 Iogic 1.239 Iogic 1.238 Iogic 1.2388 Iogic 1.23	Current State: • Errors: • Warnings: • Updated: tition Summary ization Summary Available 7,168 7,168 3,584 1,239 1,239 7,168 221	Placed and Ro           No Errors           215 Warnings           Thu Dec 5 19:0           Utilization           9%           28%           34%           100%           0%           30%	Note(s)
Iodification: Project File: Module Name: Target Device: Product Version: No partition information was found.  Logic Utilization Number of Slice Filp Flops Number of Slices Containing only related I Number of Slices containing only related Io Number of Slices containing unrelated Io Number of Slices containing unrelated Io Number of Slices containing unrelated Io Number used as a route-thru Number of bonded IOBs Number of GCL Ke	modi.ise S_2D_CSDA_MST xc3s400-5fg320 ISE 9.1i MODI Par Device Util Used 1.239 IGC 0 2.158 2.048 2.048 1.239 Jojc 0 1.239 1.238 1.2	Current State: • Errors: • Warnings: • Updated: tition Summary ization Summary Available 7,168 7,168 3,584 1,239 1,239 1,239 7,168 221 8	Placed and Ro           No Errors           215 Wamings           Thu Dec 5 19:0           Utilization           9%           28%           100%           34%           100%           30%           85%           12%	uted 03:35 2013 Note(s)
Iodification: Project File: Module Name: Target Device: Product Version: No partition information was found.  Logic Utilization Number of Slice Filp Flops Number of Slices Containing only related Io Number of Slices containing only related Io Total Number of 4 input LUTs Number used as a route-thru Number of bonded IOBs Number of GCLKs	modi.ise	Current State: • Errors: • Warnings: • Updated: tition Summary ization Summary Available 7,168 7,168 7,168 1,239 1,239 1,239 7,168 221 8	Placed and Ro           No Errors           215 Warninots           Thu Dec 5 19:0           Thu Dec 5 19:0           Utilization           9%           28%           34%           100%           30%           30%           85%           12%	uted 03:35 2013 Note(s)

# **RTL Schematic:**

![](_page_11_Figure_6.jpeg)

Fig: 22: S\_2D\_CSDA\_MST

![](_page_12_Figure_2.jpeg)

# Fig: 23: CSDA\_MST\_2D with Transpose Memory

![](_page_12_Figure_4.jpeg)

Fig 24: Internal Schematic for 2D CSDA MST

![](_page_12_Figure_6.jpeg)

# Fig 25: RTL Schematic for S\_BUF

![](_page_12_Figure_8.jpeg)

Fig 26: RTL schematic View In Xilinx for Odd part & even part CSDA

![](_page_13_Figure_2.jpeg)

Fig: 27: Schematic view for S\_1D\_CSDA\_MST\_1 & S\_CSDA\_MST\_2

![](_page_13_Figure_4.jpeg)

Fig:28: Xilinx Schematic view for S\_2D\_CSDA\_MST

4.TECHNOLOGY SCHEMATIC VIEW:

![](_page_13_Picture_7.jpeg)

Fig: 29: ISE Schematic View (M.53d)-[S\_2d\_CSDA\_MST (RTL1)]

#### 5. CONCLUSION:

The CSDA-MST core can achieve high performance, with a high throughput rate and low-cost VLSI design, supporting MPEG-1/2/4, H.264, and VC-1 MSTs. By using the proposed CSDA method, the number of adders and MUXs in the MST core can be saved efficiently. Measured results show the CSDA-MST core with a throughput rate of 1.28 G-pels/s, which can support ( $4928 \times 2048@24$  Hz) digital cinema format with only 30 k logic gates. Because visual media technology has advanced rapidly, this approach will help meet the rising high-resolution specifications and future needs as well.

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