Multilevel Inverter

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Abstract

— Now a day's multilevel inverter is immerged as a very good area under research. Significant work has been carried out over Multi level inverter technology due to its high-power medium-voltage energy control and a lower Total Harmonic Distortion (THD). In this paper we have presented an overview of the multi level inverter topologies. From the discussion it is concluded that the H-bridge inverter topology is best because it produces least total harmonic distortion and lower dv/dt at the output.

Keywords: — *Multi level inverter, Total Harmonic Distortion (THD), H-bridge inverter.*

1. INTRODUCTION

In electrical power systems one of the major problems is the Harmonic contents. There are 2 types of harmonics present in an electrical system. These are Current harmonics and voltage harmonics. Both of these harmonics can be generated either by the load or source. Harmonics in the load can be generated due to nonlinear behavior of the electronic devices, such as converters, gas discharge lighting devices and arc-furnaces etc. Due to load harmonics overheating of the magnetic cores of transformer and motors can be seen. On the other hand power supply with non-sinusoidal voltage waveform., may give rise to source harmonics. The voltage harmonics in the power supply gives rise to the current harmonics and is dependent on load. The type of load may be resistive, capacitive or inductive. Current and voltage harmonics may lead to power losses and Electromagnetic Interference (EMI) in AC motor drives. To obtain the harmonic component it can be represented by the superposition of fundamental component. Then these components can be extracted by applying Fast Fourier Transform [FFT]. The frequency of each harmonic is the multiple of its fundamental frequency. To indicate the quantity of harmonic contents there are several methods such as: Selective Harmonic Elimination (SHE) Strategy, Artificial Neural Network (ANN), Total Harmonic Distortion (THD), etc. [1] Out of these methods THD method is most widely used. Mathematically the Total Harmonic Distortion is given by

$$\mathbf{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} H(n)^2}}{H_1}$$

2. RELATED WORK

Multilevel inverters generate stepped AC signals and thus overcome many of the limitations with the classical inverter circuit. Multilevel inverters use many number of switches and generate staircase type output through controlled switching of various switches. The sequence of switching and the duration of each step are very vital in minimizing the THD. The methods of generating gating signals are not unique. Many methods that are proposed in literatures make use of SPWM technique. Sinusoidal Pulse Width Modulation (SPWM) is a popular control method widely used in power electronic inverter circuit. It has advantages like low switching losses, the output has fewer harmonic and
method is easy to implement. The different SPWM methods are: (A) Phase Disposition PWM (PDPWM), (B) Phase Opposition Disposition PWM (PODPWM), (C) Alternative Opposition and Disposition PWM (APODPWM), (D) Phase Shift PWM (PSPWM), (E) Carrier Overlapping PWM (COPWM) and (F) Multi Carrier Sinusoidal Pulse Width Modulation with Variable Frequency (MCSPWMVF). All the above methods make use of many triangular signals, that are level shifted or phase shifted, and compare with a single sine wave to generate gating signals for the respective switches. The intersection of the sine signal with the
various triangular signals will generate the gating signals for the respective switches. In [2] a generalized gating signal generation method was proposed using only one modulating and one carrier signal. The signal so generated is steered into various switches through pulse steering circuit.

SPWM inverter technology uses the manner of digital control gradually by the development of embedded system, but the traditional development method of embedded system is linearized, a lot of time and effort is wasted. In [3], SPWM control model is created in MA TLAB with model-based design. The code of chip required is generated automatically after model is validated and revised. Development time is shortened greatly. The test is showed that the generated code line meet the actual needs, model-based design improves the efficiency of development and space of upgrading, suitable for the development of embedded system.

Voltage or current converters generate discrete output waveforms, which require large inductances connected in series with the respective load to generate the desired current waveform. Mostly, neither the voltage nor the current waveforms are as expected and also have distorted voltages and currents waveforms produces harmonic contamination, additional power losses, and high frequency noise. In [4] a method of minimization of THD with near to reference current generation is proposed based on multilevel inverter. A sinusoidal pulse width modulation scheme was developed for the multilevel inverter.

Many industrial applications require variable speed drives. In recent days many researchers have focused on Pulse Width Modulation (PWM) based multilevel inverter drives for inverter quality improvement. Inverter performances are evaluated by calculating overall THD of output signals. In [5] a new multilevel inverter topology is described with reduced number of switches. Different Sinusoidal PWM schemes (PD, POD, APOD) has been employed to the reduced switch inverter and a comparative performance is analyzed of the inverter in terms of Total Harmonic Distortion. The reduced switch multilevel inverter has been designed and different SPWM schemes have been developed in MATLAB SIMULINK environment.

3. INVERTER TOPOLOGIES

In recent years a number of industrial applications have started using high power apparatus. But, certain motor drives still required medium voltage (few MW) for their operation. For these applications it is not suitable to connect a power semiconductor switching device directly. Therefore in order to overcome this problem a multilevel inverter is introduced. A multilevel inverter also improves the quality of harmonics present in the output voltage. It can also achieve medium and high power ratings with the use of renewable sources such as Solar, wind and fossil fuels.

A multilevel inverter can produce an AC waveform of desired level with different DC levels. The magnitude of these DC voltages may be or may not be necessarily equal. The AC output voltage obtained at the output of inverter is like step size. Therefore, the main drawback of this type of inverter is that the stepped waveform is to be approximated to obtain the sinusoidal waveform. Due to the staircase nature of the output of inverter it has sharp transitions and these sharp transitions results in harmonics that is proved by Fourier series. [6]

During the last two decades a huge number of multilevel inverter topologies have been proposed.
Novel inverter topologies and unique modulation schemes has been evolved due to contemporary research. The three multilevel inverter topologies that have been widely used are:

Diode clamped /Neutral clamped Multilevel Inverter

Flying capacitors /Capacitor clamped Multilevel Inverter Cascaded H-bridge Multilevel Inverter

A. Diode-Clamped Inverter:

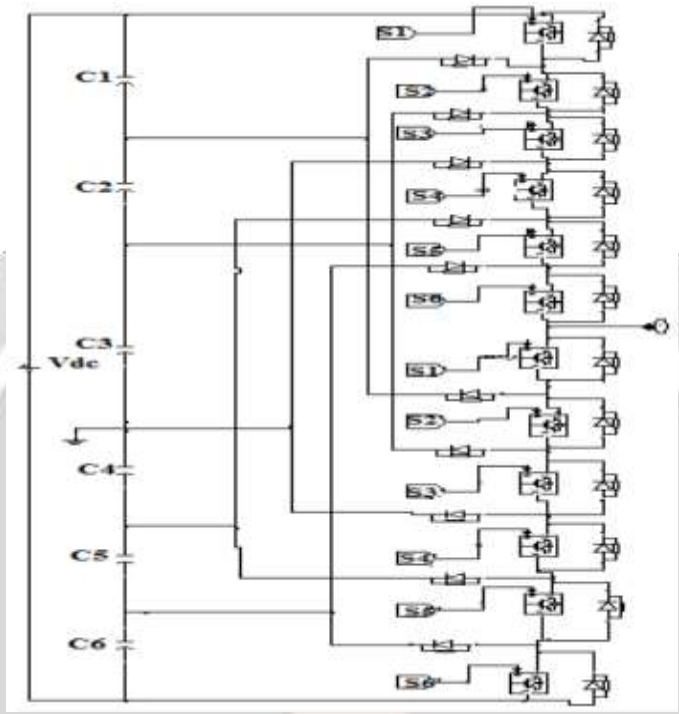

Fig 1: Diode - clamped 7 - level inverter power circuit [7]

S_1	S_2	S_3	S_4	S_5	S_6	S_1'	S_2'	S_3'	S_4'	S_5'	S_6'	V_{an}
1	1	1	1	1	1	0	0	0	0	0	0	$V_{dc}/2$
0	1	1	1	1	1	1	0	0	0	0	0	$V_{dc}/3$
0	0	1	1	1	1	1	1	0	0	0	0	$V_{dc}6$
0	0	0	1	1	1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	1	1	1	0	0	- $V_{dc}/6$
0	0	0	0	0	1	1	1	1	1	1	9	- $V_{dc}/3$
0	0	0	0	0	0	1	1	1	1	1	1	- $V_{dc}/2$

Table 1: Diode - clamped 7-level inverter switch states [7]

Fig. 1 shows the structure a 7 level diode clamped multilevel inverter. Only one phase leg is shown in order to obtain better clarity. Here, in this circuit the switches are connected in series and the DC power supply is connected across the capacitors and switches through clamp diodes. The clamp diodes are used here in order to block the current. Here, the number of phase voltage levels is proportional to the number of capacitors in each phase. The common point of the circuit i.e ground is connected in between DC link. In order to generate N voltage levels through a diode clamped inverter N-1 capacitors are required in the circuit. Therefore, in the 7 level inverter shown in Fig. 1 six capacitors: C1, C2, C3, C4, C5 & C6 are connected. If these

capacitors are connected across a DC voltage of magnitude Vdc then the capacitor voltages will be Vdc/6. The switching pattern of a 7 level inverter is shown in Table 1. Here a "Logic 1" indicates that the switch is ON and the "Logic 0" indicates an OFF condition. [7]

B. Flying capacitors /Capacitor clamped Multilevel Inverter:

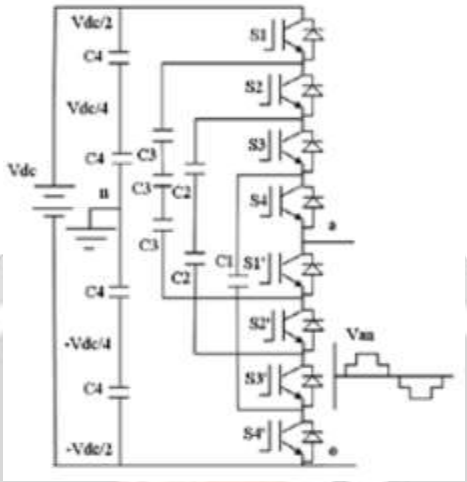

Figure 2: Capacitor Clamped Multilevel Inverter Circuit Topology [8]

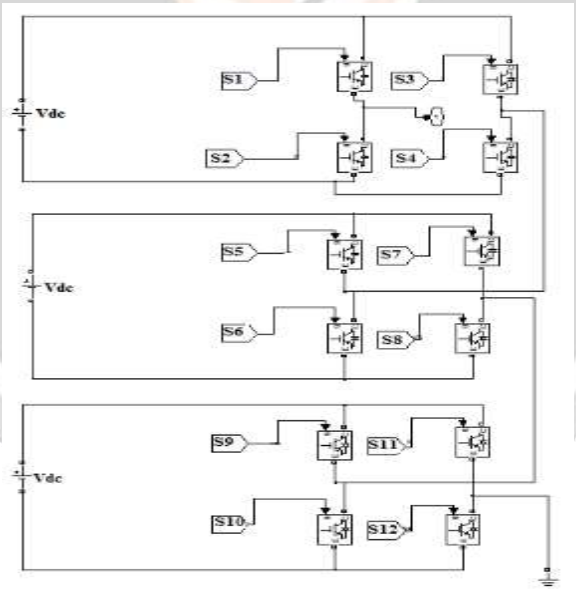

Fig 3: Cascaded H bridge 7 level power circuit [7]

Fig. 2 shows the structure of a Flying capacitor MLI. From the fig. it can be seen that the structure of FC MLI is similar to that of the diode clamped inverter with the exception that instead of using clamping diodes, the inverter utilizes capacitors.
Fig 2 shows a single phase n level configuration of the capacitor clamped inverter. A total of (n-1)×(n-2)/2 clamping capacitors per phase leg and (n-1) main DC bus capacitors will be required in an n level inverter. For an n level inverter the voltage levels and the arrangements of the flying capacitors in the FCI structure assures that the voltage stress across each main device is same and is equal to Vdc/(n-1). [8]

C. Cascaded H-bridge Multilevel Inverter:

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	V_{an}
1	0	0	1	1	0	0	1	1	0	0	1	$+3V_{dc}$
0	1	0	1	1	0	0	1	1	0	0	1	$+2V_{dc}$
0	1	0	1	0	1	0	1	1	0	0	1	$+V_{dc}$
0	1	0	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	1	0	$-V_{dc}$
1	0	0	1	0	1	1	0	0	1	1	0	$-2V_{dc}$
0	1	1	0	0	1	1	0	0	1	1	0	$-3V_{dc}$

Table 3: Cascaded H Bridge 7 level inverter switch states [7]

Fig. 3 shows the structure of a 7 level cascaded H bridge inverter. Only one phase leg is shown in order to obtain better clarity. Here, in this circuit the switches are connected in series and, the number of phase voltage levels is proportional to the number of cells. the number of phase voltage levels at the converter terminals is 12+N in this topology, where N is the number of cells or dc link voltages. Here, each cell has a different dc link Voltage that is same among the cells. The number of phase voltage levels is proportional to the number of dc link voltages. The common point shown in figure is referred to as ground. Each cell in H bridge may have either a negative, positive or zero voltage. [7]

4. CONCLUSION

In this paper multi level inverter topologies are described briefly along with their control strategies. This would help researchers to apply proper techniques to control the inverter. From the research we can conclude that the H-bridge inverter is most suitable due to its low harmonic contents and THD.

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