PWM Series Capacitor High Conversion Ratio DC-DC CONVERTER

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ABSTRACT

In this letter, an asymmetrical pulse width modulated (PWM) scheme is proposed to solve the inductor current unbalance and nonlinear voltage gain issues of the series-capacitor (SC) high-conversion-ratio (HCR) converter when D > 0.5. With the proposed scheme, the converter can achieve both current balancing and high step-down conversion even for D > 0.5. As a result, combined with the conventional PWM scheme, the duty cycle limitation of the SC-HCR converter is completely eliminated. A 2-kW prototype SC-HCR converter was fabricated and tested to validate the performance of the proposed PWM scheme.

Keyword: - *Asymmetrical pulse width modulated (PWM)1, buck converter2, high conversion ratio (HCR)3, interleaved4, series capacitor (SC)5.*

1.INTRODUCTION

The two-phase interleaved buck converter (IBC) shown in Fig.1 is widely used in many industrial applications where a large output current is demanded. However, it is well known that the IBC suffers from unbalanced inductor currents (iL1, iL2) when there is a small mismatch in the gate signals. In addition, the converter duty ratio (D) becomes extremely small, and the voltage stress for all semiconductor devices is equal to supply voltage.

1.1Working of the proposed system

In order to overcome the shortcomings of the conventional IBC, a series capacitor, (double step down) high conversion ratio (HCR) shown in Fig.2 was introduced. In a modified SC-HCR converter was introduced to solve the start-up issue of the SC-HCR converter, and the same structure was extended to the dual-active-bridge converter and voltage balancer. The SC-HCR converter can achieve high step-down function and its voltage gain is half of the conventional IBC.

Whereas, for IBC i.e., $\frac{V_0}{V_{in}} = D^2$ and for SC HCR i.e.,= $\frac{V_o}{V_{in}} = \frac{D}{2}$.

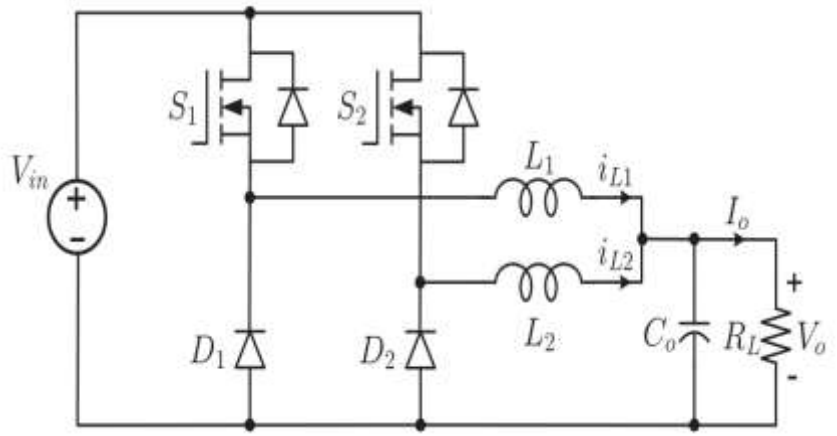


Fig .1 Two-phase IBC

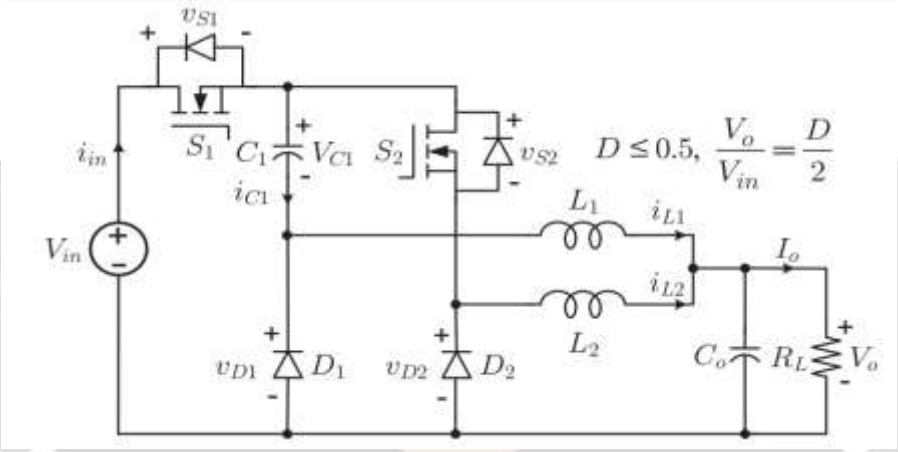


Fig.2 SC high-conversion-ratio converter in [3]

Moreover, owing to (IBC) the charge balance condition on the capacitor C1, the two inductor currents are balanced automatically. However, the mentioned merits only hold when D ≤ 0.5 and they are lost when D > 0.5. As will be explained in Section III, when D > 0.5, the two inductor currents no longer balanced. This letter proposes an asymmetrical PWM scheme for the SC-HCR converter. With the proposed PWM scheme, the two inductor currents (iL1, iL2) continue to balance, and the voltage gain of converter does not change and maintains D/2 even with D > 0.5. The new PWM scheme is verified through both simulation and experiment with a 5-kW prototype converter.

2. PWM ASYMMETRICAL PWM SCHEME

Fig. 3(a) and (b) shows the conventional PWM scheme for the SC-HCR converter. The gate signals of S1 and S2 have the same duty ratio D and they are phase-shifted by 180° for interleaving. As shown, when D ≤ 0.5 [see Fig. 3(a)], the two

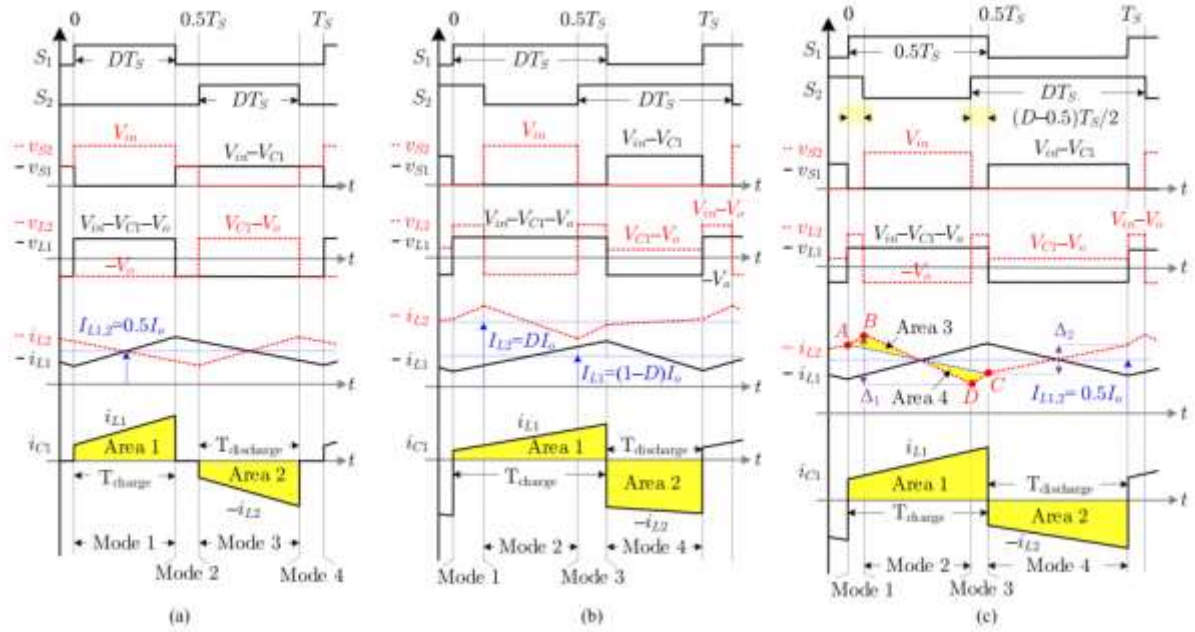


Fig. 3 Key waveforms of the SC-HCR converter with different PWM schemes. (a) Conventional PWM scheme when *D* ≤ 0.5. (b) Conventional PWM scheme when*D* >0.5. (c) Proposed asymmetrical PWM scheme when*D* >0.5.

inductor currents are well balanced. However, when D > 0.5 [see Fig. 3(b)], they are not balanced, and the average inductor currents (IL1, IL2) are related to D (this will be explained in Section III-B). Fig. 3(c) shows the proposed PWM scheme. In the proposed PWM scheme, duty ratios of switch S1 and S2 are not equal. As shown in Fig. 3(c), duty ratio of S2 is equal to that of the conventional PWM scheme, while duty ratio of S1 is set to 0.5. Operation of the converter with the proposed PWM scheme is depicted in Fig. 4 and detailed analysis is explained as follows.

1) *Mode 1* [see Fig. 4(a)]: S1 and S2 are both turned-ON, whereas D1 and D2 are turned-OFF. The two inductors are charged and the sum of the two inductor currents (iL1, iL2) flows through the switch S1. The capacitor C1 is charged and its current is equal to iL1.

2) *Mode 2* [see Fig. 4(b)]: S2 is turned-OFF, thus, iL2 freewheels through D2. S1 is kept ON, thus, the capacitor C1 and L1 continue to charge by iL1. In this mode, the switch S2 voltage (vS2) is equal to Vin.

3) *Mode 3*: S2 is turned-ON again, thus, this mode is the same as mode 1.

4) *Mode 4* [see Fig. 4(c)]: S2 maintains ON. S1 is turnedOFF and iL1 freewheels through D1. At the same time, the capacitor C1 is discharged through S2 and D1. Thus, the capacitor C1 current is equal to (−iL2). In this mode, the current through D1 is sum of the two inductor currents (or output current), while the switch S1 voltage (vS1) is equal to (Vin − VC1). The voltage on the inductor L2 (vL2) is equal to (VC1 − Vo) and it becomes positive when D ≤ (2/3) and negative when D > (2/3), respectively.

3. CHARACTERISTICS OF THE SC-HCR CONVERTER WITH THE PROPOSED AND CONVENTIONAL PWM SCHEMES

3.1 Voltage Gain

From the switch S2 voltage (vS2) waveform in Fig. 3(c), the average value of vS2 is (1 − D)Vin. In addition, by using the flux (volt–sec) balance condition on L1 and L2 in the loop 1 in Fig. 5, the average value of vS2 is equal to VC1. Therefore, following can be obtained:

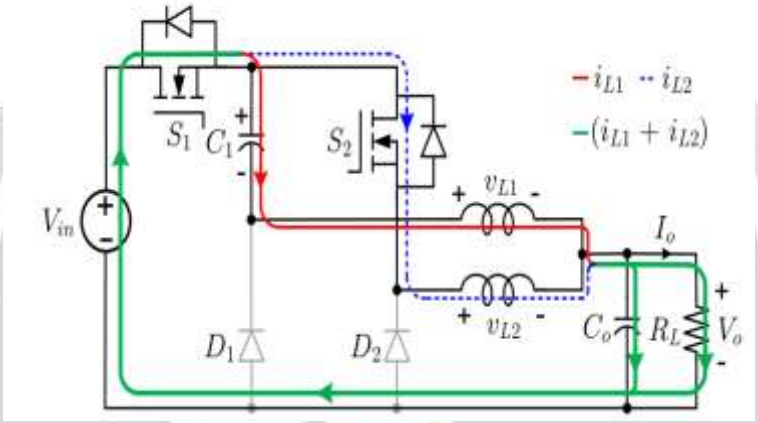
$$VC1 = (1 - D)\,Vin \qquad (1)$$

Similarly, by using the flux balance condition on L1 in Fig. 3(c), following can be obtained:

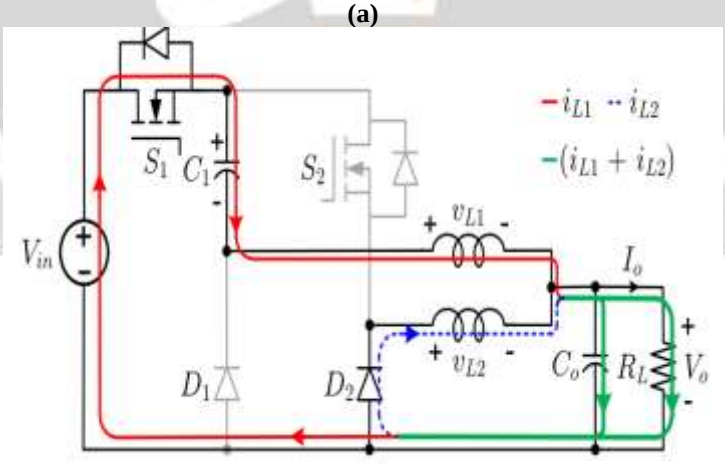
$$Vo = 0.5\,(Vin - VC1). \qquad (2)$$

3.2 Inductor Currents Balancing

With the proposed scheme, as shown in Fig. 3(c), the time intervals of modes 1 and 3 are equal. Also, the lines AB and CD have the same slope as (Vin − Vo)/L2. Thus, the areas 3 and 4 are the same. As a result, the inductor current iL2 has the same average values during the charging (Tcharge) and discharging (Tdischarge) times of C1. In addition, the two areas [areas 1 and 2 in Fig. 3(c)]

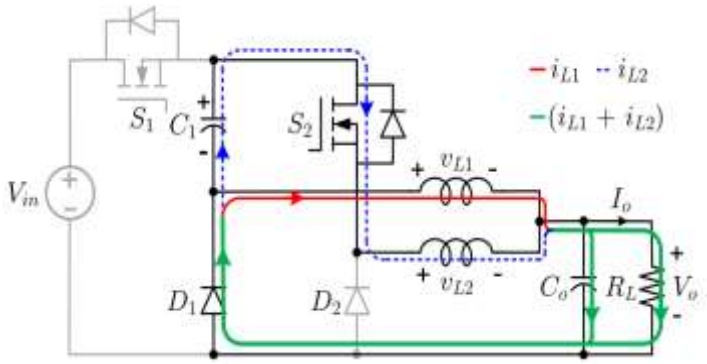


(a)



(b)

in the capacitor current must be the same due to the charge (amp–sec) balance condition on C1. Therefore, the two inductor average currents have the following relationship:



(C)

3.3 Switch Voltage and Current Stresses

The comparison of the conventional and proposed scheme is summarized in Table I. In both schemes, when $D > 0.5$, the voltage stresses of $S2$ and $D2$ are equal to Vin, whereas the voltage stresses of $S1$ and $D1$ are equal to $D\,Vin$. The current stresses of $S1$ and $D1$ are equal to the output current (Io). However, in the proposed scheme, thanks to the inductor currents balancing, the current stresses of $S2$ and $D2$ are reduced from DIo to $0.5Io$.

The input rms current (I.rms) is also reduced. shows the voltage and current waveforms of semiconductor devices when $D \leq 0.5$ and shows the same waveforms when $D > 0.5$ with the proposed scheme. The detailed comparison under the same output voltage is summarized in Table II. As shown, except for the rms currents of $S1$ and $S2$, almost values are reduced when the proposed PWM scheme is applied for $D > 0.5$. The voltage stresses of $S1$, $S2$, and $D1$ are reduced when $D > 0.5$, whereas the maximum value of $D2$ ($vD2$) is $4Vo$, which is equal to the value at $D = 0.25$. When $D > 0.5$, the voltage stress of $D2$ ($2Vo/D$) decreases when D increases. In addition, the diode average current ($iD2$.avg) reduces when $D > 0.5$, which leads to reduced diode conduction loss.

4. SIMULATION RESULTS

A 2-kW prototype of the SC-HCR converter was fabricated with the design parameters Fig.5 show the experimental results with the proposed PWM scheme at full-load (Vin = 250 V, Vo = 100 V, and D = 0.8).

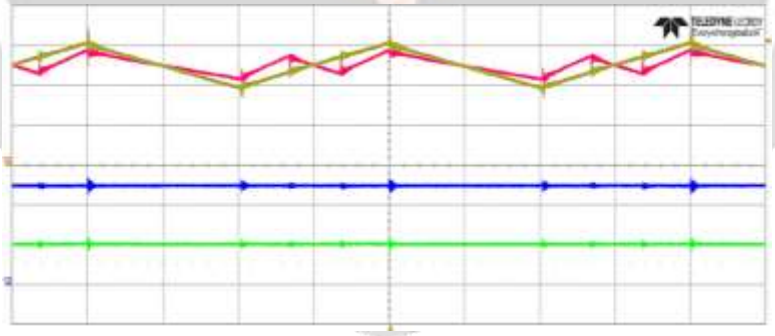


Fig .5

As shown in Fig. 5, the voltage stresses of $S1$ and $D1$ are equal to $D\,V$in (or Vin − $VC1$), whereas the voltage stresses of $S2$ and $D2$ are equal to the input voltage. Fig.5 shows the input voltage, output voltage, and two inductor currents. Similar to the simulation results, the two inductor currents are well balanced and equally share the output current. In both conditions, the two inductor currents also share the output current, and they are well balanced as expected.

5. CONCLUSION

In this letter, an asymmetrical PWM scheme applied for $D > 0.5$ has been proposed for the SC-HCR converter. The proposed scheme has the following advantages over the conventional PWM scheme .

1) The two inductor currents can continue to balance even When $D > 0.5$.
2) Unlike the conventional scheme having the voltage gain of $D2$ when $D > 0.5$, the proposed scheme can maintain the same voltage gain (i.e., $D/2$) as when $D \leq 0.5$.
3) The current stresses of switch $S2$ and $D2$ are reduced.

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