SPEED AND AREA EFFICIENT VLSI ARCHITECTURE FOR MPSK MODEMS

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ABSTRACT

M-PSK (M-ary Phase Shift Keying) designs are used in the field of satellite correspondence, because they offer higher pace of information exchange limit and has power capable differentiated and distinctive plans. This paper exhibits the designs for M-PSK structures; for M=4, 8, 16 using Very large scale Composed circuit (VLSI) plans. The proposed MODEMs make an effort not to use any multipliers as compared to the old methods; therefore making the proposed systems to perform faster also making it area efficient system. Also this paper puts forward certain demodulation computations that are perceptible in straightforward as well as in automated zones. The modeling of presented MPSK MODEM structures is here done using Verilog language and finally checked for validation on "Xilinx ISE 14.6" software. The simulation output affirms their utilitarian authenticity and the Implementation result of the proposed structures exhibit their suitability for satellite communication applications.

Keywords: - *MPSK- QPSK, 8PSK, 16PSK MODEMs, VLSI Architecture, Xilinx ISE 14.6*

1. INTRODUCTION

The digital Modulation schemes have increased its significance in contrast to the Analog modulation schemes in the present era due to numerous preferences, for example, better clamor execution, more prominent security and simpler usage in large scale incorporated circuits. For satellite applications, M-PSK computerized tweak plans are progressively utilized as they are more data transfer capacity productive, control effective and have a sensible receiver complex quality.

M-PSK, as the name tells, the phase of carrier signal is differed for every incoming pattern. Most of the previously proposed designs for QPSK MODEMS comprised of multipliers, which involved substantial space, adding to large delay in the way between input and output on the integrated circuit thereby diminishing the performance speed.

The specialty of the modems presented in this paper is, they don't use multipliers consequently giving elite w.r.t speed as well as space occupied. The initiated QPSK modems, frame the principal segment for outlining 8 and 16 PSK structures.

Earlier, Researchers have proposed a design for QPSK modems that doesn't use multipliers using CORDIC module approach. The CORDIC approach offered desirable Phase determination however the equipment is complex in nature, in contrast with modulators utilizing look into table (LUT) method. Therefore we make use of LUT method which significantly needs minimum equipment spacing without trading off in faster performance. Also, this paper shows calculations for 8PSK and 16PSK frameworks based upon the approach proposed in 32-APSK system in [1]; which can be designed both in Analog and digital areas.

2. PROPOSED METHODOLOGY

2.1 Quadrature (or M=4) Phase Shift Keying MODEM.

QPSK Modulation:

Fig1 shows the implementations of QPSK modulator. The approaching input bits are sent into a S2P convertor giving bits B [1:0] or B [0], B [1]. The combination of bits, also called as symbol can be called as constellation point in the "constellation diagram". The mapper as shown in the diagram scales the constellation bits to the desired specific points. The function of the constellation mapper is same for all the modulators. At any instant, for a specific

information pattern, the memory location of Read Only Memory should be altered which should also cause the phase of the carrier to be modified, for the respective constellation point. This condition can be satisfied by using a 3 bit adder. The MSB from the counter yield and a CONCAT bit is the quantity given to the adder which is as shown in the figure. The procedure of modulation can be summarized as: For instance, for an input pattern '00' there ought to be a change in Φ=45. Here 'Φ' denotes phase angle. The counter that is up counting ("0 to 255"), must see that the ROM address is altered in like manner with the end goal that, there is a similar alter in "Φ" of the carrier signal at yield of Digital to Analog Convertor. Therefore this same procedure is carried out for all the input bit patterns.

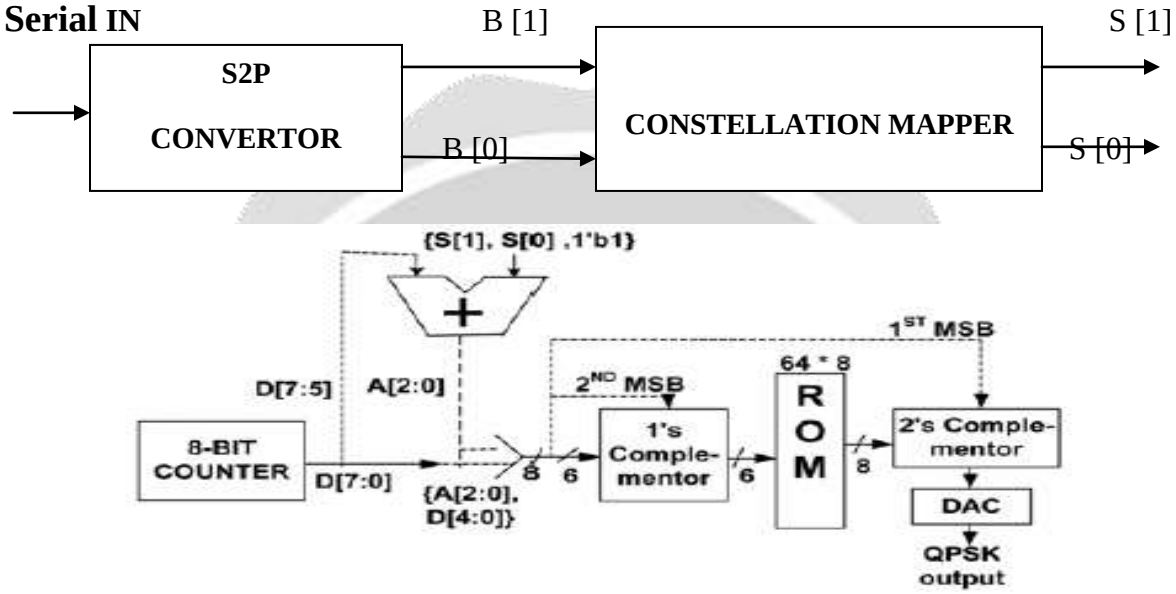

Fig1. Modulator with Phase = Π/2.

Assume that Tcm = 'Delay w.r.t the mapper module, T_{adder} = adder delay, T_{rom} = latency to access the content from ROM. The "critical time delay'' (T) is:

$$T = T_{cm} + T_{adder} + T_{rom}$$

This critical delay (T) can be minimized by placing a register in front of the ROM. Thus the above equation can be re-written as:

$$T = T_{cm} + T_{adder,\ Trom}$$

This delay is insignificant when differentiated and the essential delay is obtained from analog modulator. The critical delay can further be minimized by reducing latency of ROM. Fig 1 shows the 4PSK modulator consisting π/2 radian of carrier signal, set away in ROM.As a result, decreasing the memory zone to $1/4^{th}$ as compared to the modulator with 2 π carrier. Now as opposed to samples of 256, the amount of tests has dropped down to samples of 64. By doing this we get greater scope to increase the performance also Noise of various range can be minimized by employing the methods as proposed in [2].

QPSK Demodulation:

In the case of Demodulation, let us assume S (t) is the signal obtained from the modulator and let B[1:0] be the bits that has to be recovered at the output of QPSK Demodulator . For Analog domain to obtain demodulated signal the steps are as follows:

1. Calculate

$$Ik = \int_0^{2\pi} S(t)\, A\cos(wt)\, d(wt)$$

$$Qk = -\int_0^{2\pi} S(t)\, A\sin(wt)\, d(wt) \quad \} \rightarrow 1$$

2. De-mapping

B [1] = 1 if (Ik <= 0); 0= otherwise.
B [0] = 1 if (Qk <= 0); 0= otherwise.

The VLSI usage of the given calculation is examined below. As the algorithm depends on coherent recognition method, we expect that the carrier signal is promptly accessible at the recipient side. Subsequently, the needed carrier i.e., A cos (2πfct) and −A sin (2πfct) can be stored in COS-ROM and SIN-ROM, individually.

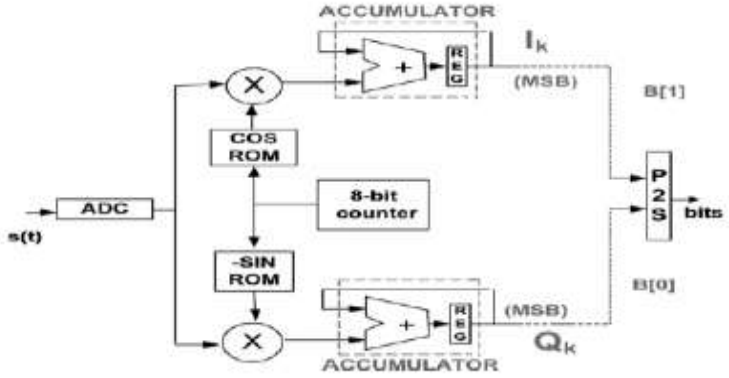

Fig 2 QPSK DEMODULATOR

The accumulator output are I_k and Q_k ; which can written as :

$$I_k = \sum_{n=0}^{255} s\left(\frac{n}{f_s}\right) A \cos\left(2\pi f_c\left(\frac{n}{f_s}\right)\right)$$

$$Q_k = -\sum_{n=0}^{255} s\left(\frac{n}{f_s}\right) A \sin\left(2\pi f_c\left(\frac{n}{f_s}\right)\right)$$

Thus the required output is recovered at the output of Parallel to serial convertor (P2S). Here Pipelined architecture is used which reduces the area occupied thus reducing the critical path delay and increasing the speed of performance.

2.2 8PSK MODEM

8PSK Modulation:

Fig 3 shows the implementation design of modulator for (M=8) PSK. The entire working of 8 PSK modulator is very similar to that of the 4 PSK modulator; additional is that we are considering extra 4 symbols(4,5,6,7) in constellation diagram as the name suggests it is 8 PSK i.e (m=8; 0,1,2,3,4,5,6,7). The first 4 symbols (0, 1, 2,3) are already explained in QPSK section. Now for the rest of the 4 symbols, MSB is checked and entire constellation is shifted with a phase angle 45 degrees; where 45degree is equal to decimal number 32 in ROM address location.

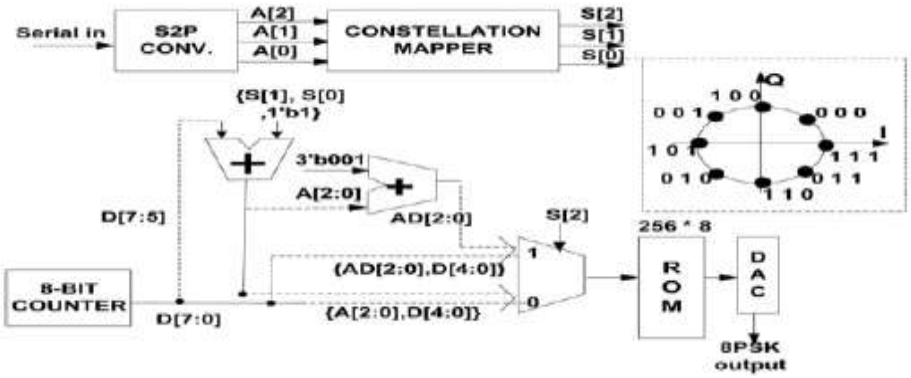

Fig 3: Modulator -8PSK.

Here the architecture also consists of extra 8bit 0adder to add d=32. The 8 PSK's critical path delay is given by:

$$T_{\text{critical path delay}} = T_{cm} + 2T_{adder} + T_{rom} + T_{mux}$$

Where Tmux is the delay caused by the multiplexer. Thus to remove this delay we go for pipelining; this can be done by putting 2 registers at the yield of adder and in front of ROM. Now the delay reduced can be written as:

$$T_{\text{critical path delay}} = \max (Tcm + T_{adder}, T_{mux} + T_{adder}, T_{rom})$$

8PSK Demodulation:

The operation of 8 PSK Demodulation is similar to QPSK demodulation with additional processing steps that contains multiplication, addition, subtraction and shift operations that can be explained by the algorithm.
The sequence of steps that happens inside the 8 PSK demodulator is shown below

Iteration1: calculation of

$$Ik = \int_0^{2\pi} S(t) A\cos(2\pi fct) d(2\pi fct)$$
$$Qk = -\int_0^{2\pi} S(t) A\sin(2\pi fct) d(2\pi fct)$$

Iteration2: calculation of

l1=2Ik-Qk
l2=Ik+2Qk
l3=Ik-2Qk
l4=2Ik+Qk

Iteration3: De mapping

B [2] =1 if {l3 ≤ 0 & l4> 0 and vice versa
B [1] =1 if l1≤ 0
B [0] = 1 if l2 > 0; else 0

The proposed design for Demodulation using 8 PSK is depicted in fig 4

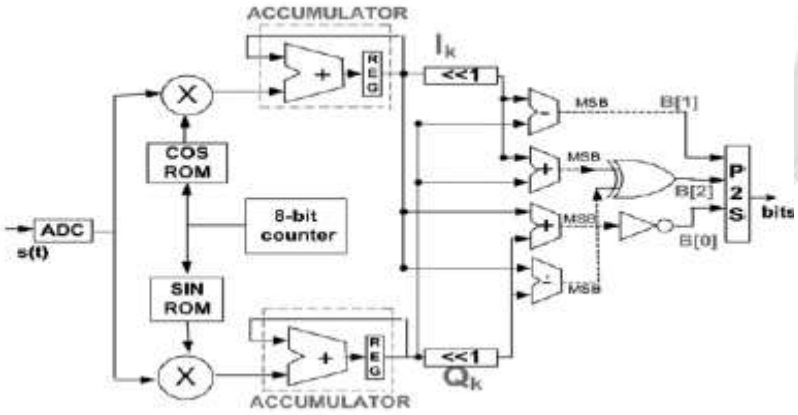

Fig 4 Demodulator of 8PSK

2.3 16PSK MODEM

16PSK Modulation:

Fig.4 shows the implementation design of Modulator for (M=16) PSK. The task of Constellation mapper is as explained for QPSK.

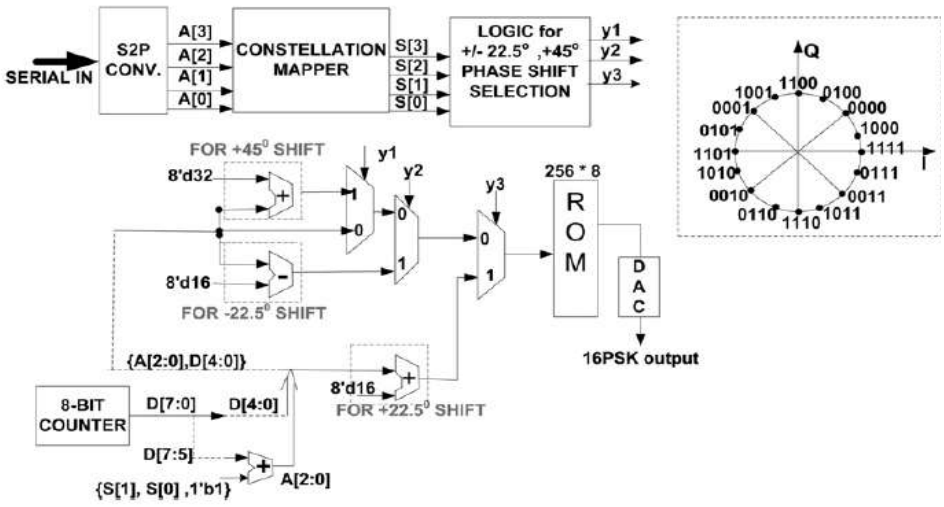

Fig5. 16 PSK Modulator.

Considering the constellation points at bits 0, 1 2 and 3. Disregarding first 2 MSBs, would straightforwardly speak to constellation points of QPSK. Therefore the same design methodology of QPSK modulator can be used here for first four bits (0, 1, 2,3).Unlike 8PSK we first rotate QPSK by phase angel +22.5 degree that is proportional to including +16 to memory location of Read Only Memory of modulator of 4PSK for bits 4,5,6,7. This is as depicted in Fig.5 Now; QPSK constellation is rotated by phase angle −22.5° that is proportional to deducting -16 from memory location of 4PSK modulator for next 4 bits. Now we utilize 8-bit subtractor as depicted in the figure. Now for remaining 4 bits we pivot the QPSK with a phase angle of 45 degree that is identical to including +32 to Memory location. In each of the above mentioned cases the select flags to the multiplexer will be four bits each respectively.

16 PSK Demodulator

In this section the demodulation calculations for 16APSK that is derived from 32APSK framework is introduced. The fig6 shows the representation for 32 APSK constellations. The 32A PSK as shown above comprises of 3 circular bands represented as R1, R2, and R3 individually. Circular band R3 specifically belongs to 16PSK frame.

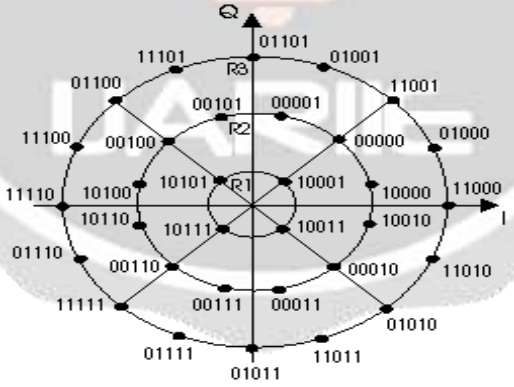

Fig 6 Constellation representation of 32 APSK

Earlier some authors have put forth calculations for 32APSK system [1]**.** From these calculations we particularly have chosen conditions that identify patterns on band R3 giving rise to computations to demodulate 16PSK. As Shown in fig 7, S(t) is the input given to the demodulator received from 16 PSK modulator. Let B[3:0] be the output symbol.

The sequence of calculation for 16PSK is shown below

Iteration1. calculate

$$Ik = \int_0^{2\pi} S(t)\, Acos(wt) d(wt)$$

$$Qk = -\int_0^{2\pi} S(t)\, Asin(wt) d(wt)$$

Iteration2. calculate

$$K1 = QK - IKtan\left(\frac{3\pi}{16}\right)$$

$$K2 = QK + IK \tan(5\pi/16)$$

$$K3 = QK + IK \tan(\pi/16)$$

$$K4 = QK - IK \tan(7\pi/16)$$

$$K5 = QK - IK \tan(\pi/16)$$

$$K6 = QK + IK \tan(3\pi/16)$$

$$K8 = QK + IK \tan(7\pi/16)$$

$$K9 = QK - IK \tan(5\pi/16)$$

Iteration 3: De Mapping

B [3] =1 if {K5, K2, K9 ≤ 0 & K6 K8, K1> 0 respectively
&
{K5, K2, K9> 0 & K6, K8, K1 ≤ 0 respectively
Otherwise 0

B [2] =1 if K4 ≤ 0 otherwise 0

B [1] =1 if K3 ≤ 0 otherwise 0

B [0] =1 if {K1, K2 ≤ 0, K1, K2 > 0 otherwise 0

The VLSI Implementations of 16 PSK using Pipeline strategy is depicted in fig7

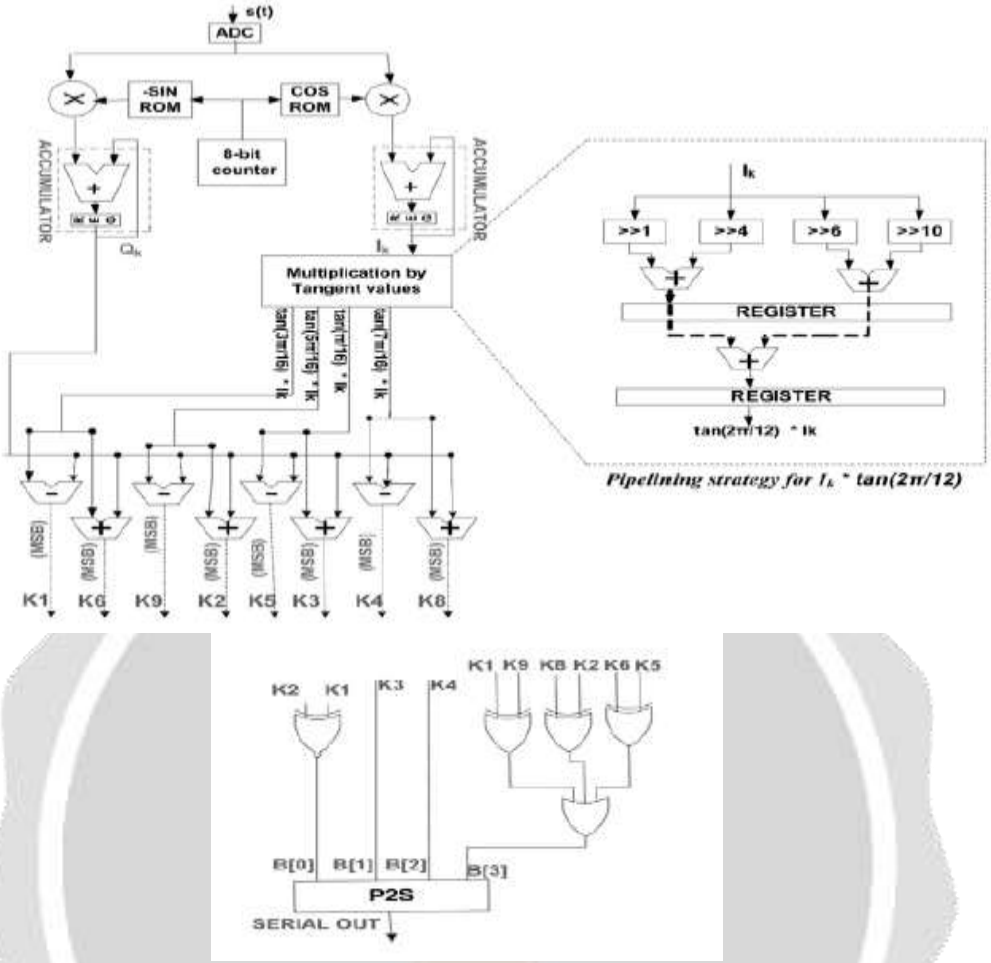

Fig7. 16PSK DEMODULATOR

3 CONCLUSIONS

MPSK MODEMS that are used in today's silicon technology for the application of Satellite communication is finally designed using VLSI architectures, modeled in Verilog language and checked for validation using "Xilinx ISE" 14.6 software as explained in this paper.

This Paper has presented multiplier less Modulators and Demodulators thus making this approach area efficient implementation.

This proposed architecture also has the advantage of high performance by using the pipeline strategy in the implementation which also assures higher throughput.

Digitally employable calculations with VLSI models are shown in this paper.

4. REFERENCES

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