SIMULATION OF ENHANCED PHASE-SHIFTED PWM CARRIER DISPOSITION FOR INTERLEAVEDVOLTAGE-SOURCE INVERTERS

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ABSTRACT

This a novel implementation of pulse width modulation that improves the quality of the line-to-line output voltages in interleaved multiphase voltage-source inverters(VSIs). In multiphase VSIs with n interleaved parallel-connected legs, the best single-phase output voltage is achieved when the carriers are evenly phase shifted. However, switching among non adjacent levels can be observed at regular intervals in the line-to-line voltages, causing bad harmonic performance. With the proposed method, switching in the line-to-line voltages happens exclusively between adjacent levels. The modulator utilizes two sets of n evenly phase-shifted carriers that are dynamically allocated. Because of its generality, the proposed implementation is valid for any number of phases and any number of legs in parallel. A MATLAB/Simulink model has been set up for simulation purposes. Selected experimental results obtained from a three-phase VSI made up with two and three legs in parallel per phase are reported, confirming the enhancement attained with the proposed implementation.

Keywords : *Interleaving, legs connected in parallel, pulse width modulation, voltage-source inverter (VSI).*

INTRODUCTION

Voltage-Source inverters (VSIs) with legs connected in parallel are widely used when high output currents are to be achieved, thus increasing the overall output power .Inductors are the passive components used to connect several phase legs in parallel. They not only limit circulating currents among the phase legs, but also qualify for averaging the voltage from the legs to form the output voltage. If interleaving is used, the Thevenin equivalent output voltage of a phase with n legs connected in parallel has $n + 1$ levels because of the averaging effect Different methods to set the instantaneous output voltage level can be used, including space vector modulation (SVM) or carrier-based pulse-width modulation (CB-PWM). The effect on their harmonic spectra has been largely investigated .In CB-PWM, the use of as many carriers as legs are connected in parallel is the standard procedure if interleaving is to be implemented .In an interleaved phase-shifted PWM (PS-PWM)scheme, all the carriers have the same frequency and amplitude(usually ranging from -1 to $+ 1$ per unit) and are evenly phase shifted within a switching period. Each carrier is associated with a specific leg. In level-shifted PWM (LS-PWM) schemes, n triangular carriers with the same frequency and $2/n$ peak-to-peak value are arranged in contiguous zones to fully occupy the range from -1 to $+ 1$. Depending on the relative phase relationship among the carriers, different PWM strategies are commonly referenced. The most popular one is phase-disposition PWM(PD-PWM)].In multilevel inverters, a PD-PWM scheme provides line-to line voltages where switching happens only between adjacent levels. However, LS-PWM techniques, such as PD-PWM, cannot be applied without modification in converters with legs connected in parallel. If each carrier were associated with one leg, only the leg associated with the carrier in the zone where the reference signal was would be switching. The remaining $n - 1$legswould be clamped to either the positive or the negative dc link voltage, depending on the relative position of their reference signal. This process would create dc-voltage components across the inductors and produce extremely large circulating currents. This letter proposes a new PS-PWM implementation for interleaved multiphase VSIs, where switching in the line-to-line voltages happens

exclusively between adjacent levels. As a consequence, the proposed modulator improves the quality of the line-to-line output voltages when compared to the conventional PS-PWM implementation. For a VSI with *n* legs in parallel ,the modulator utilizes two sets of *n* evenly phase-shifted carriers that are dynamically allocated. Because of its generality ,the proposed implementation can be applied to VSIs with any number of phases and any number of legs connected in parallel.

II. INTERLEAVED PS-PWM

The interleaving technique is applied to VSIs with legs in parallel to achieve an apparent switching frequency *n* times higher than the individual switching frequency of each leg .When operating with a CB-PWM, this is achieved by using *n*evenly phase-shifted carriers. Since there are *n* legs connected in parallel per phase, the Thevenin-equivalent output voltage of the *y*-phase becomes

$$v_y = \frac{1}{n}\sum_{x=1}^{n} v_{yx} \qquad (1)$$

due to the averaging effect of the parallel connection. The equivalent line-to-line voltage is the difference between the equivalent output voltage of two phases.Fig. 2(a) illustrates the case of a three-phase VSI with three legs in parallel per phase. The phase angles for the three carriers used (*vc*11, *vc*12, and *vc*13) are 0°, 120°, and 240°, respectively. The reference signals (*v*ref*a* , *v*ref*b*, and *v*ref*c*) are compared to their respective carrier signal to set the ON–OFF state of the switches. In order to further extend the range of the linear modulation index (*ma*) up to 1.15, the offset voltage

$$V_{offset} = -\frac{\max(V_{refa}, V_{refb}, V_{ref\_c}) + \min(V_{refa}, V_{refb}, V_{refc})}{2} \qquad (2)$$

is added as a zero sequence component to the three-phase references. The same equivalent output voltages as if centered SVM was used are obtained .Although the use of a set of evenly shifted carriers yields the best attainable single-phase output voltage in terms of THD ,that is not the case for line-to-line output voltages .From the equivalent line-to-line voltage in Fig. 2(a), it can be observed that during certain intervals, there is switching among three adjacent levels, thus worsening the overall THD and with negative implications in terms of electromagnetic interference on account of bigger voltage steps. The use of a different, but also evenly phase shifted, set of carriers does not fix that. But if two different sets of carriers are used to modulate two different phases, the periods of time where three-level switching in the line-to-line voltages is observed vary. Fig. 2(b) depicts the

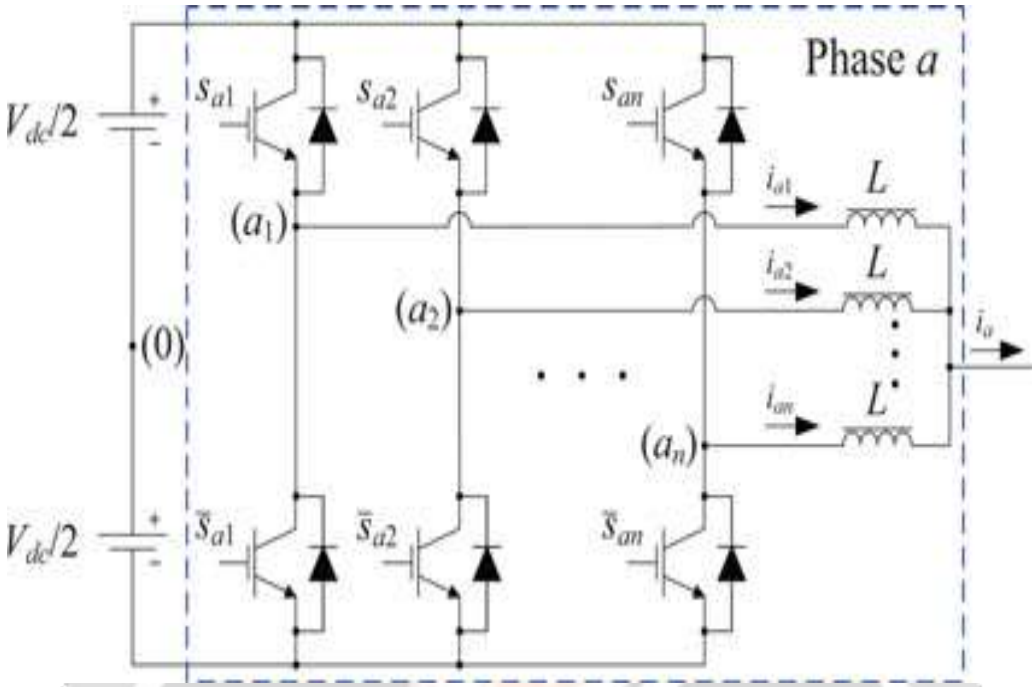

Fig: 1 One phase of a VSI incorporating n legs connected in parallel.

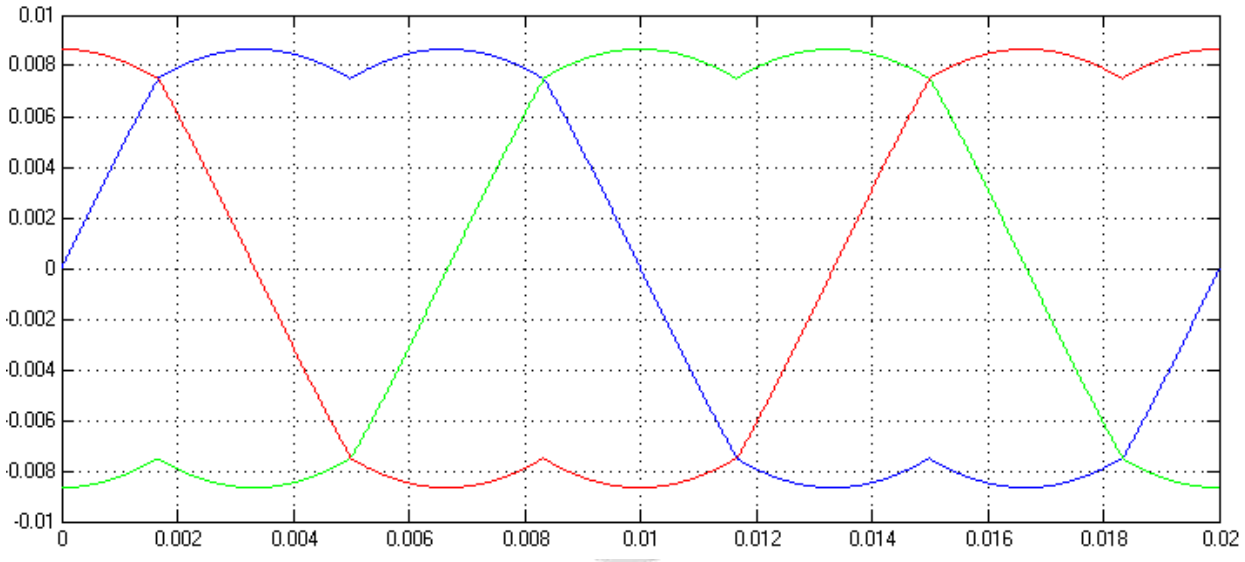

Fig. 2. Voltage references, set of carriers, and Thevenin-equivalent line-toline output voltage (*vab*) for a three-phase VSI with three legs connected in parallel for *ma* = 0.8 and *fc* = 800 Hz: (a) one set of carriers

results obtained for the aforementioned VSI if *vrefa* is modulated by means of the first set of carriers, i.e., *vc*11, *vc*12, and*vc*13, and *vref b* is modulated by means of a second set of carriers, i.e., *vc*21, *vc*22, and *vc*23, whose respective angle phases are 60°,180°, and 300°.On scrutinizing the examples shown in Fig. 2, one can conclude that those intervals of two-level and three-level switching, when using one or another set of carriers, are fully complementary .As a consequence, line-to-line output voltages with

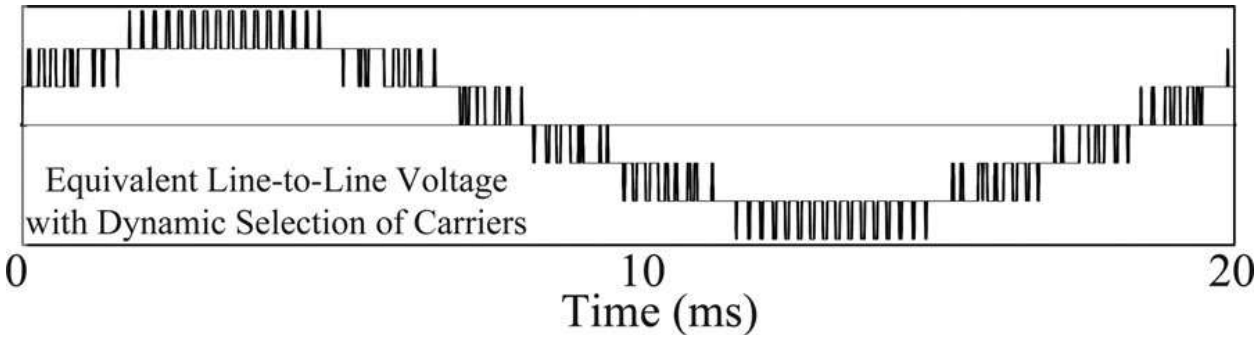

Fig. 3. Line-to-line voltage waveform for a three-phase VSI with three legs in parallel per phase achieved when using a dynamic assignment of carriers.

switching only happening between adjacent levels are achievable with a dynamic selection of the appropriate set of carriers, as can be seen in Fig. 3.

III. ENHANCED MODULATOR

The new modulator requires the use of two sets of carriers.For the general case of *n* legs connected in parallel per phase, carrier Set 1 is made up of *n* phase-shifted carriers (*vc*1, *vc*2,. . . , and *vc*1*n*) with a relative phase shift of 360◦/*n*. A second set of carriers (*vc*21, *vc*22, . . . , and *vc*2*n*)—Set 2—is also evenly phase shifted, but the whole set is phase shifted by 360◦/(2*n*)with regards to Set 1. Table I shows the relative phase shifting among the carriers. The phase shift depends on the number of carriers, i.e., the number of legs in parallel. The carrier set selection is dynamically assessed depending on the instantaneous value of the modulating reference signals (*v*ref*a* , *v*ref*b*, . . . , and *v*ref*m*). For that purpose, and considering a linear-modulation operation, the carrier/reference signal domain (which ranges from −1 to +1) is broken down into *n* equally sized zones of 2/*n* peak-to-peak value that are numbered upwards, as it is shown in Fig. 4. In order to quantize them, the following expression is used:

$$z_{ref\,y} = 1 + \left[\frac{1+v_{ref\,y}}{\frac{2}{n}}\right], \quad \text{for y} = \{\text{a, b, ... m}\} \tag{3}$$

where *z*ref *y* variables can take values from 1 to *n*.

Fig. 5 shows a block diagram of the proposed modulator for*m* phases and *n* legs per phase. The modulators for each phase useeither Set 1 or Set 2 depending on the position of their reference signals. The even/odd zone detectors pinpoint the zones where the reference signals are and generate the *z*ref*a* , *z*ref*b*, . . . ,and *z*ref*m* signals. The even/odd zone detectors also assess the parity of the *z*ref*y* signals, and generate the sel*y* selection signals

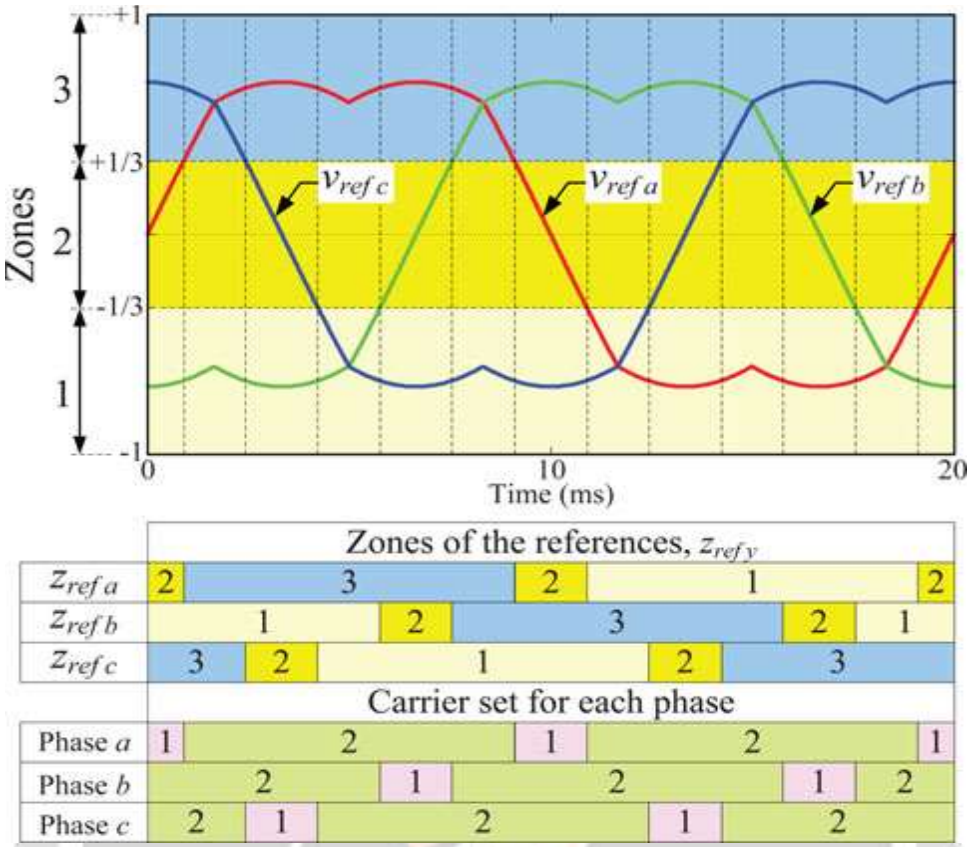

Fig. 4. Single-phase voltage reference zones and carrier set allocation for a three-phase three-paralleled-leg VSI.

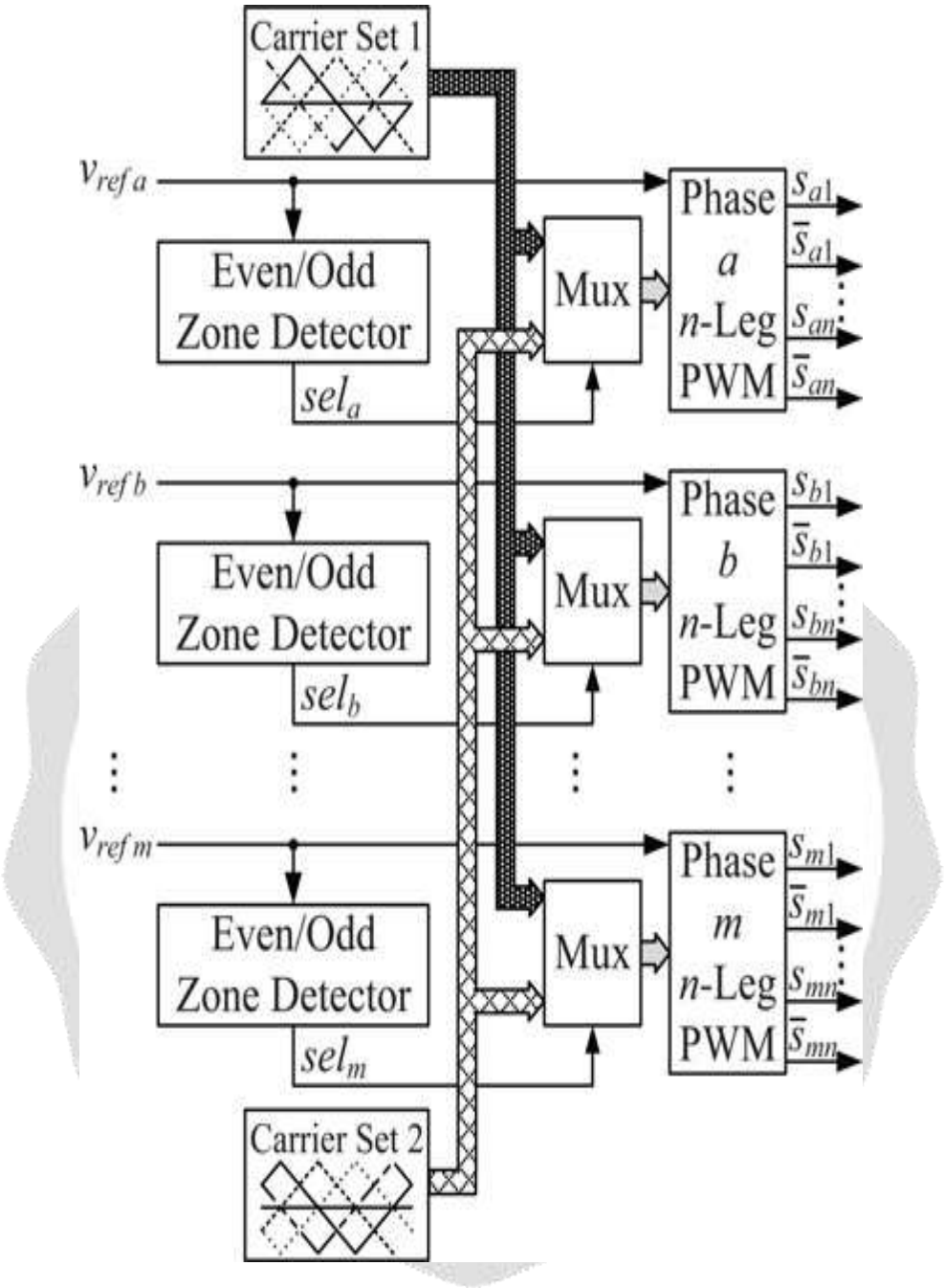

Fig. 5. Generalized *m*-phase *n*-leg modulator diagram.

according to

$$\mathrm{sel_y} = \mathrm{mod}\left[\mathrm{z_{ref\,y}}, 2\right], \quad \text{for} \quad \mathrm{y} = \{\mathrm{a}, \mathrm{b}, \ldots \ldots \mathrm{m}\} \tag{4}$$

Depending whether a phase reference signal lies within an even or an odd zone, its modulation is carried out by means of one or another set of carriers, respectively. In the example shown in Fig. 4, Set 1 is assigned to even zones and Set 2 to odd zones.Those sel*y* signals control the multiplexers that route one or another set of carriers to the PWM blocks that, ultimately, set the ON–OFF state of the VSI switches.

IV. SIMULATION RESULTS

The proposed structure of the any number of phases and any number legs connected in parallel. In this method used for a line-to-line output voltages is improved, to decrease the THD values and reduce current in the ripple. at the amplitude and frequency modulation indices using MATLAB/Simulink.The circuit parameters are

Dc bus voltage=48, carrier frequency fc =2 kHz, inductors L = 6 mH, and Wye-connected load resistors R = 10Ω.

The simulation of three phase with two legs connected in parallel is shown in Fig 6.Transient from conventional PS-PWM to proposed PS-PWM with modulation index $m_a = 0.8$ is shown in Fig 7and the THD versus modulation index is shown Fig 8.

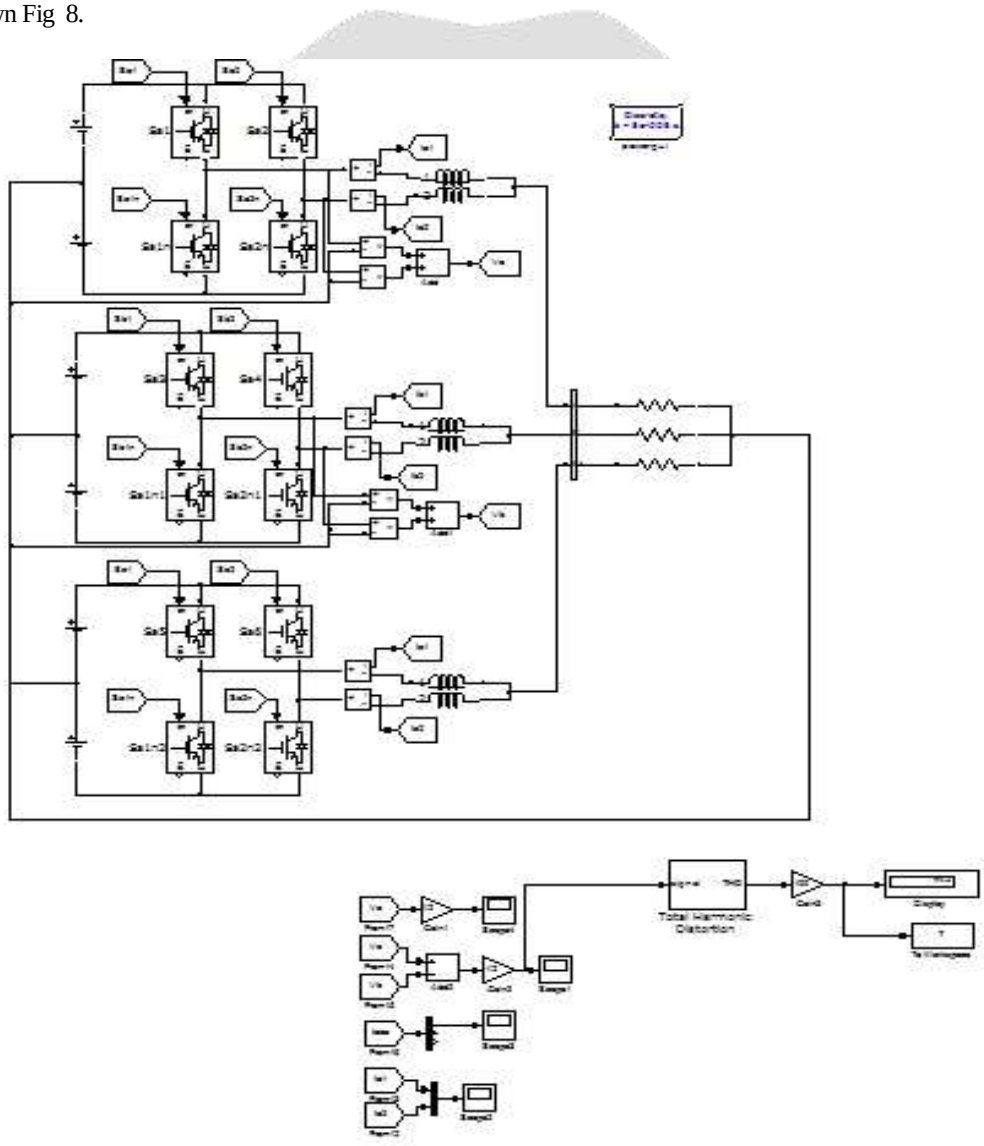

Fig 6: Simulation of three phase with two legs connected in parallel.

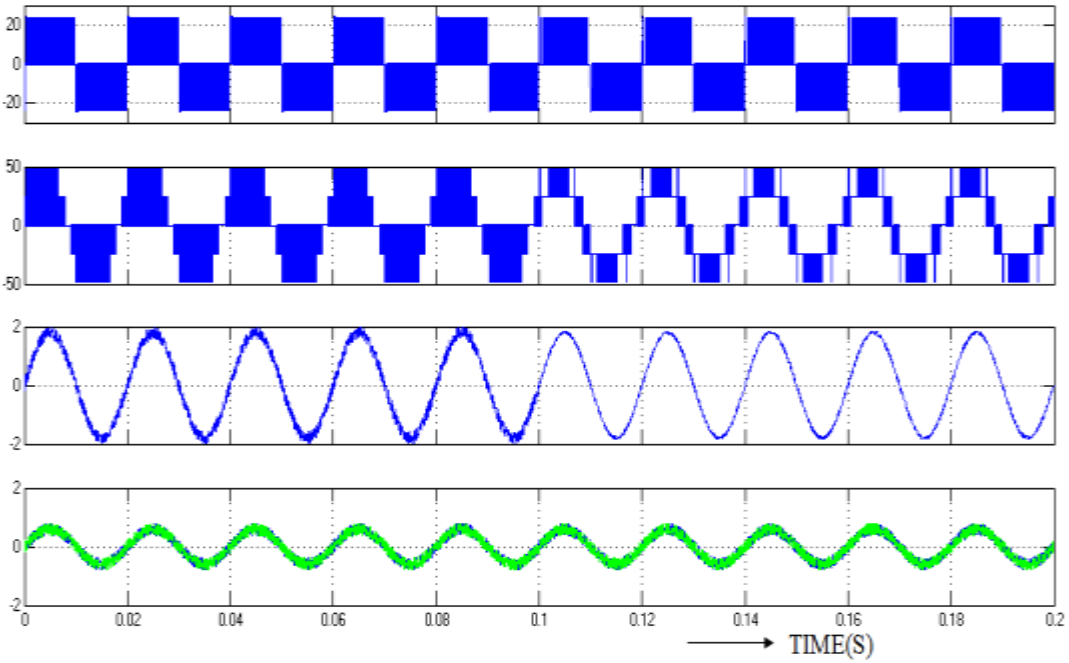

Fig7: Transient from conventional PS-PWM to proposed PS-PWM with modulation index $m_a = 0.8$ From top to bottom :phase voltage, line-to-line voltage, phase current, and phase-a leg currents.

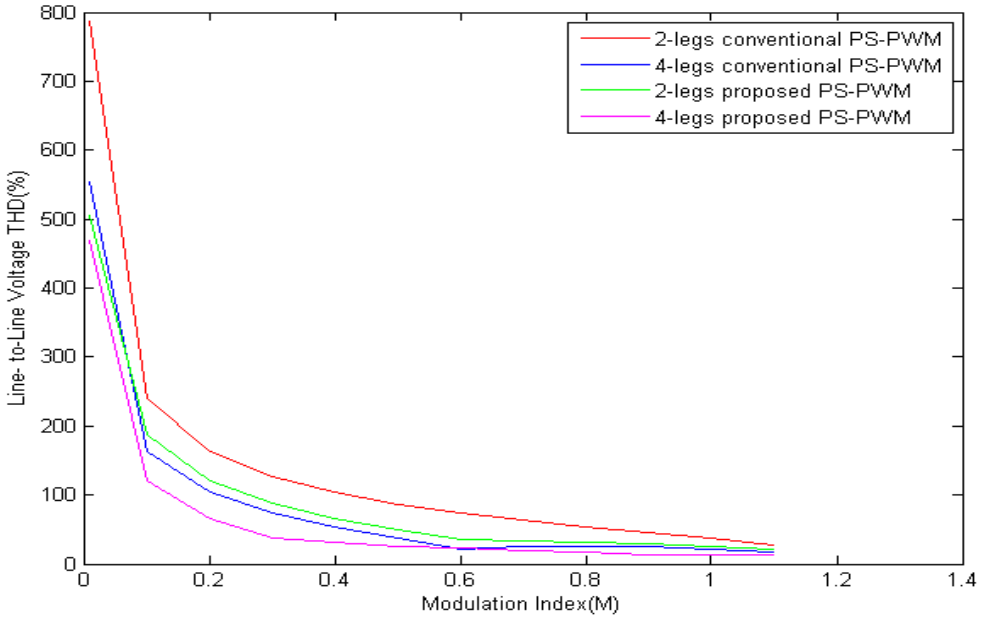

Fig8: Line-to-line voltage THD versus modulation index for two and four legs in parallel.

The simulation of three phase with three legs connected in parallel is shown in Fig 9.Transient from conventional PS-PWM to proposed PS-PWM with modulation index $m_a = 1$ is shown in Fig 10and the THD versus modulation index is shown Fig 11.

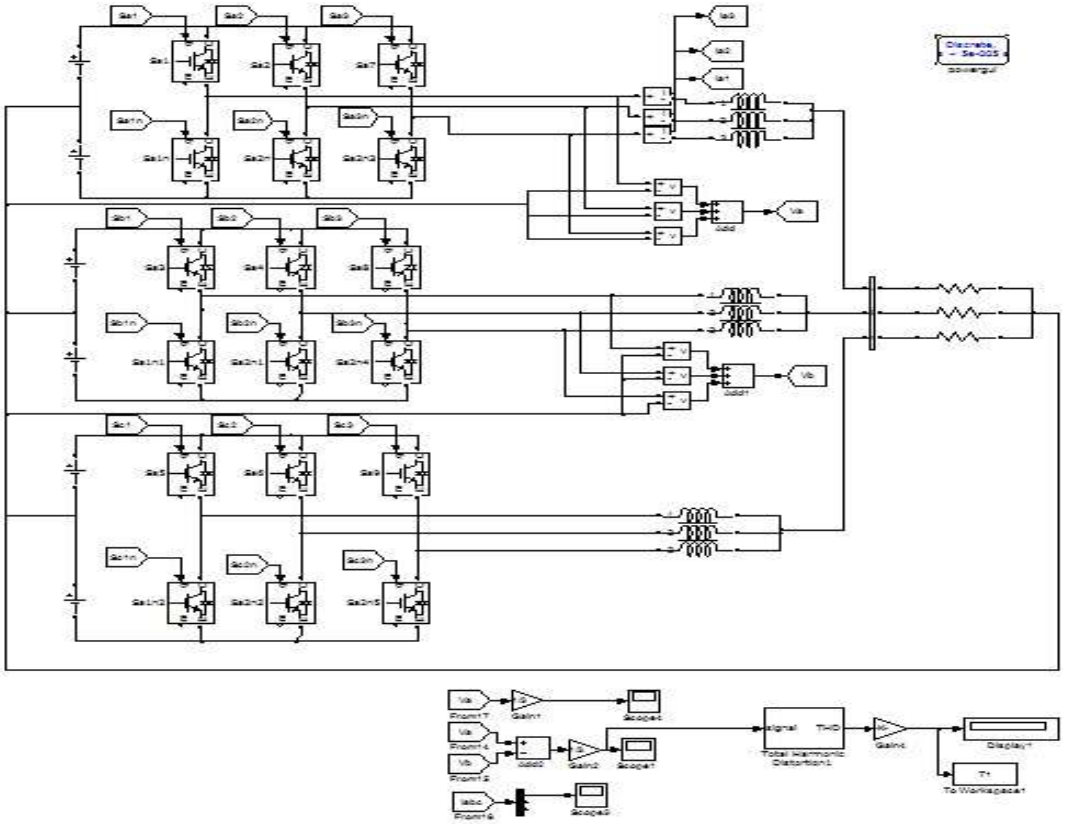

Fig 9: Simulation of three phase with three legs connected in parallel.

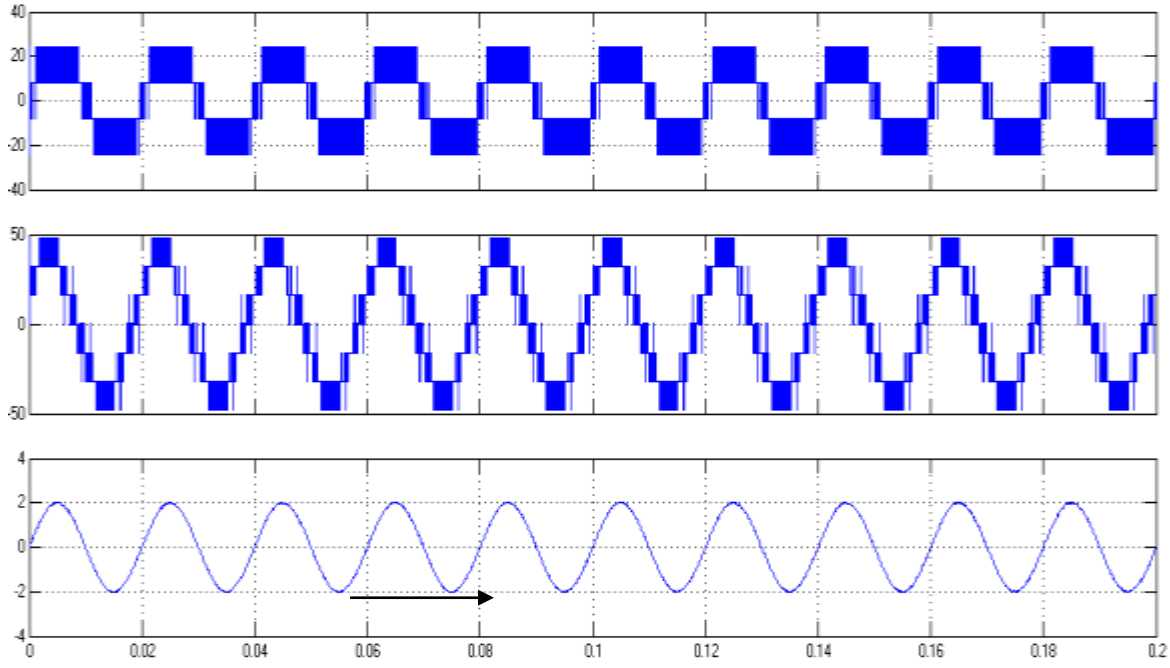

Fig10:Three phase three legs connected in parallel. Transient from conventional PS-PWM to proposed PS-PWM with modulation index $m_a = 1$ From top to bottom :phase voltage, line-to-line voltage, phase current to phase current.

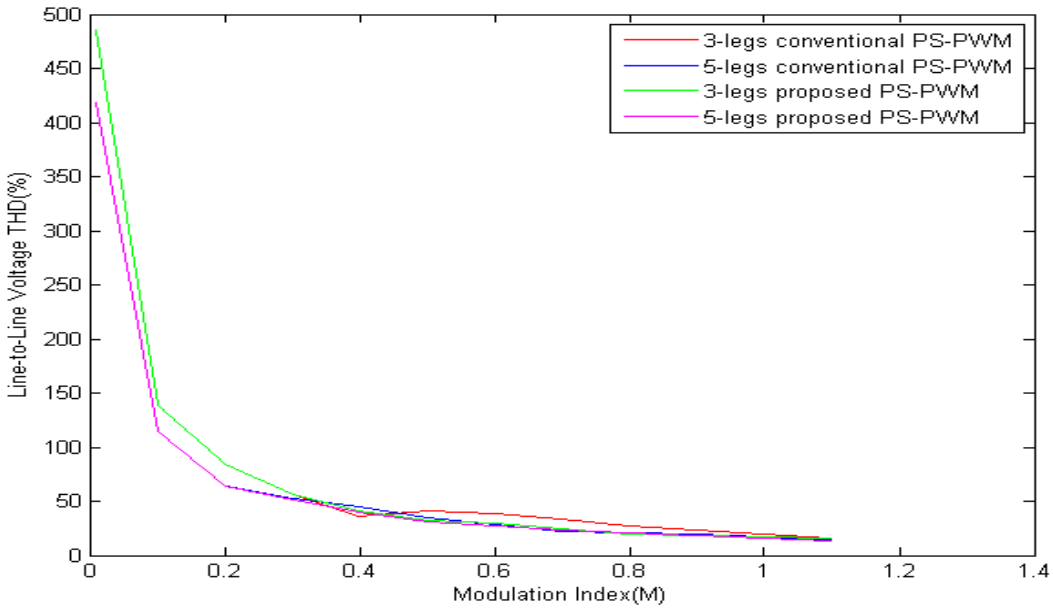

Fig11: Line-to-line voltage THD versus modulation index for three and five legs in parallel.

The simulation of three phase with three legs connected in parallel is showing a step in the modulation index m_a from 0.3 to 0.6.The reference signal includes random noise to represent a control action. The Phase-a reference voltage, reference zone is showing fig12.the phase voltage, line-to-line voltage, and phase -to-phase current are as showing Fig13

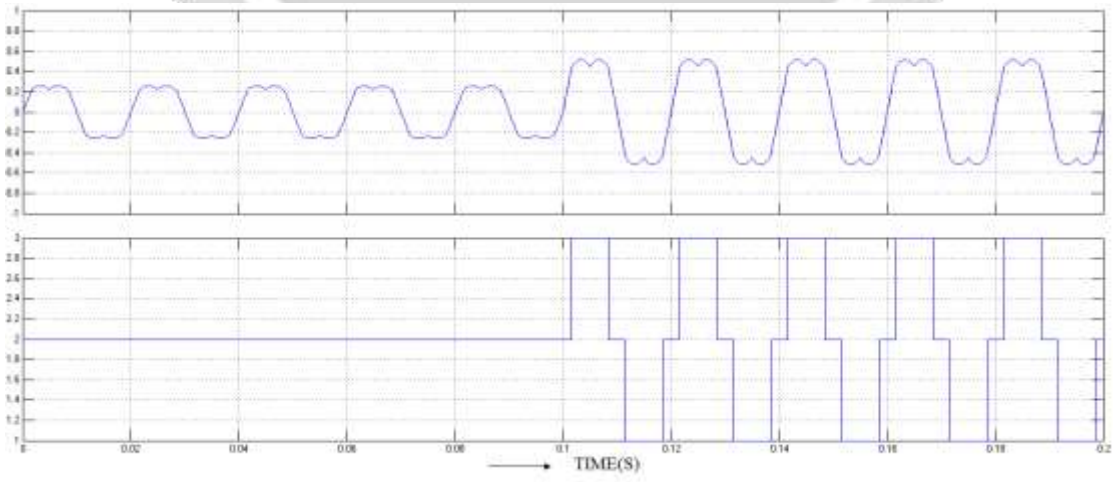

Fig12: From top to bottom: Phase-*a* reference voltage, reference zone.

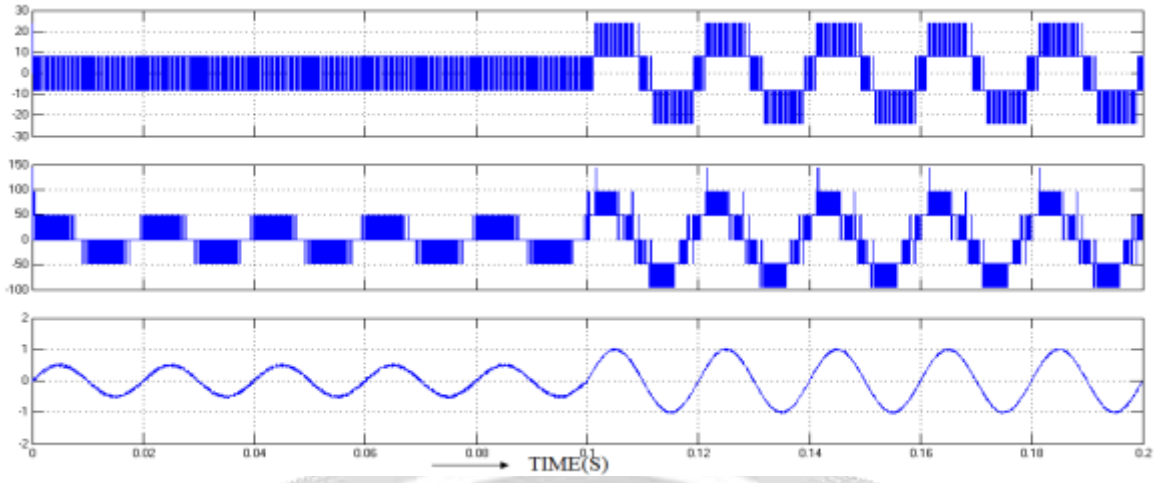

Fig13*:* From top to bottom: phase voltage, line-to-line voltage, and phase to-phase current.

V. CONCLUSION

The new inter leaved PWM implementation for VSIs with legs connected in parallel. the quality of the line-to-line output voltages is improved owing to the fact that switching occurs exclusively between adjacent levels. The modulator makes use of two sets of *n* evenly phase-shifted carriers that are dynamically allocated. The implementation is presented in a general way so that it can be applied to multiphase converters with any number of phases and any number of legs in parallel per phase. It is, therefore, appropriate for modular parallel converters. Because of the improvement in terms of line-to-line voltages, better THD values are achieved, which can lead to a reduction in the output filtering requirements.

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