SIMULATION OF THREE PHASE MULTI-LEVEL INVERTER WITH LESS NUMBER OF POWER SWITCHES USING PWM METHODS

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ABSTRACT

The cascade H-bridge multilevel inverter has lesser harmonics as well as switching stress compared with diode clamped and flying capacitor multilevel inverter, But cascaded H-bridge multilevel inverter has more number of power switches required for multilevels. Hence more number of power switches leads greater heat losses, large in size, higher in cost and huge gate circuitry. The proposed structure contains less number of power switches and less harmonics in the output voltage than compared to cascaded H-bridge multilevel inverter. In order to get lesser hormonics and quality in the output waveform by the different PWM startegies. The different PWM strategies are, In-Phase Disposition Level-shift PWM(IPDLS-PWM), Anti-Phase Disposition Level-shift PWM(APDLS-PWM), Carrier Overlap Level-shift PWM (COLS-PWM) and Variable Frequency Level-shift PWM(VFLS-PWM) has been done. The results are verified through simulation study in MATLAB/Simulink in order to select the best PWM startegy, which provides less ripple(THD) in the output wave. An LC filter has been designed to eliminate the ripples and improve the harmonic profile.

Keywords : *Multilevel inverter, PWM strategies, Total Harmonic Distortion, LC filter*.

I. INTRODUCTION

Now a days, renewable energy sources are widely used in electrical industry such as photovoltaic, wind etc., in that, photovoltaic (solar energy) most research on solar energy most research on photo voltaic(solar energy) because solar energy availability is huge in universe and free of cost. To extract the energy from solar is DC, with the help of photo voltaic cell. The conversion of dc to ac with the help of inverter(single phase or three phase inverter).The basic two level inverter gets Vdc and '0'.The generated output has high ripples. Therefore, to improve the quality of the output wave form and minimize ripples in the wave using high switching frequency and different PWM strategies. In high power applications the two level inverter has some disadvantages i.e., switching losses is more and constraints of the device ratings. Therefore the multi level inverter is overcome above disadvantages.

Multi level inverters are three different structures they are diode clamped, flying capacitor and cascaded multi level inverter. The cascaded H-bridge configuration has lesser number of components as compared to the diode clamped, flying capacitor inverter. This paper provides new three phase configuration to produce the 15 level output with less total harmonic distortion in its output voltage.

The diode clamped multilevel inverter has 28 switches, 182 diodes and 14 main DC bus capacitors per phase to produce an 15 level stair case as the output voltage .The capacitor clamped multilevel inverter uses 28 switches, 91 clamped capacitors and 14 main DC bus capacitors per phase and the cascaded H-bridge

inverter uses 32 switches per phase .This paper describes a single phase inverter configuration with 10 switches and 4 DC sources. The all single phase inverters are interconnected and get three phase inverter. The three phase inverter is connected to a star connected pure resistive load with a common earth point. Therefore the circuit offers lesser gate control circuitry, lesser cost, lesser rating, more ease of installation and lesser electromagnetic interference .The performance of multi level inverter using IPD, APD, CO and VF PWM methods the purpose of the output LC filter is attenuating voltage ripples in the output.

II. PROPOSED TOPOLOGY AND OPERATION

In proposed topology have simple concept i.e. added the voltages in series in circuit, get multilevel as output. In this proposed topology Vdc, 2Vdc, 2Vdc and 2Vdc are added up for 15 level output i.e. +7 Vdc levels for upper half cycle and -7Vdc levels for lower half cycle of the generated voltage waveform. And this paper mainly focus on minimize the power switches in the circuit for getting multilevel. The proposed inverter structure has ten power switches with four DC sources per phase as shown in Fig 1.

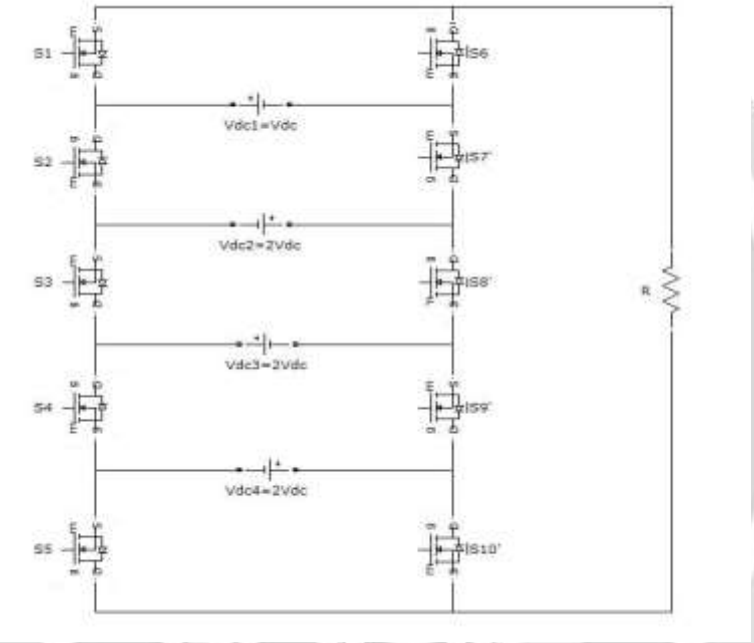

Fig 1 Proposed single phase fifteen level inverter

The operation of the proposed structure is very simple. In order to get +Vdc, the power switches S1, S7, S8, S9 and S10 are conducted. For +2Vdc, the power switches S1, S2, S3, S9 and S10 are conducted. For +3Vdc, the power switches S1, S7, S3, S4 and S5 are conducted and so on. For every level of the output five switches are conducted at time per phase. The switching states of the circuit is shown in table 1.

Switches / Levels	1	2	3	4	5	6	7	8	9	10
0	1	1	1	1	1	0	0	0	0	0
1	1	0	0	0	0	0	1	1	1	1
2	1	1	1	0	0	0	0	0	1	1
3	1	0	0	0	1	0	1	1	1	0
4	1	1	1	0	1	0	0	0	1	0
5	1	0	1	0	0	0	1	0	1	0
6	0	0	1	0	1	1	1	0	1	0
7	1	0	1	0	1	0	1	0	1	0
0	0	0	0	0	0	1	1	1	1	1
-1	0	1	1	1	1	1	0	0	0	0
-2	0	0	0	1	1	1	1	1	0	0
-3	0	1	1	1	0	1	0	0	0	1
-4	0	0	0	1	0	1	1	1	0	1
-5	0	1	0	1	1	1	0	1	0	0
-6	1	1	0	1	0	0	0	1	0	1
-7	0	1	0	1	0	1	0	1	0	1

Table 1 Switching states for fifteen level inverter

III. MODULATION TECHNIQUES

For high-power applications, low-distorted sinusoidal wave forms are required. With the availability of high-speed power semiconductor devices (MOSFET, IGBT etc.,), The harmonic contents of output voltage can be minimized or reduced significantly by switching techniques. In many industrial applications, to control of the output voltage of inverters is often necessary i.e. to cope with the variations of dc input voltage, to regulate voltage of inverter and to satisfy the constant voltage and frequency control is requirement. There are various techniques to vary the inverter gain. The most efficient method of controlling the gain (and output voltage) is to incorporate PWM technique. The sinusoidal PWM (SPWM) method has been applied to the power switches. In this PMW method sinusoidal wave as a reference signal with fundamental frequency and high frequency triangular signal as a carrier signal. These two signals are compared. The generated gate pulses are applied to the power switches. Frequency or amplitude of the multiple carrier signals are varied based on the PWM technique. The modulation indices are same in all the method of comparison. Amplitude modulation index is the ratio of the amplitude of the reference signal to the amplitude of the carrier signal. Frequency modulation index is defined as the ratio of frequency of carrier signal to frequency of reference signal. Amplitude modulation index ma and frequency modulation index mf are given by (1) and (2) respectively.

$$m_a = A_r/A_c \quad (1)$$

$$m_f = f_c/f_r \quad (2)$$

Different PWM techniques discussed in this paper are In-Phase Disposition level-shift PWM, Anti-Phase Disposition level-shift PWM, Carrier overlap level-shift PWM and Variable frequency level-shift PWM. In all PWM techniques, 'N' numbers of carrier signals are used to obtain 2N+1 voltage levels.

1. In-Phase Disposition level-shift PWM

The carrier signals are in this PWM technique. They have the same amplitude of 1V and a frequency of 10 kHz. The level shifted carrier signals are compared with reference signal which is at fundamental frequency, as illustrated in Fig 2. The different levels of the output wave is detected and decoded to produce the pulses required to trigger each switch in the inverter. In order to obtain the three phases, the sine wave is shifted by 120^0.

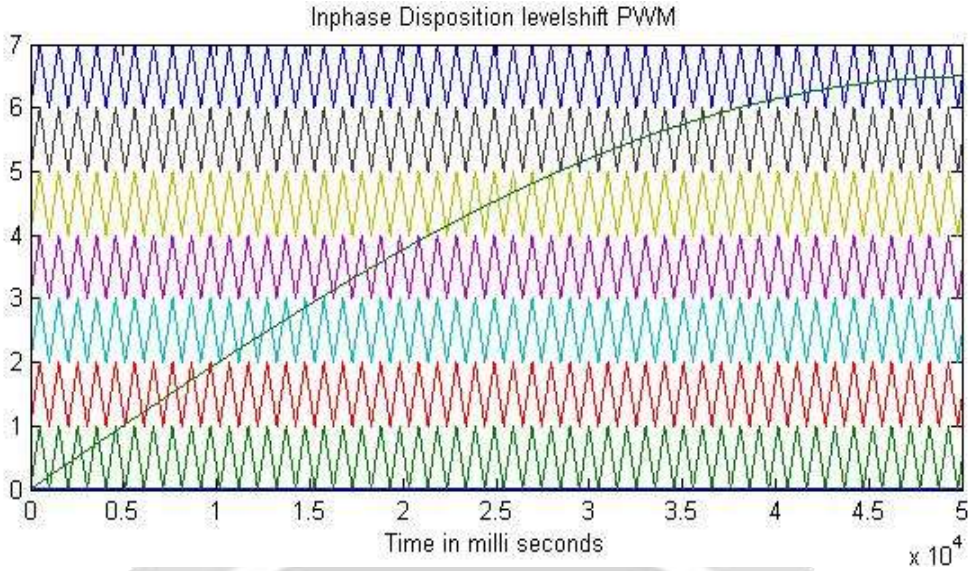

Fig 2: In-phase disposition level-shift PWM strategy

2. Anti-Phase Disposition level-shift PWM

Each carrier signal is out of phase with other carrier signal by 180^0 and has the same amplitude and frequency. The carrier signals are compared with the reference signal to produce required gate pulses as shown in Fig 3.

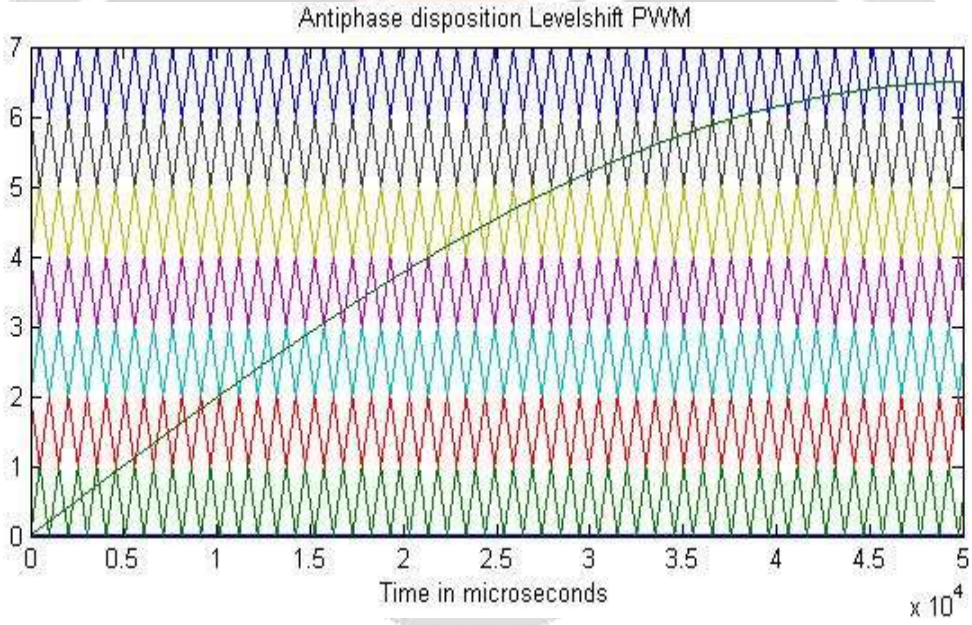

Fig 3: Anti-phase disposition level-shift PWM

3. Carrier Overlap level-shift PWM

The all level-shifted carrier signals are in phase and also overlap to each other. These are compared with the reference signal which is at fundamental frequency as shown in Fig 4. Then generated gate pulses applied to the power switches.

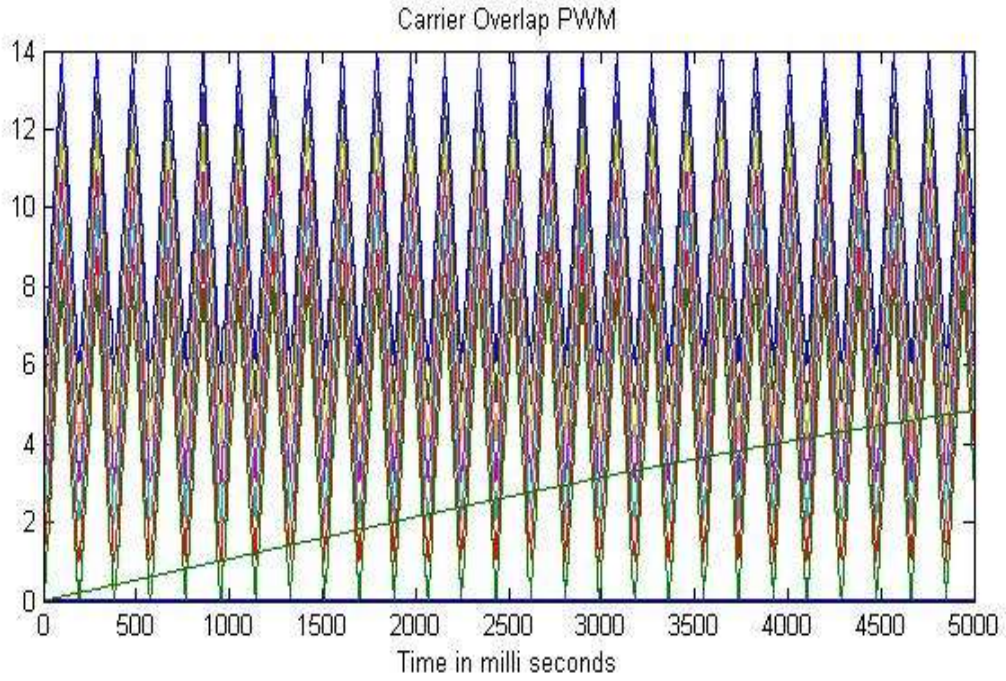

Fig 4: Carrier overlap level-shift PWM

4. Variable Frequency level-shift PWM

All level-shifted carrier signals are having different frequency. These are compared with the reference signal which is at fundamental frequency as shown in Fig 5. Then generated gate pulses are applied to the power switches.

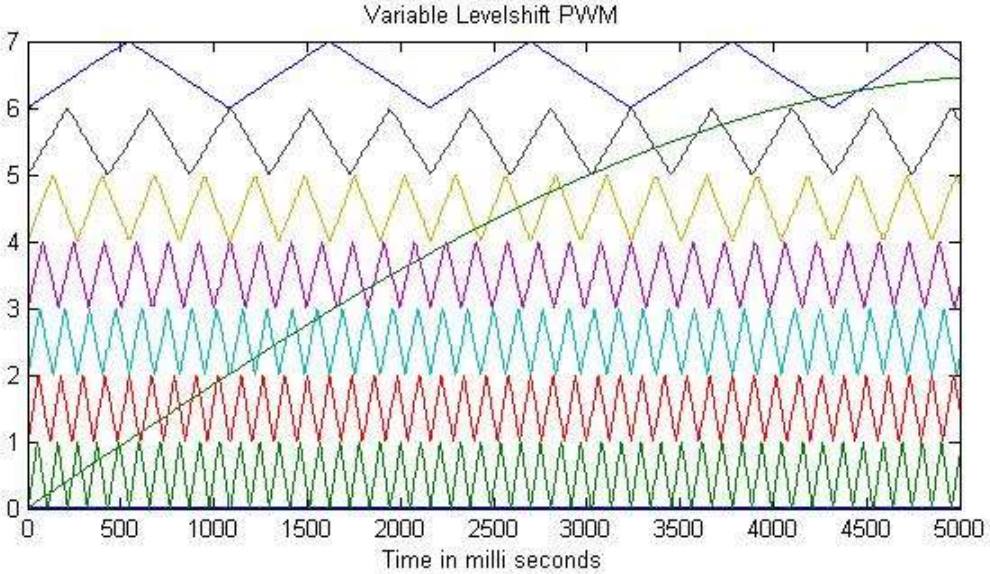

Fig 5: Variable frequency level-shift PWM

IV. SIMULATION RESULTS

Different PWM strategies are applied to the proposed structure of the three phase inverter at the same amplitude and frequency modulation indices using MATLAB/Simulink. The RMS study has been made between the RMS values of fundamental value of the output voltage and total harmonic distortion using FFT analysis tool. The circuit parameters are,

fc =10kHz, fr = 50Hz, Ar = 6.5 V, Ac = 7 V

star connected R-load, R = 50 ohms.

The simulation of three phase multilevel with less number of power switches using different PWM strategies is shown in Fig 6. The three phase output voltage waveform obtained from IPD-LSPWM strategy is shown in Fig 7.And the harmonics of the output wave is shown in Fig 8. The fundamental value of the output voltage is higher and THD is small by IPD-LSPWM. The carrier waves are in phase with each other in the IPD type, resulting in less complex circuitry.

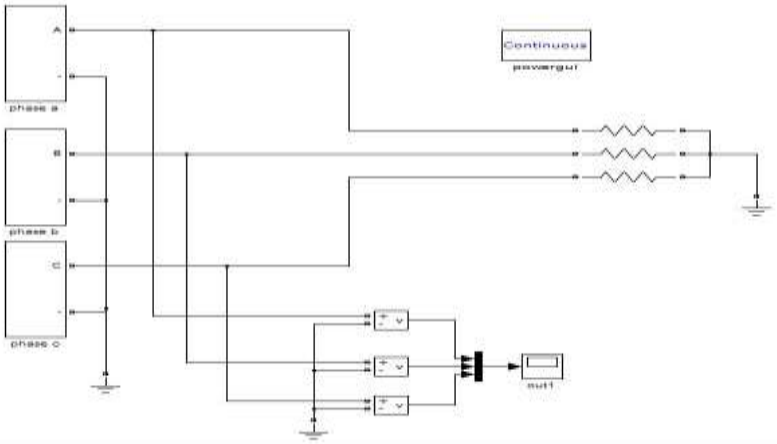

Fig 6: Simulation of three phase multilevel inverter

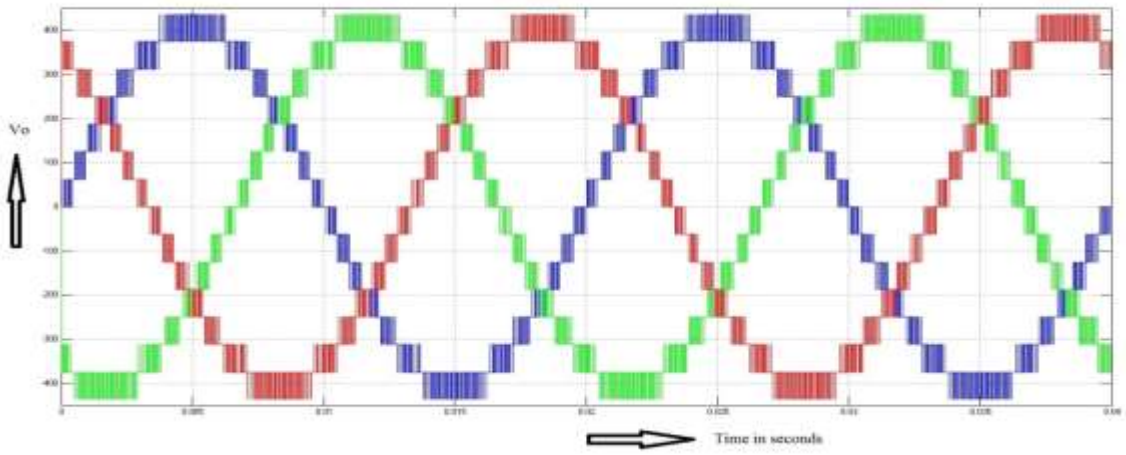

Fig 7: Three phase output voltage waveform using IPD-LSPWM strategy

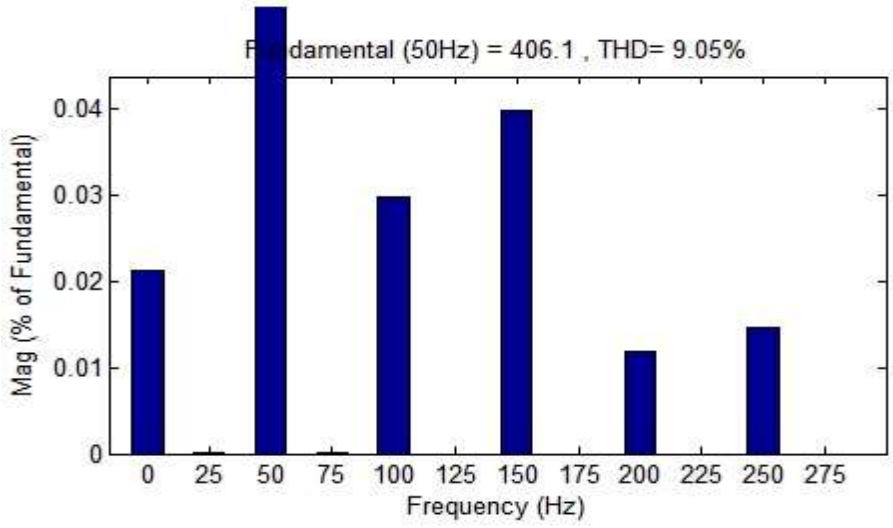

Fig 8: FFT analysis for IPD-LSPWM

The output voltages and harmonic THD using APD-LSPWM strategy are shown in figures 9 and 10. The APD-LSPWM has lesser harmonic than IPD-LSPWM strategy, because the two carrier waves are out of each other.

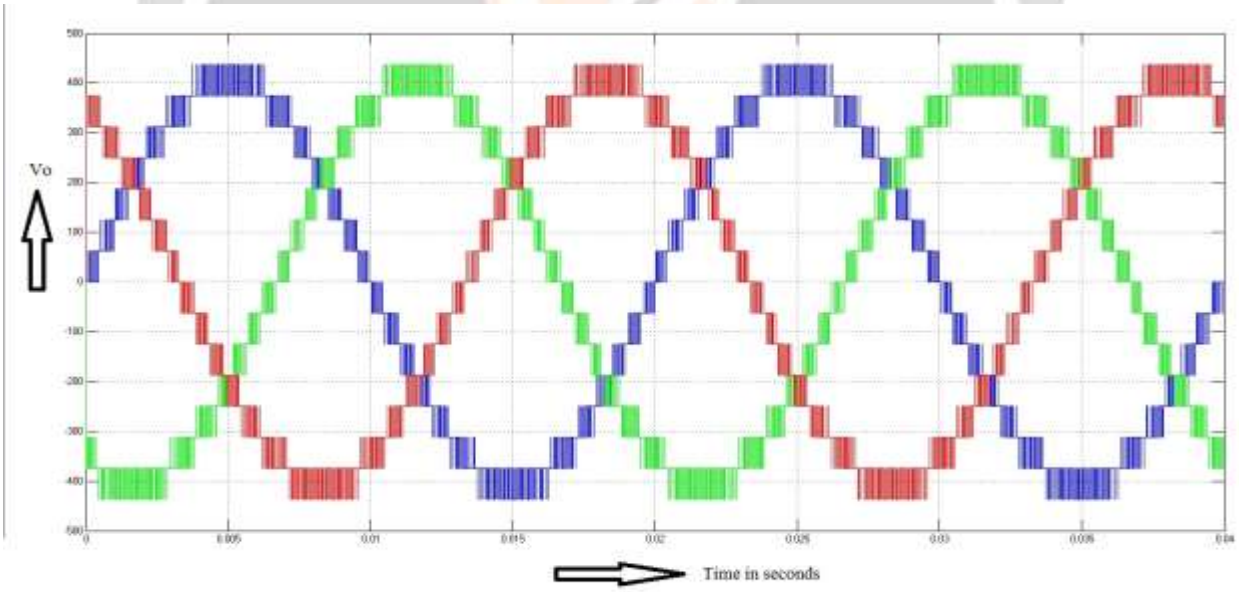

Fig 9: Three phase output voltage waveform using APD-LSPWM strategy

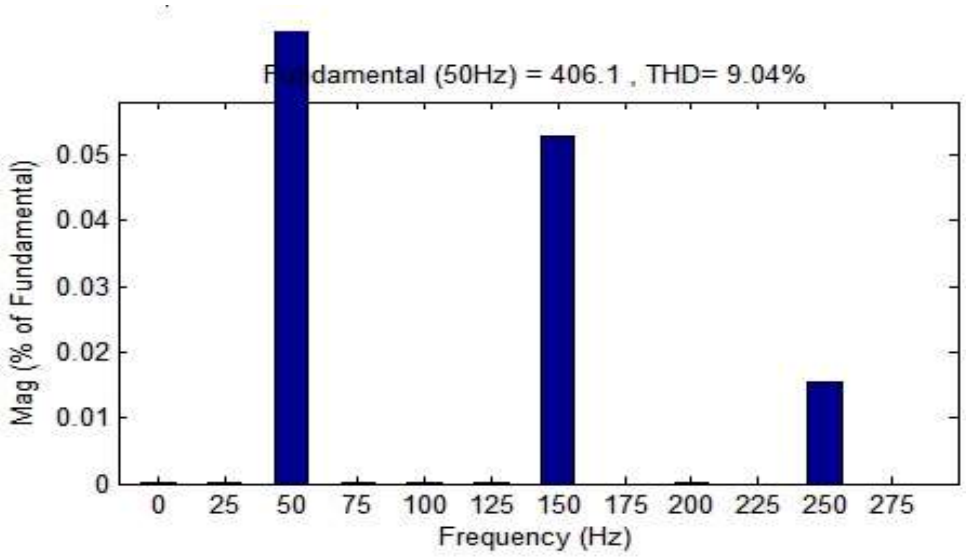

Fig 10: FFT analysis for APD-LSPWM

The three phase output waveform and total harmonic distortion using CO-PWM strategy are shown in Fig 11 and Fig 12. By the carrier overlap level shift PWM strategy has more total harmonic distortion than compared to the remain strategies, because all the carrier waves are overlapping each other. Hence generated output levels also overlaps.

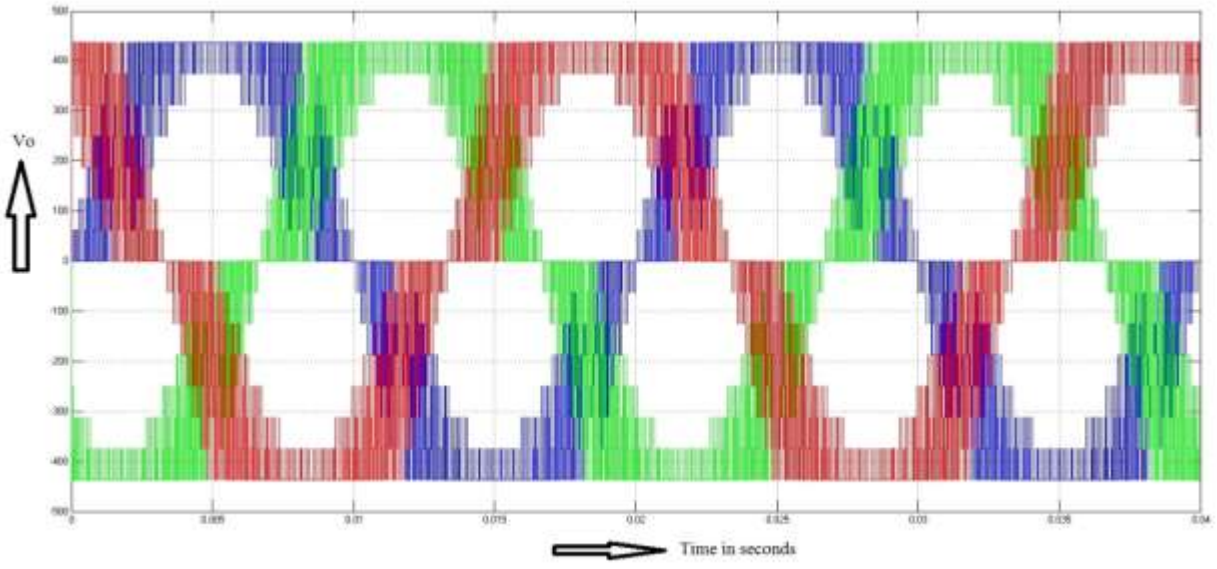

Fig 11: Three phase output voltage waveform using CO-LSPWM strategy

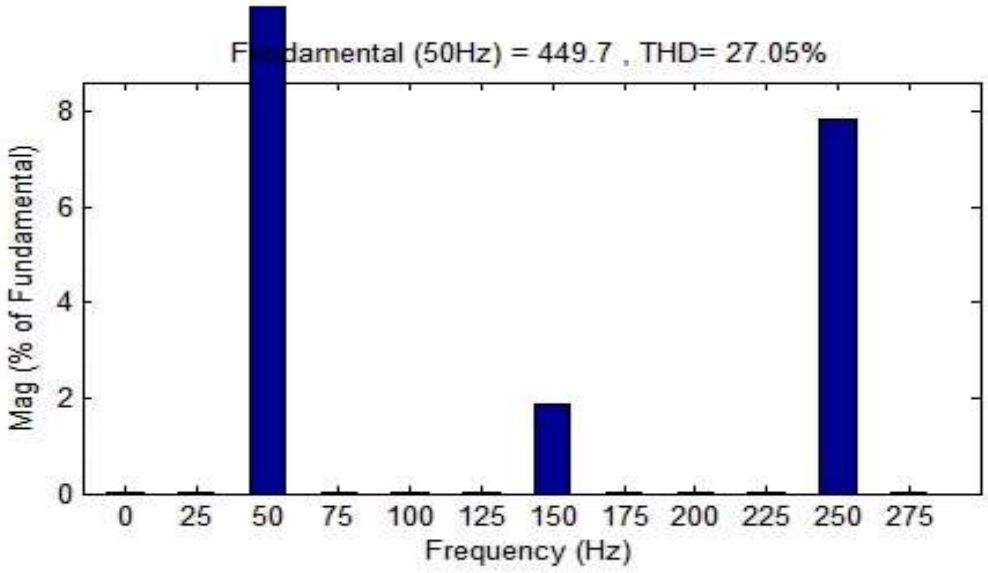

Fig 12: FFT analysis for CO-LSPWM

The output voltage waveform and total harmonic distortion using VF-PWM are shown in Fig 13 and Fig 14. The VF-PWM has less harmonic content in the presented waveform than compared to IPD-PWM, APD-PWM and CO-PWM.

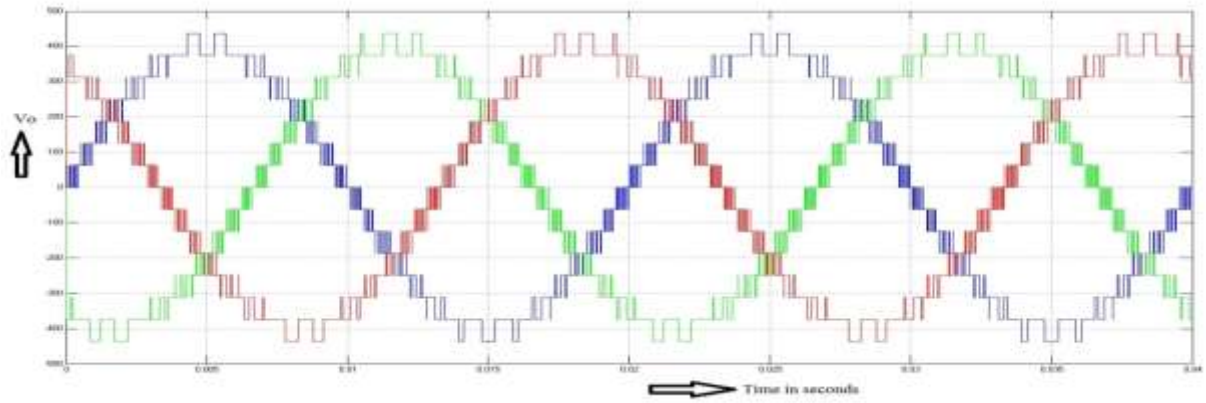

Fig 13: Three phase output voltage waveform using VF-LSPWM strategy

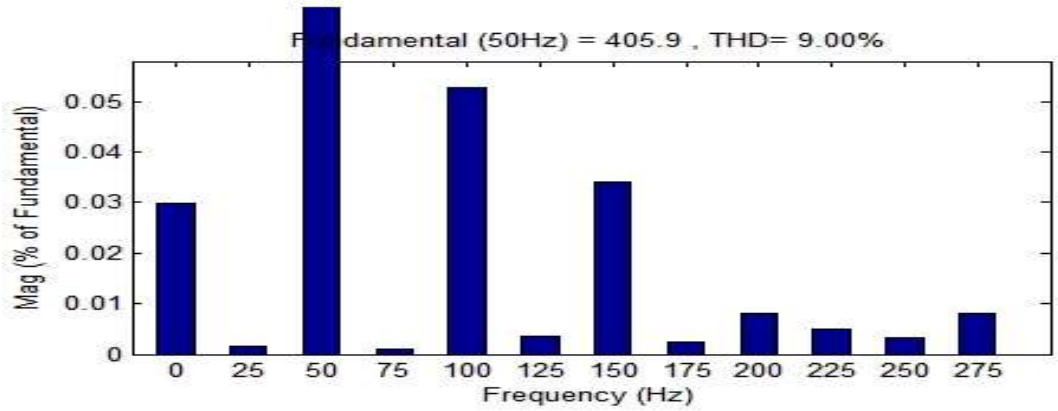

Fig 14: FFT analysis for VF-LSPWM

V. LC FILTER DESIGN

The produced the staircase fifteen level inverter has contained harmonics (i.e. higher order harmonics). The higher order harmonic is easily eliminated by LC filter. The Land C values are designed for encountering the ripples in the output waveform.

The inductance value designed,

$$L \geq \frac{R_{L-max}}{3\omega} \text{ for single phase}$$

$$L \geq \frac{2x R_{L-max}}{p(p^2-1)\omega} \text{ for poly phase}$$

(Where P= number of phases and $\omega = 2\pi f$)

The three phase inverter is connected to a star connected pure resistive load of 50 ohms. The capacitor value assumed to be 1 micro farades.

VI. CONCLUSION

The three phase fifteen level inverter structure with less number of power switches is proposed and simulated. Different PWM strategies are analyzed and compared.

From the simulation results, the variable frequency level-shift PWM strategy gives less harmonic in the wave i.e. 9.0 %. This will be best strategy compared to In-phase level-shift PWM, Anti-phase level-shift PWM, Carrier overlap PWM. The harmonic content in the wave is eliminated by LC filter.

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