Solar Photovoltaic Array Fault Diagnosis Using an IoT and Semi-Supervised Learning-Based Strategy

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Abstract

Faults inside the arrays of solar photovoltaic (SPV) systems have a major impact on their performance. The nonlinear properties of solar cells and changes in the environment make it difficult for traditional protection techniques to detect flaws. Large amounts of data and sensors are needed for learning-based fault diagnosis techniques, which makes them expensive and difficult to integrate with current SPV systems. Furthermore, current methods are unable to locate the problematic panel precisely due to the absence of panel-level monitoring. To tackle these problems, this paper suggests a methodology for fault detection, pinpointing the precise damaged panel, and precisely categorizing errors in SPV arrays. A sensor less electronic circuit with a bipolar junction transistor (BJT) and Zener diode for fault detection, an Internet of Things (IoT)-based web application for tracking individual solar panels for fault localization, and a semi-supervised learning module based on a deep auto encoder (DAE) followed by a hybrid support vector machine and logistic regression (SVM-LR) for fault classification are all part of the methodology.

Index Terms— *Solar photovoltaic (SPV) arrays, semi-supervised learning, the Internet of Things (IoT), fault categorization, fault detection, and fault localization.*

I. INTRODUCTION

For an SPV plant to operate dependably and effectively, FAULT detection is necessary. Numerous fault types, including LL, line-to-ground LG, OC, and PSCs, might affect SPV systems. These faults can be caused by poor maintenance, natural disasters, electric short circuits between ground and current-carrying conductors, accidental disconnection of two points within a string or between two adjacent strings, and accidental interconnection of two points at different potentials in an SPV array. Fire risks, decreased system efficiency, and output power loss are all possible outcomes of an undiagnosed malfunction [1]. According to estimates of energy losses from SPV array defects based on a comparison of estimated and actual data, faults may result in a sizable loss of energy [2].

Literature Review and Motivation

Numerous attempts have been made up to this point to create reliable fault diagnosis techniques. Thevenin's equivalent resistance computation using array voltage, current, temperature, and insolation measurement [7] has been used, as has statistical analysis such as comparing actual and estimated data from the SPV array [3], comparing the voltage drop in the i-v curve [4], and conducting circuit analysis based on the i-v curve and a diode-based LL and LG fault diagnosis [5], [6]. Even though these approaches accurately identify the defects, they are not cost-effective because they require a significant number of sensors. In contrast to the techniques, Hu et al. [8] improved the placement of voltage sensors for fault detection by using the i-v curve of the SPV array.

A comparable strategy made use of the threshold voltage-based method, which detects problems by means of differential voltage sensors [9]. In an SPV system, integrating the sensors with the current power units is difficult. Furthermore, PSCs and electrical problems cannot be distinguished using these methods. On the other hand, signal processing-based analysis has been widely used for SPV array fault detection using signal spread spectrum time domain reflectometry [10], autoregressive (AR) model-based time correlation of multiple signals [11], pattern recognition using a fuzzy inference system based on multi-resolution signal decomposition [12], and multi-resolution signal decomposition-based two-stage SVM [13]. However, they're computationally dependent on extra hardware. Furthermore, they can only be used for LL and LG fault detection for SPV arrays that do not have blocking diodes. Or, a machine. Examples include the following: fuzzy C-mean clustering based on feature extraction using output i-v characteristics measurement [17], graph-based semi-supervised learning [14], [15], convolutional neural network-based approach [16], artificial neural network-based SPV bypass diode fault detection [18], data-augmented neural network (DANN) approach [19], and a classifier selection methodology that uses hierarchical classification and machine learning to classify LL and LG faults [20]. However, the majority of these methods do not make use of bypass and blocking diodes. Moreover, these algorithms in a real-time system require a large amount of labeled data and training, which is costly and time-consuming. Recently, sensor less techniques [21], [22], [23], and [24] have focused on identifying SPV array failures in order to lessen the massive data demand. The limits of these methods are the precise localization of the defective panel and the classification of PSCs and OC faults, despite the fact that they identify the problem accurately. Murtaza et al. [25] proposed a sensor less circuit-based reconfiguration method for panels that are bypassed during PSCs .It does not, however, take into account every kind of fault event. Additionally, these techniques are evaluated without bypass diodes or blocking. Despite the abundance of research in this area, there are still a number of unresolved issues that make it difficult to pinpoint the exact location of defective panels and categorize all fault kinds, including PSCs. The National Electricity Code (NEC) of the United States, for example, mandates that OCPD be connected in series with every SPV string. However, with smaller mismatch level faults, it could not be enough to stop the low magnitude back-feeding current [22]. Additionally, the SPV array's current is significantly decreased due to MPPT operation in order to preserve the inverter's working voltage in the event of a malfunction [26]. The minimum operational current needed by ground fault prevention devices (GFPDs) might not be achievable in dimly lit environments. It is difficult to distinguish between fault and PSC when blocking and bypass diodes.

Describe the strategies used by the suggested plan to get around these restrictions

This article suggests an Internet of Things (IoT)-based sensor less electronic circuit to identify and pinpoint the issues in order to get around these difficulties. The majority of the techniques used in the literature to categorize the errors are supervised learning based and mostly rely on labeled data, which is costly to acquire. In order to solve this problem, a hybrid support vector machine and logistic regression (SVM-LR) model is created to categorize the fault occurrences after a semi-supervised deep learning technique based on LSTM and DAE. In light of this, none of the current approaches suggests a sensor-less, learning-aided technique.

A. *Significance and Contributions:*

The following is a list of this article's main contributions.

1) A sensor-less FDEC that is inexpensive and simple to install is created.

2) To locate malfunctioning or circumvented SPV panels, an Internet of Things-based FMDS was created.

3) A data-on-demand strategy is suggested, whereby panel data is only provided to the deep learning model when an abnormality is found. Consequently, the amount of data is decreased, and the processing load is reduced.

4) To classify the defects, a hybrid SVM-LR model is created using a customized deep auto encoder-based semi-supervised deep learning technique. Training duration was significantly reduced by 97% and classification labels were reduced by 88% using this strategy. To the best of the author's knowledge, SPV fault classification is the first application of the created algorithm.

In order to diagnose faults in an SPV system, this article aims to lessen the need for expensive sensors and a significant amount of data. In a grid-connected SPV hardware arrangement operating under MPPT with bypass and blocking diodes under various electrical and climatic circumstances, the suggested approach is experimentally verified. The methodology is supported by the experimental findings, which total 99.67% accuracy. The performance of the suggested methodology in SPV defect detection, localization, and classification is sufficiently enhanced when compared to existing methods that are available in the literature. It is

easy to incorporate the proposed methodology into new or existing SPV installations and can be applied to SPV systems of any type.

A. Article Organization

The various sections of the article are organized as follows. Section II describes the conventional SPV array configuration and associated faults. Section III provides an explanation of the recommended detection and classification techniques. Section IV discusses the simulation results and associated experimental validation. The article is concluded in Section V.

II. Configuration of the SPV Array and Related Issues

A grid-connected SPV system with two stages is shown in Fig. 1. The dc-dc boost converter, which is further coupled to the single-phase dc-ac inverter, receives electricity from the SPV array. The boost converter is driven by the MPPT controller to maximize the SPV array's power. Every panel has a bypass diode wired across it for protection. Between each string and a common output terminal, a blocking diode is placed.. In the event of a ground fault, the array is detected and isolated using GPID.

According to Fig. 1, "F1" is the LL fault in string A with a 10% mismatch level, assuming a string contains ten panels. An LL fault with an 80% mismatch level is "F2." String B's "F3" is an OC fault, while strings B and C's "F4" is a cross-string LL fault. "F5" indicates that one panel in string C is partially shaded, and "F6" is an LG fault with a 30% mismatch level. The amount of mismatch determines how serious the error is.

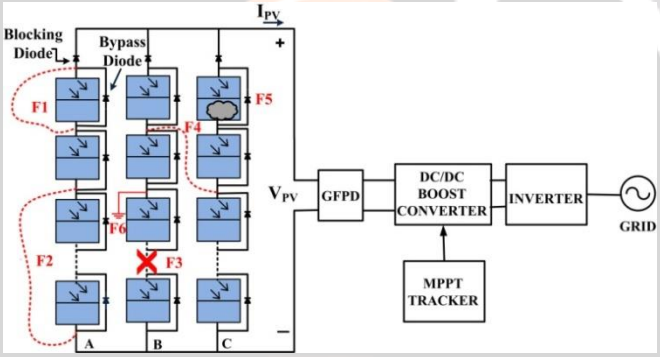


Fig. 1. Typical grid-connected SPV array configuration and differentassociated faults.

In a given string, it is defined as the number of panels impacted by the problem [20].

III. SUGGESTED TECHNIQUE

The proposed methodology's overall schematic is shown in Fig. 2. It includes three steps:
1) Utilizing a sensorless FDEC to detect an event, like a fault or PSC; 2) using an IoT-based FMDAS to locate faults; and 3) classifying the fault events using a semi-supervised deep learning algorithm. In Sections III-A through III-D, the specific process is described.

A. Measurement and Acquiring of Data

The tools and equipment utilized for data measurement are presented in Table II. The FDEC, a measuring circuit for fault detection, is developed using a BJT and a Zener diode. Through analog to digital conversion (ADC), the collector voltage, VC, from the FDEC is measured by an 18-channel 12-bit ADC ESP32 microcontroller. Additionally, VC is a binary measurement with two possible values: HIGH and LOW. FDEC is transformed into an Internet of Things device using an ESP32 microcontroller. For fault localization, it sends measured VC to the server using PHP and MySQL [30]. Using a 1 kHz sample rate, the TI F28379D microcontroller measures ipv and vpv. The

instruments used for measurement have several important benefits, including low cost and low power needs.

B. Identification of Faults:

A sensorless electrical circuit for identifying malfunctioning panels is shown in this article. [25] is the driving force behind the suggested redesigned circuit. The circuit's use is not restricted to identifying the bypassed panel during PSC; it may also be applied to various defective events. It is then expanded to include fault categorization.

1) *Electronic Circuit Design:*

To identify malfunctioning or circumvented SPV panels, a sensor less electronic circuit based on BJT and Zener diodes is created. In the breakdown zone, a reverse-biased zener diode is utilized to keep the voltage across it constant. It also functions as a shielding device, preventing abrupt voltage spikes and huge reverse currents during unexpected malfunctions. An n-p-n-BJT is used in the saturation and cut-off regions of the suggested detection circuit. BJT functions as a constant current regulator when combined with a Zener diode.

2) *Design parameters and circuit interface with SPV panels:* Fig. 3 illustrates how the fault detection circuit is integrated with SPV panels. The Zener diode connects the BJT's input (base terminal) to the SPV panel's bypass diode. The transistor's output is coupled to the 5 V biasing supply via collector resistance R3, together with two resistors R1 and R2. A voltage divider circuit with R1 and R2 positioned in its middle serves as the fault detection output. R2 is chosen to restrict the amount of current that passes through the Zener diode. With a voltage (VZ) rating of 5.1 V and a power (PZ) rating of 1 W, the maximum Zener current can be computed as

$$I_Z = \frac{P_Z}{V_Z}$$

An excessive diode current caused by a tiny value of R2 raises the FDEC's power consumption. A value of 39 kΩ is selected as the R2 value based on multiple experimental iterations. Deducing the diode current by setting the diode forward voltage (VF) at 1.2 V and the Vpv, min at 5 V,

Under MPPT conditions, Vpv, min is the minimum panel voltage, and it is taken to be 5 V. To improve the regulation of Zener voltage, R1 is set at 1.5 kΩ. This is the BJT's collector current:

$$I_C = \beta \times I_B$$

where I_B represents the base current and β represents the BJT's current gain. A value of 100 μA is determined for Id, which is sufficiently minimal to prevent any loading effect on the sensing circuit. The β is expected to be 0.1 for a given value of Id. By taking 0.3 V as the saturation voltage between the collector and emitter ($V_{C\,E,sat}$) and 5 V as V_{bias}, the collector resistance R3 may be computed as

Please take note that the type of Zener diode and BJT will determine the resistance and diode current. Additionally, these values can be empirically determined to maintain low power consumption of the sensing circuit, as long as the BJT and Zener diode's minimum operating conditions are not broken [27], [28].

3) Interfaced Circuit Operation: Figure 3 shows that the related SPV panel's bypass diode is reverse biased and that string current IS flows through it under normal conditions (NF). Under these circumstances, collector voltage VC stays "LOW" and BJT functions in saturation mode. The bypass diode gets forward biased during any defective event (LL, LG, OC, or PSC), causing the string current IS to flow through it. This results in zero forward current Id through the resistor R2, which forces the BJT to operate within the cut-off area. As a result, the collector voltage VC settles to the biasing voltage and becomes "HIGH," while the collector current IC drops to zero.

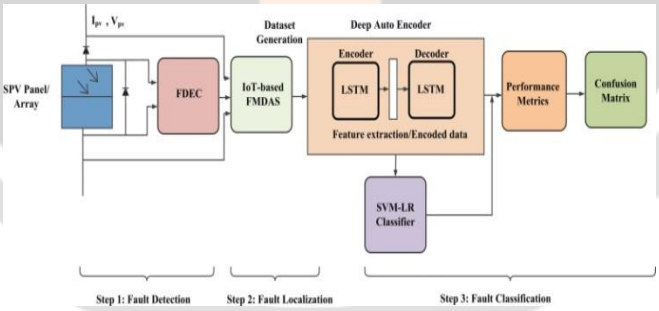


Fig. 2. Schematic of the proposed SPV array fault detection, localization, and classification methodology.

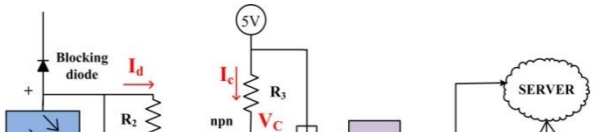


Fig. 3. Proposed FDEC and IoT-based monitoring system.

4) Benefits of the Fault Detection Approach: The following is a summary of the benefits of the suggested fault detection technique.
1) The FDEC costs as little as INR 10 ($0.15) for all of its parts. A small amount of room is needed to interface the proposed circuit with the SPV panel close to the junction box because of its compact design.
2) Just 0.01% of the panel's rated power is used by the suggested FDEC. According to what the experiments showed,
When connected to a Vmpp 18.1 V and Impp 2.2 A SPV panel, it uses 0.221 mA.
3) The Zener diode isolates the sensor circuit by acting as a shielding device that can tolerate large reverse current and prevent voltage spikes.
4) It is noteworthy that the suggested FDEC functions best at temperatures between -55 °C and +175 °C [27], [28]. Section IV talks about the experimental validation.

C. *Fault Localization System Based on IoT*
A web application based on the Internet of Things is created to pinpoint the precise location of malfunctioning panels. The ESP32 [29], a low-cost microcontroller with built-in WiFi, is used for this. The whole fault monitoring system is seen in Fig. 3. A multiplexer (MUX) receives the collector voltage (VC) from each SPV panel, and the ESP32 receives the MUX's analog output. The ESP32 handles the ADC, and the SPV panel's condition is determined by the collector voltage status; if the VC is "LOW," the panel is "NOR-MAL." In the event that VC is "HIGH," the panel is deemed "FAULTY." As illustrated in Fig. 4, data is transmitted to the server using MySQL and PHP [30].
To prevent inaccurate information about the SPV panels, the server is turned on or off based on the time stamp. Following data collection, the web server receives the SPV panel's status and uses it to pinpoint the problematic panel. The process is described in Algorithm 1, and a real-time visualization of a purposeful cross-string failure between SPV panels 2 and 5 in a 3 3 SPV array is displayed in Fig. 5. As a result, 100% accuracy of localization (AOL) is deduced.

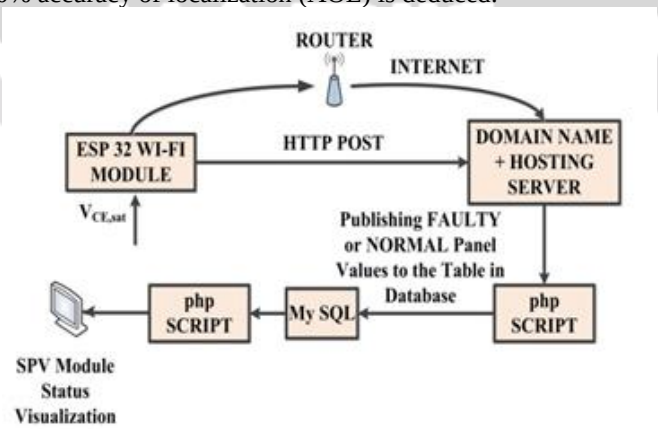


Fig:4 MySQL and php flowchart

D. Categorization of faults
The methodology for classifying SPV array faults is explained in Figure 6. The benefits of LSTM and DAE are combined in the suggested semi-supervised learning method for autonomous feature extraction. The extended input characteristics include i_{pv} and v_{pv} at maximum power point (MPP) at various degrees of solar insolation (G) and temperature (T). The data samples are next

preprocessed and normalized to eliminate any outliers as specified in (5) in order to have common generalization among the obtained samples. The input data is normalized in this case, and the variables max and min stand for maximum and minimum values, respectively.

1) LSTM-DAE-Based Feature Extraction: In many domains, deep learning is a crucial instrument for defect diagnosis and classification. In this article, temporal features were extracted using LSTM, semi-supervised learning was done using DAE, and the hybrid SVM-LR classifier was utilized after that.

By removing the gradient issue in back-propagation for time series modeling, LSTM networks are utilized in favor of recurrent neural networks. Three gates make up a basic LSTM network: input, forget, and output gates. Each memory cell's ability to store incoming data is determined by the input gate. The forget gate enables memory to remove unnecessary information, while the output gate prevents disruptions from extraneous data. The following equations provide the general mathematical formulation for LSTM:

$$f_t = \rho(W_f[h_{t-1}, x_t] + v_f) \quad (6)$$

$$i_t = \rho(W_i[h_{t-1}, x_t] + v_i) \quad (7)$$

$$\tilde{C}_t = \tan h(W_c[h_{t-1}, x_t] + v_c) \quad (8)$$

$$C_t = f_t C_{t-1} + i_t \tilde{C}_t \quad (9)$$

$$o_t = \rho(W_o[h_{t-1}, x_t] + v_o) \quad (10)$$

$$h_t = \tan h(C_t) \quad (11)$$

where, i_t is the input gate generated by the hidden layer h_{t-1} from the previous LSTM unit and input x_t at the current step t. W_i and v_i are the weight matrix and bias respectively. (6)

Represents the forget gate which decides the storing of the pre-vious unit state C_{t-1}. W_f and v_f are the weight matrix and bias of the forget gate. $\tilde{C}_t$ is the input information of the updated current cell. h_t is the hidden state [31]. DAE uses automatic principal feature capture to reduce the dimensions of the data. There are two stages to it: encoding and decoding. As seen in Figure 7, each step is made up of fully connected hidden layers denoted by h1, h2,... The encoder converts input Xt to a hidden feature representation yt given by using a deterministic mapping function with nonlinearity given by (12).

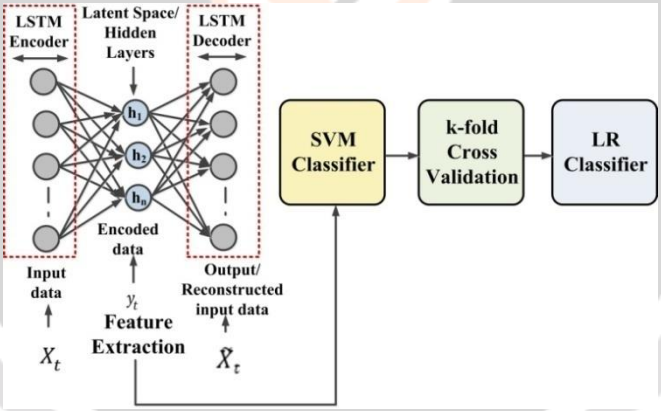


Fig.5.LSTM-DAE architecture followed by hybrid SVM-LR classifier

where y is the output, B is the bias, W is the weight matrix between the hidden layers, and ρ is an activation function. Mini-batch stochastic gradient descent (SGD) in all hidden layers during training continually updates W and B to represent Xt. Using back propagation, the DAE is trained. The output of representing input Xt is comparable to that of X_t. The mistake in reconstruction is provided in (13). The objective function in (14) can be reduced to reduce this error. In this case, X_t represents the t_{th} input sample, and X_t represents the input-corresponding reconstructed sample. In LSTM-DAE, LSTM is responsible for both encoding and decoding. When LSTM is used as a decoder, the output is the same as the length of the ipv and v_{pv} samples, but it is the same as the feature when LSTM is used as an encoder. Cutting down on the error between X_t and the precision is enhanced by X_t. Owing to DAE's dynamic behavior depending on the type of input, the hyper-parameters for the training process were empirically selected by looking at the value of E, which represents the least error [32].

2) Hybrid SVM-LR Classifier: With the use of kernels, SVM, a popular machine learning technique, has demonstrated superior performance in resolving challenging classification issues. LR's capacity to handle classification problems linearly has made it an excellent classifier. Additionally, LR responds faster and is easier to use. Managing a smaller quantity of stochastic SPV data and semi-supervised learning may result in an unbalanced training dataset that contains noise, which could reduce fault classification accuracy. In this work, a hybrid SVM-LR classifier is presented to circumvent this. In Fig. 6, the process is described. In this case, the hybrid classifier optimizes the model parameter performance and finds the particular input characteristics. The SVM classifier's structure is coupled with an equal number of LSTM-DAE output data samples. K-fold cross-validation is used to train and validate

the SVM model, after which it is combined with the LR classifier. The LR classifier is fitted with the chosen variables from SVM using the binomial approach.
A binomial target variable and several prognosticator variables are related in the binomial LR model, it employs a linear function as the input to another function.

$h_\theta(x) = g(\theta^T x)$ where, $0 \leq h_\theta \leq 1$ (15)

where g is the logistic or sigmoid function given as

$$g(z) = \frac{1}{1+e^{-z}} \quad \text{where,} \quad z = \theta^T x.$$

IV. OUTCOMES AND CONVERSATION

The suggested approach is experimentally verified using nine SPV panels coupled in a 3S3P (3 3) arrangement. The CHROMA 61830 grid simulator receives the electricity produced by the SPV array through a dc-ac inverter and dc-dc boost converter. The HIOKI PW3380 power analyzer was used to record the corresponding graphs after the TI C2000 F28379D microcontroller was used to deploy the MPPT algorithm and inverter control. A laboratory setup for real-time SPV array defect diagnosis is depicted in Fig. The specifications of the components employed are explained in Table.

SPECIFICATIONS OF HARDWARE COMPONENTS

Parameters/Circuit Elements	Values	
	DC/DC Boost Converter	DC/AC Inverter
Inductance	2 mH	-
Capacitance	2200 μF	-
Filter Inductance	-	4 mH
Filter Capacitance		10 μF
Switching Frequency	2 kHz	10 kHz
Sampling Frequency	-	100 kHz
SPV Panel		
Model Number	MS1240	
Maximum Power (P_{max})	40 Wp	
Maximum Power Voltage (V_{max})	18.1 V	
Maximum Power Current (I_{max})	2.21 A	
Open Circuit Voltage (V_{OC})	22.32 V	
Short Circuit Current (I_{SC})	2.42 A	
Tolerance at P_{max}	$\pm 5\%$	

A. *Identification of Faults*

The hardware configuration depicted in Figure 7 is utilized to confirm FDEC's functionality. A 3 3 SPV array is subjected to a variety of fault occurrences at the junction box, and PSCs are produced by purposefully hiding an SPV panel. Figure 9 displays corresponding charts of the circuit's collector voltage (Vc), grid side power (Pgrid), and SPV array power (Ppv). A problem or PSC situation is indicated by a high Vc signal.
The first string has a 33.33% mismatch level when an LL fault is introduced. Through the diode, the specific panel is avoided, resulting in "HIGH" Vc.

B. *Categorization of faults*

The two stages of fault classification are the creation of the LSTM-DAE and SVM-LR classifiers utilizing data produced in a simulated setting and the experimental validation that follows via real-time data collection from FDEC. The suggested classification approach is validated by simulating a 5 5 SPV array in grid-connected mode in PSCAD/EMTDC software to provide training and test data. A variety of fault events are purposefully produced and the associated data are documented. Python 3.64 is used to implement the method on a Windows 10 computer with an Intel i7 processor, 2.8 GHz CPU, and 32 GB of RAM.

1) *Simulation Results*: To prepare the initial data labels, LL faults are created at the 20%, 60%, and 100% mismatch levels. Additionally, cross-string LL faults between strings with every possible combination—1-2, 1-3, 1-4, 1-5, 2-3, 3-4, 2-5, etc.—are taken into account. LL fault with a 20% mismatch level is also provided in a single string at low insolation (300 W/m2). LG fault is

taken into consideration at 20%, 60%, and 100% mismatch levels at various strings. In a similar manner, PSC at one of each string's panels and OC fault with 10 potential combinations are reviewed. All LL and LG fault combinations at each mismatch level are combined under a single (master) label as LL and LG, respectively, because the number of mismatch levels is already stated in the suggested algorithm. Cross-string LL errors are included in this as well.

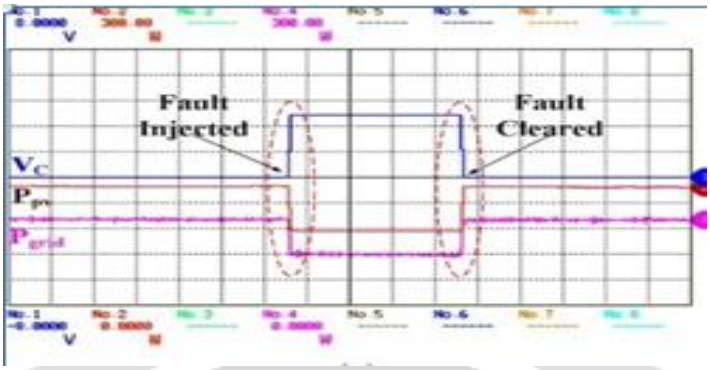
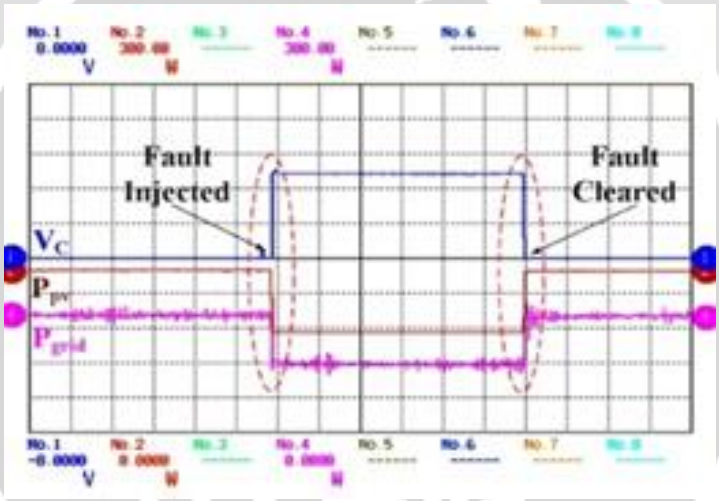
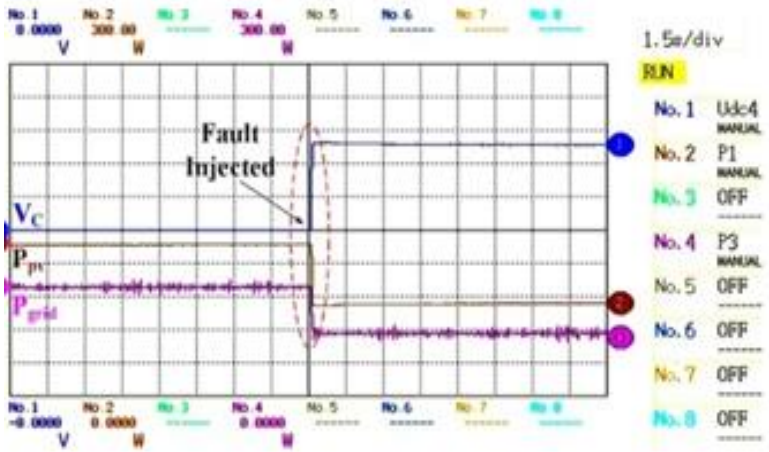


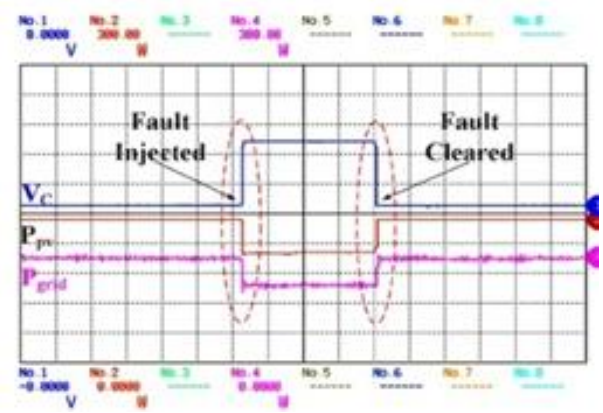
Fig 6. a) LL Faults with 33.33% mismatch



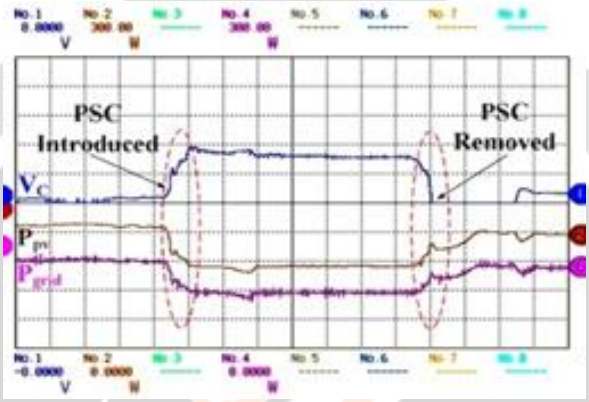
b) LG Fault with 66.67% mismatch



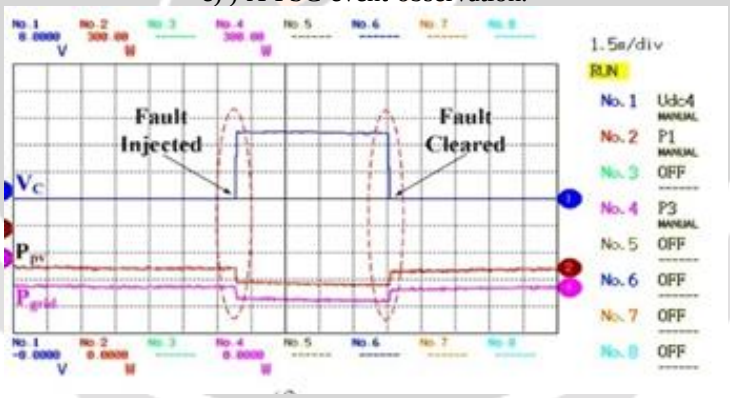
c) OC Fault at second string



d)) Cross-string LLfault between first and second string.



e)) A PSC event observation.



f) LL fault under low insolation.

V CONCLUSION

A learning-aided sensor less electronic circuit-based method for diagnosing faults in an SPV array with blocking and bypass diodes was presented in this research. First, an FDEC is created for fault event detection utilizing a BJT and Zener diode. It is determined that LL, LG, OC, and PSC faults can be detected by the suggested FDEC. Second, an IoT-based FMDAS that uses MySQL and PHP to accurately find the malfunctioning or bypassed panel was integrated with the FDEC using an ESP32 microcontroller. The FMDAS reduces redundant data overload by operating on a data-on-demand basis, sending data to the server for additional analysis only in the event of a system anomaly. Even with less labeled and more unlabeled data, a semi-supervised deep learning method based on LSTM-DAE was created using FMDAS that reliably detects errors and PSCs. The hybridization of SVM and LR classifiers improves the accuracy of complex SPV fault classification. The methodology that is being provided is very accurate in identifying and categorizing defects at all levels of mismatch and solar insolation. In addition, compared to the other approaches currently used in the literature, the suggested methodology is inexpensive, power-efficient, and maintenance-free, requires less data, and provides a fast problem detection solution. A real-time laboratory setup of a grid-connected SPV system operating under MPPT management under various electrical and climatic circumstances was

used to confirm the work's effectiveness.

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