SPEED EFFICIENT 64 BIT MAC DESIGN USING VEDIC MULTIPLIER AND REVERSIBLE LOGIC GATES

K.Aruna Sree[1], S.T.Mrudula[2],K.Geetha[3], Dr.R.Ramachandra[4]

[1]*M.Tech Scholar, Department of Electronics and communication Engineering, Intell Engineering college, Anantapur, Andrapradesh, India*

[2]*Guide & Associate Professor, Department of Electronics and communication Engineering, Intell Engineering college, Anantapur, Andrapradesh, India*

[3]*HOD & Associate Professor, Department of Electronics and communication Engineering, Intell Engineering college, Anantapur, Andrapradesh, India*

[4]*Principal & Professor, Department of Mechanical Engineering, Intell Engineering college, Anantapur, Andrapradesh, India*

ABSTRACT

A multiplying block operate may be concededin 3 totally different ways: standard addition, partial product addition (PPA) and eventually partial product Generation (PPG).The two bud vase materials that must be considered are raising the speed of MAC which is accumulator block partial and product reduction. The 64 bit MAC design which will make use of Vedic multiplier and reversible logic gate can be accomplished in two stages. Firstly, multiplier stage, where a usual multiplier is replaced by Vedic multiplier using UrdhavaTriyagbhayam sutra from Vedic Mathematics. Multiplication is the primary operation of MAC unit. Speed, area, Power dissipation, consumption and latency are the major concerns in the multiplier stage. So, to evade them, we are going to select quick multipliers innumerous applications of DSP, networking, etc.

Keywords: *PPG, PPA, MAC, DSP*

I. INTRODUCTION

In this computer era digital technology commanding the world. We can see all most every computer sharing the work another computer. The speed of a processor greatly depends on its multiplier's performance. This in turn increases the demand for high speed multipliers, at the same time keeping in mind low area and moderate power consumption. Over the past few decades, several new architectures of multipliers have been designed and explored. Multipliers based on the Booth's and modified Booth's algorithm is quite popular in modern VLSI design but come along with their own set of disadvantages. In these algorithms, the multiplication process, involves several intermediate operations before arriving at the final[1] answer.

The intermediate stages include several comparisons, additions and subtractions which reduce the speed exponentially with the total number of bits present in the multiplier and the multiplicand. Since speed is our major concern, utilizing such type of architectures is not a feasible[2] approach since it involves several time consuming operations.

II. IMPLEMENTATION

In the accumulate adder the previous MAC output and the present output will added and it consists of Multiplier unit, one adder unit and both will get be combined by an accumulate unit. The major applications of Multiply Accumulate[3] (MAC) unit are microprocessors, logic units and digital signal processors, since it determines the speed of the overall system. The efficient designs by MAC unit are Nonlinear Computation like Discrete Cosine or wavelet Transform (DCT), FFT/IFFT. Since, they are basically executed by insistent application of multiplication and addition, the entire speed and performance can be compute by the speed of the addition and multiplication taking place in the system. Generally the delay, mainly critical delay, happens due to the long multiplication process and the propagation delay is observed because of parallel adders in the addition stage. The main idea of this paper is comparison of area, speed and other parameters of Conventional MAC unit with the Vedic MAC design.

A multiplying function can be carried out in three ways: partial product Generation (PPG), partial product addition (PPA), and final conventional addition. The two bottle necks that should be considered are increasing the speed of MAC are partial product reduction and accumulator block. The 32 bit Mac design by using Vedic multiplier and reversible logic gate can be done in two parts. First, multiplier unit,[4] where a conventional multiplier is replaced by Vedic multiplier using Urdhava Triyagbhayam sutra. Multiplication is the fundamental operation of MAC unit. Power consumption, dissipation, area, speed and latency are the major issues in the multiplier unit. So, to avoid them, we go for fast multipliers in various applications of DSP, networking, etc. There are two major criterions that improve the speed of the MAC units are reducing the partial products and because of that accumulator burden is getting reduced. The basic operational blocks in digital system in which the multiplier determines the critical path and the delay. The (log2N + 1) partial products are produced by 2N-1 cross products of different widths for N*N. The partial products are generated[5] by Urdhava sutra is by Criss Cross Method. The maximum number of bits in partial products will lead to Critical path. The second part of MAC is Reversible logic gate. In modern VLSI, fast switching of signals leads to more power 2015 International Conference on Circuit, Power and Computing Technologies [ICCPCT] dissipation. Loss of every bit of information in the computations that are not reversible is kT*log2 joules of heat energy is generated, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. In recent years, reversible logic functions has emerged and played a vital role in several fields such as Optical, Nano, Cryptography, etc.

2.1 Design of MAC Architecture

The design of MAC architecture consists of 3 sub designs[6].

a) Design of 64 × 64 bit Vedic multiplier.
b) Design of adder using DKG gate reversible logic.
c) Design of accumulator which integrates both multiplier and adder stages

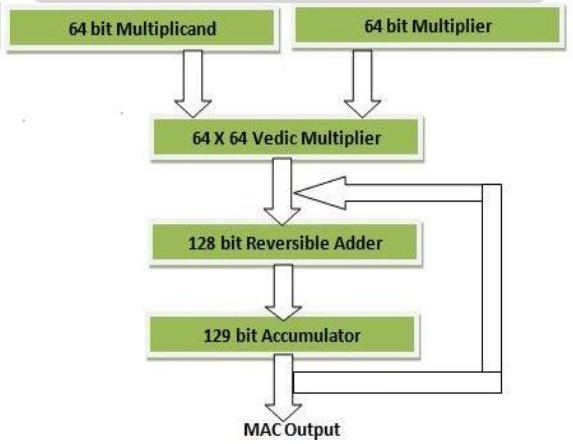

Fig 2.1: Modified MAC Architecture

2.2 64x64 bit Vedic Multiplier

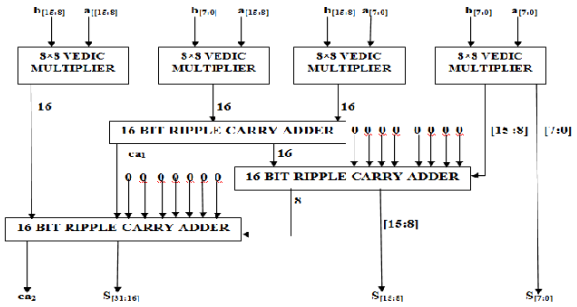

Fig 2.2: 16×16 Vedic multiplier using 8×8 Vedic multiplier

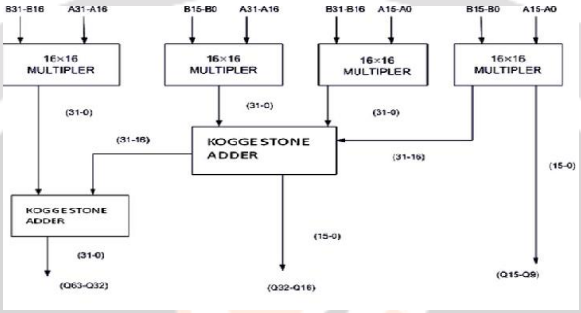

Fig 2.3: 32 × 32 Vedic Multiplier with Kogge Stone Adder

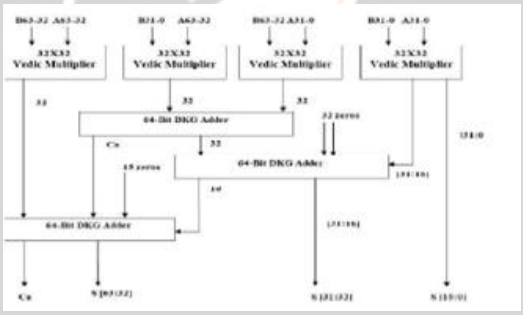

Fig 2.4: 64 × 64 Vedic multiplier using 32 × 32 Vedic Multiplier

Vedic mathematics is an ancient system of mathematics, which was formulated by Sri Jagadguru Swami Bharati Krishna Tirthaji (1884 - 1960). After a research of eight years, he developed sixteen mathematical formulae from Atharvana Veda. The sutras (aphorisms) covered each andevery topic of Mathematics such as Arithmetic, Algebra, Geometry, Trigonometry, differential, integral, etc., The word"Vedic" is derived from the word "Veda" which means thepower house of all knowledge and divine. The proposed Vedicmultiplier is based on the "UrdhavaTriyagbhayam" sutra(algorithm). These Sutras have been traditionally[7] used for themultiplication of two numbers in the decimal number system.In this work, we will utilize similar techniques to solve the binary number system to make the new aphorism, which will be more compatible for the digital systems. It is a general multiplication formula applicable to all cases of multiplication.

2.2.1 DKG Gate

A 4*4 reversible DKG gate that can work [8]singly as a reversible full adder and a reversible full subtractor is shown below. If input A=0, the DKG gate works as a reversible Full adder, and if input A=1 then it works as a

reversible Full subtractor. It has been verified that a reversible full-adder circuit requires at least two or three garbage outputs to make the output combinations unique.

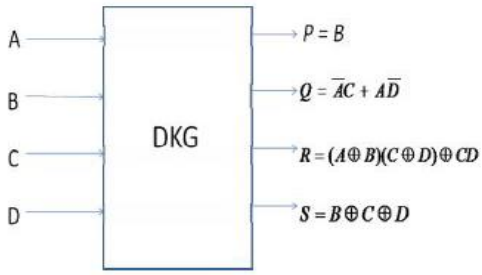

Fig 2.5: DKG gate

III. ACCUMULATOR STAGE

Accumulator has an important role in the DSP applications in various ranges and is a very basic and common method. The register designed in the accumulator is used to add the multiplied numbers. Multiplier, adder and an accumulator are forming the essential foundation for the[9] MAC unit. The conventional MAC unit has a multiplier and multiplicand to do the basic multiplication and some parallel adders to add the partial products generated in the previous step[10]. To get the final multiplication output we add the partial product to these results. Vedic Multiplier has put forward to intensify the action of the MAC Unit. The suggested MAC is compared with the conventional MAC and the results are analyzed. The results obtained using our design had better performance when compared to the pervious MAC designs.

IV. RESULTS & DISCUSSION

The modified multiplier using Vedic multiplier and kogge stone adder is fast and design of MAC done using

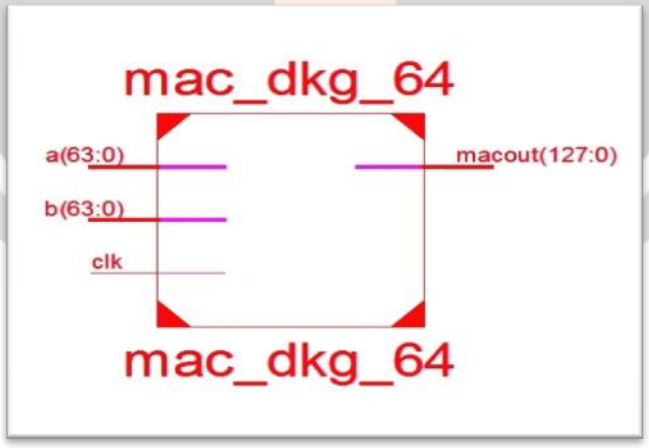

Fig:4.1 RTL Schematic of MAC Unit

Xilinx. This design is implemented in VHDL code using Xilinx. The below figure shows the simulation result of the proposed design. The fig 5 shows the RTL Schematic of MAC unit. The modified 64 bit multiplier using Vedic multiplier and DKG adder is fast and design of MAC done using Xilinx. This design is implemented in Verilog code using Xilinx. The below figure shows the simulation result of the proposed design. The above figure shows the RTL Schematic of MAC unit.

Parameter

The table shows comparison between MAC design unit using different Multipliers. The power consumption in MAC design using booth multiplier will be greater than 4 nW and speed is also high. But it will take more area

Logic utilization	Vedic 8X8 BEC	Vedic 16X16 BEC	Array 8X8	Array 16X16
Delay in ns	23.18	38.82	24.88	61.49

Table 4.1 Comparision between array & vedic multipliers

Parameter	Booth multiplier	Booth recoded Wallace tree multiplier	Vedic multiplier with kogge stone adder and reversible logic (proposed model)	Vedic multiplier and reversible logic (proposed model)
Power (nW)	18398.67	17567.678	15621.12	15546.567
Speed(ns)	6.567	6.436	4.932	5.667
Area (um^2)	2322	2379	1972	2123

Table 4.2: Analysis report of 32-bit MAC using Booth, Wallace tree and Vedic with Reversible logic multiplier.

The figure shows the results of Vedic multiplier with different gates and adders. In which DKG Adders has moderate delay. But it consumes very less power and it can be designed in small area.

The figure shows the results of Vedic multiplier with different gates and adders. In which DKG Stone Adders has moderate delay. But it consumes very less power and it can be designed in small area. The above figure 8 shows that simulation result of DKG adder. It is a 64 bit adder. In this design we used two 64 bit adders.

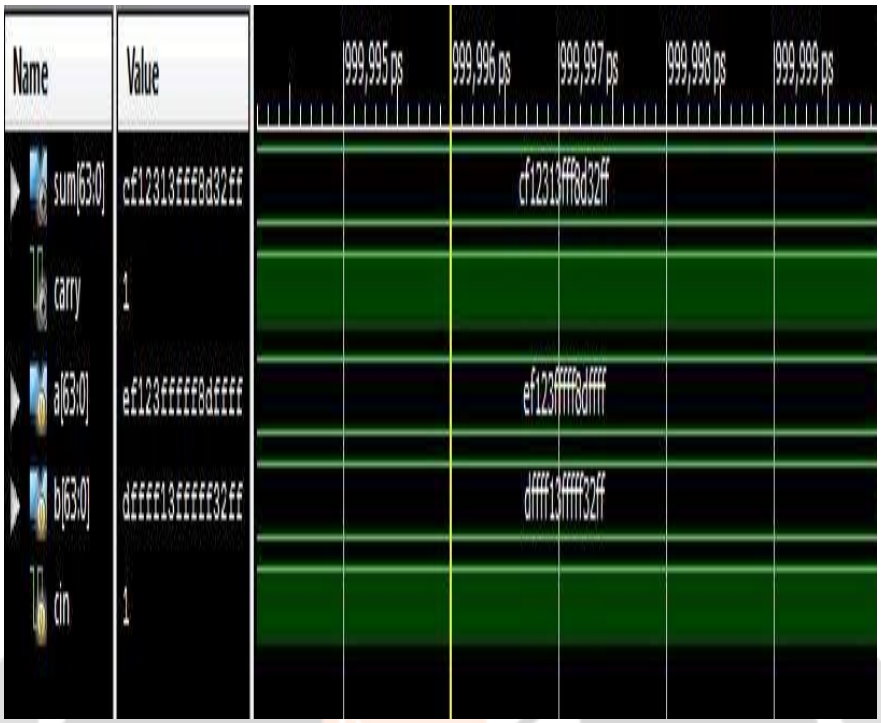

Fig 4.2: Simulation result of Adder

V. CONCLUSION AND FUTURE SCOPE

The results obtained by the proposed design of Vedic multiplier with 64 bits and reversible logic are quite good. The work presented is based on 64 bit MAC unit with Vedic Multipliers. We have designed MAC unit basic building blocks and its performance has been analyzed for all the blocks. Therefore, we can say that the Urdhava Triyagbhayam sutra with 32-bit Multiplier and reversible logic is the best in all aspects like delay, speed, area and complexity as compared to all other architectures which are shown in table 2. Many researchers are reconfiguring the structure of MAC unit, which is the basic block in different designs and aspects especially using reversible logic which develops in recent days. Spectrum Analysis and Correlation linear filtering which are the applications of transform algorithm further add to the field of communication, signal and image processing and instrumentation. By Combining the Vedic and reversible logic will lead to new and efficient achievements in developing various fields of Mathematics, science as well engineering.. Future work is to implement the designs using Synopsys IC Compiler to analyze the post layout results for area and delay. Synopsys Prime Time can be used to analyze the multipliers for their power consumption.

VI. REFERENCES

[1] R.NareshNaik , P.Siva Nagendra Reddy and K. Madan Mohan "Design of Vedic Multiplier for Digital Signal Processing Applications" in International Journal of Engineering Trends and Technology, volume 4 issue 7-2013 ISSN: 2231-5381(IJETT).

[2] VaijyanathKunchigi,LinganagoudaKulkarni, SubhashKulkarni 32-bit MAC unit design using Vedic multiplier International Journal of Scientific and Research Publications, Volume3, Issue 2, February 2013

[3] Ramalatha, M.Dayalan, K D Dharani, P Priya, and S Deoborah, High Speed Energy Efficient ALU design using Vedic multiplication techniques, International Conference on Advances in Computational Tools forEngineering Applications, 2009. ACTEA '09.pp. 600 -3,Jul 15-17, 2009

[4] P.Siva Nagendra Reddy et all.."Design and Implementation of FPGA based 64-bit MAC Unit using VEDIC Multiplier and Reversible Logic Gates" Indian Journal of Science and Technology, Vol 10(3),DOI:10.17485/ijst/2017/v10i3/109413, January 2017.
[5] A. Abdelgawad, MagdyBayoumi ," High Speed and Area- Efficient Multiply Accumulate (MAC) Unit for Digital Signal Processing Applications", IEEE Int. Symp.Circuits Syst. (2007) 3199–3202.
[6] R.Bhaskar, GanapathiHegde, P.R.Vaya," An efficient hardware model for RSA Encryption system using Vedic mathematics",International Conference on Communication Technology and System Design 2011 Procedia Engineering 30 (2012) 124 – 128.
[7] FatemehKashfi, S. Mehdi Fakhraie, Saeed Safari,"Designing an ultra-high-speed multiply-accumulate structure", Microelectronics Journal 39 (2008) 1476– 1484.
[8] D.P.Vasudevan, P.K.Lala, J.Di and J.P.Parkerson,
"Reversiblelogic design with online testability", IEEE Trans. On Instrumentation and Measurement, vol.55., no.2, pp.406-414,April 2006.
[9] RaghavaGaripelly , P.MadhuKiran , A.Santhosh Kumar A Review on Reversible Logic Gates and their Implementation International Journal of Emerging Technology and Advanced Engineering Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 3, Issue 3, March 2013.
[10] PrabirSaha, Arindam Banerjee, Partha Bhattacharyya, AnupDandapat, High Speed ASIC Design of ComplexMultiplier Using Vedic Mathematics, Proceeding of the 2011 IEEE Students' Technology Symposium 14-16 January, 2011, IIT Kharagpur.