THRESHOLD LOGIC'S IMPORTANCE IN BUILDING EFFICIENT AND COMPACT DIGITAL CIRCUITS AND ITS SCOPE IN MODERN TECHNOLOGY

[1]ABHINAV KUMAR, *B.TECH,ECE,SRM INSTITUTE OF SCIENCE AND TECHNOLOGY*
[2]ANTONY FERNANDAS F, *M.TECH,ASSISTANT PROFESSOR,SRM INSTITUTE OF SCIENCE AND TECHNOLOGY*
[3]E.VENU BHAGIRATH, *B.TECH,ECE,SRM INSTITUTE OF SCIENCE AND TECHNOLOGY*
[4]MAHENDAR CHOUDHARY J, *B.TECH,SRM INTITUTE OF SCIENCE AND TECHNOLOGY*

ABSTRACT

Power consumption has been a major parameter in designing of integrated circuits. There have been a number of ways to reduce dynamic and leakage power. Some of them have been logic synthesis, restructuring to reduce switching activity, gate sizing, technology mapping, retiming, voltage scaling. Similarly using dual supply device threshold voltage, adaptive body biasing, clock and power gating, transistor stacking. Thus, the techniques for reducing power at logic and circuit level have been thoroughly explored leaving little opportunity for improvement with this the focus has shifted to higher level of design. Such as power efficient microarchitectures, memory, compilers and operating system, system level control, thread migration among processor cores etc. The suffix 'omics' in the word threshnomics has been added to the names of many fields to denote studies undertaken on a large scale. Threshold science has become so pervasive in everyday life of making decisions. We investigate differences in power between application-specific integrated circuits (ASICs). A variety of factors cause synthesizable designs to consume 3 to 7× more power. When TLGs (called hybrid circuits) are placed and routed using commercial tools it has been observed that there is a significant reductions in power, leakage, and area of the hybrid circuits when compared with the conventional logic circuits, when both are operated at the maximum possible frequency of the conventional design. Threshold functions have also made major contribution in the stream of biomedical engineering in developing a model mocking the behaviour of the neuron where the concept of threshold is used in decision making in the human brain which is further discussed in the paper.

KEYWORDS:-*Threshnomics,Threshold logic, Neuron models, Neuron circuits, Memristors*

1.INTRODUCTION

One of the most important parameters in the design of integrate circuit has been their power dissipation. this was not a major concern previously the major concerns then were area, performance, cost and reliability. It is in recent times that power consumption is also taken into serious considerations in low power VLSI design. Reducing power consumption differ from application too application. In class of micro powered battery operated, portable application such as cellular phase and personal digital assistants such as watches and wireless leakage which is recently being us. The goal is to keep the battery life time high and weight reasonable and the packaging cost low. For high performance in portable come such as laptop and notebooks put our goal is to reducing the power dissipation the electronic portion of the system at a point where is about half of the total power dissipation. Finally, for high performance not the battery operates systems such as set-up computers and multimedia information processing and communication systems in overall goal here is to reduce system cost (cooling, packaging an energy bill) and ensure long-term circuit reliability. One of the major reasons is the growth in personal computing devices and modern wireless communication system in which low power consumption has be an attractive factor also this makes efficient use of renewable energy sources which is the need of the hour. Before we get to know about the various power reduction techniques it is important to know that why CMOS is preferred more than MOS. CMOS design uses both PMOS and NMOS transistor where as

NMOS design uses same as FETs. CMOS can propagate both O an I where as NMOS can propagate only logic (V_{dd}) which is why CMOS is chosen over NMOS for embed system design. CMOS and NMOS have the same function as transistor for both analog and digital circuit a CMOS and NMOS are both inspired by the growth in digital technologies which are now used contractarian integrated circuits. Many digital logic circuit and functions like static RAM and microprocessor are made using CMOS an NMOS. In analog circuit they are used as data convert an image sensor and are also used in trans receptors for many modes of telephone communication. So, it is quite evident that both CMOS and NMOS have similar function as transistors even though most people CMOS Technology for its many advantages. CMOS technology has features like low static power utilization and noise resistance. It conceives energy and does not produce heat. CMOS technology is chosen even though it is costly this is due to its complex composition which makes it hard to be fabricated in the black market. [1]

2.COMPONENTS OF POWER CONSUMPTION

The usual performance target for designer is to reduce both total power when a circuit is active and standby power. Active power includes both dynamic and static power consumption, when the logic evaluates or the clock transitions and current leakage when it is not switched. In standby there is no computation logic to prevent switching the clock must be another factor that consumes power during standby. The clock tree and registers control and data path logic and memory are one of the major sources of power consumption. The reduction of power consumption among these depends on the application and design. Clock tree and register consume 18% to 36% of the total power in most typical embedded processing and microprocessor. In case of custom core for discrete cosine transformer and increase discrete transform, contribution to total power range between 5% to 10 from control logic 40% from clock tree and clock buffer and 40% from data path logic [3]. Memory can account for a suitable position of power consumption. It is observed the storage cashes assume 48% power.

2.1 DYNAMIC POWER

Dynamic power is due to switching capacitance and short circuit power when there is a current path from supply to ground. The switching power can be derived from $\alpha f C V_{dd}^2$ where α is the switching activity per clock, f is the clock frequency, C is the capacitance discharge and V_{dd} is the voltage switching. The switching activity increase through glitches, which cause 15% to 20% of the activity in complementary static CMOS logic [3]. About 10% of the total dynamic power is contributes to short circuit, which increase as V_{dd} increases and decrease as V_{th} decreases. Short circuit power can be reduced by matching input and output rise and full times [4]. Reducing the capacitance by downsizing the gates and reducing wire is required as dynamic power depends quadratically on V_{dd} and methods for reducing V_{dd}.

2.2 LEAKAGE POWER

Leakage power account for 10% to 80% of the total power when a chip is active and leakage power contributes a large portion of average power consumption. In case of low performance application and this is most observed as a chip has long idle modes without bring fully off. It has 8% to 21% of the total power consumption in combinational logic. However, the possible V_{dd} and V_{th} values depend on the particular process technology and standard cell libraries available. In the case of complementary static CMOS logic in bulk CMOS it is due to sub threshold and gate leakage is affected exponentially with V_{th} and temperature, as V_{th} decrease and temperature increases subthreshold leakage increase exponentially. This can be strongly dependent on transistor channel length in short channel devices reduction in gate aside thickness has resulted in exponential increase in gate leakage. There has be significant increase in leakage in deep submission process technologies. [2]

3. THRESHOLD LOGIC AND THRESHOLD GATES

Most of the logic circuit are designed using conventional gates like AND, OR, NOT and some of the function blocks like the multiplexer and the de-multiplexer. Beside these techniques there has been use of threshold logic which is an interesting alternative in logic design. It helps in much simple circuit realizations of many functions. Threshold logic is now considered very important in designing efficient compact devices in modern time. Although threshold logic is not a new concept, technologies available for implementing are discovered recently which widened the scope for it. It is discovered that threshold logic can be used in neuromorphic computing. Neuromorphic computing is a concept developed by Carver Mead, in the late 1980s, describing the use of very-large-scale integration (VLSI) systems to mimic neuro-biological architectures present in the nervous system.[9]

Neuron models are found to work in a way very similar to the threshold gate. Threshold logic circuits can be implemented using threshold logic gates.

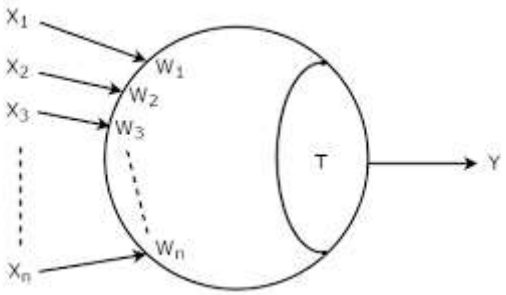


Fig 3.1: schematic diagram of threshold gate

Here x1, x2…. xn are inputs. Unlike conventional gates threshold gates has weights assigned to its input w1, w2, w3…. wn and 'T' which is called threshold and Y is the output. The Inputs x1, x2…. xn are binary inputs, the output Y is also a binary output but the weights and threshold are not binary numbers. These are real numbers.

The output (Y) depends on sum of product of weights with their input as shown

$$\sum_{i=1}^{n} \text{w1xi}$$

Y=1, if and only if $w_1x_1 + w_2x_2 + \ldots\ldots + w_nx_n \geq T$

Y=0, if and only if $w_1x_1 + w_2x_2 + \ldots\ldots + w_nx_n < T$

Let us take a four variable function and implement it using conventional gates and threshold gates to know the difference.

Example: $Y=f(x_1, x_2, x_3) = \sum (1,2,3,6,7)$

$= x_1'x_3 + x_2$

Using conventional gate, we would require three gates a NAND gate, a NOT gate and an OR gate.

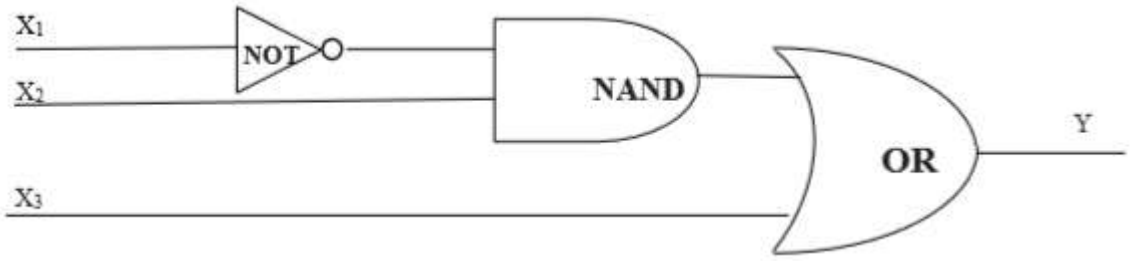


Fig3.2: logic diagram of function if realised by conventional gate

Whereas using threshold logic we can implement this function using a single threshold element.

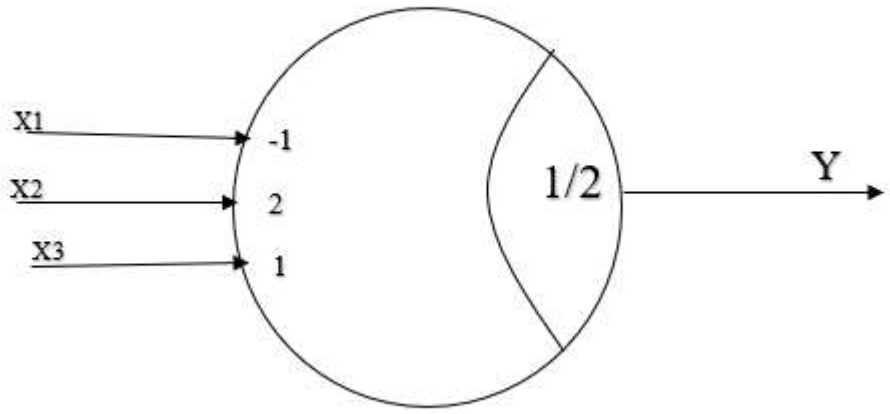


Fig 3.3: schematic of function realised by threshold gate.

INPUT VALUES			**WIEGHTED SUM VALUES**	**OUTPUT**
X_1	**X_2**	**X_3**	**$-2X_1 + X_2 + 3X_3$**	**Y**
0	0	0	0	0
0	0	1	1	1
0	1	0	2	1
0	1	1	3	1
1	0	0	-1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	2	1

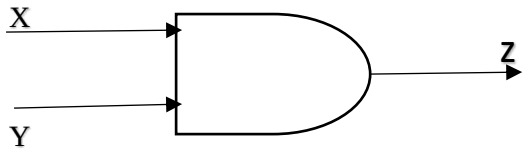
Table 3.1: Output of function when realised by threshold gate

For all the possible inputs of x_1, x_2, x_3 the truth table shows the outputs. For the inputs 1,1,0 at x_1, x_2 and x_3 the weighted sum is 1. 1 is now compared to the threshold which is T=1/2. 1 is greater than the threshold so the output gets executed.

$$(1)(-1) + (1)(2) + (0)(1) = 1$$

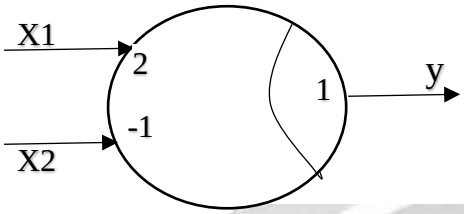
3.1 ADVANTAGES OF THRESHOLD GATES

A threshold gate is functionally complete similar to the universal gates NAND and NOR which can be used to implement any function. A threshold gate can also be used to implement any kind pof function. Threshold gate can generalize a larger clan of functions which in conventional gate will require a lot of several of them instead instead they can be realized using a single threshold gate. To understand how threshold gates are functionally complete let us realize some of the conventional gates using threshold gates.



INPUTS		Output
X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

Fig 3.1.1 : NAND gate and its truth table



X1	X2	-X1 -X2	Y
0	0	0	1
0	1	-1	1
1	0	-1	1
1	1	-2	0

Fig 3.1.2: schematic diagram of NAND gate realised by threshold gate and corresponding

Although we have seen that the threshold gates are functionally complete. A single threshold gate cannot realize all the functions. Let us consider this example

$$f(x_1, x_2, x_3, x_4) = x_1 x_2 + x_3 x_4$$

In order to get the output, we will have to consider the combinations whose output is one. Here for the product terms x_1, x_2, x_3, x_4 the output must be 1 for x_1, x_2, x'_3, x'_4

$$w_1 + w_2 \geq T$$

$$w_3 + w_4 \geq T$$

For both the minterms the output to be one of the conditions given

$$w_1 + w_2 + w_3 + w_4 \geq 2T$$

Let us consider the opposite where the output will be zero

As seen before output will be one of the either x_1x_2 is n x_3x_4 are 1, similarly output will be zero if either one of x_1x_2 or one of x_3x_4 are zero.

For, $x'_1x_2x'_3x_4$ $x_1x'_2x_3x'_4$

this gives us the condition where the weighted sum is less than the threshold

$$w_2 + w_3 < T$$

$$w_1 + w_3 < T$$

$$w_1 + w_2 + w_3 + w_4 < 2T$$

We could not find the condition where the sum of weights is greater than or equal to 2T and also it must be less than 2T.

3.2 THRESHOLD LOGIC DESIGN

For a given switching functions f (X1, X2....Xn) to determine whether it can be realized by a single threshold element, if so, to find the appropriate weight and threshold such function is called a threshold function.

Let us understand the threshold logic; the truth table is constructed from which inequality constraints one obtained from each row. Since we have 2n rows we will be having 2n constraints by solving them we can determine the weight.

Example: f 9(X_1, X_2, X_3) =X_1'X_2'+X_1'X_3

D	X_1	X_2	X_3	f	Inequality
0	0	0	0	1	$0 \geq T$
1	0	0	1	1	$W_3 \geq T$
2	0	1	0	0	$W_2 < T$
3	0	1	1	1	$W_2+W_3 \geq T$
4	1	0	0	0	$W_1 < T$
5	1	0	1	0	$W_1+W_3 < T$
6	1	1	0	0	$W_1+W_2 < T$
7	1	1	1	0	$W_1+W_2+W_3 < T$

Table 3.2.1: Inequality constraints for all possible inputs.

For the given function we have obtained truth table X_1 X_2 X_3 and the output f. In order to build a threshold gate the input

Will be X_1, X_2, X_3 and the weight will be W_1 W_2 W_3 and the threshold will be T and output is f.

Now for the input O, O, O at X_1, X_2, X_3 the output is 1. since the output is

X_1	X_2	X_3	f	T
0	0	0	1	$0 \geq T$

The weighted sum must be greater than or equal to zero. Similarly, for the

The input 001n at X_1, X_2, X_3 the output is 1, hence $W_3 > T$ OR $W =_3 = T$. Since the output is 1.

X_1	X_2	X_3	f	inequality
0	0	1	1	$W_3 \geq T$

X_1	X_2	X_3	f	inequality
0	1	1	1	$W_2+W_3 \geq T$

When the output is zero i.e. the input is 010 at X_1, X_2, X_3 only X_2 is 1. hence $W_2 < T$.

X_1	X_2	X_3	f	inequality
0	1	0	0	$W_2 < T$

For the input 101 at X1, X2, X3 the output is zero, hence, W1+W2<T

X_1	X_2	X_3	f	inequality
1	0	1	0	$W_1+W_3 < T$

Similarly taking inequalities for all the output and inputs we eight inequality constraints from the truth table. Now by solving for W_1, W_2 and W_3 we obtain the weights

For the first input zero. $D_=$ 0 we come to the conclusion T is negative for D=2, W<T which leads us to conclusion T is negative for D=4 ,W2<T hence W1must also be negative. From D=3 and D=5 we observe that W3 cancels out in the case where W1 W2 and T are negative values, which can be more clearly understood for D=1, $_{W3}$<T or W3=T. All the observations lead us to the conclusion

$$W_3 > T \text{ or } W = T > W_3 > W_1$$

Now we must take arbitrary values which satisfies the condition and T must be negative. One of the many possibilities is

W_1= -2 W_3= 1`

W_2= -1 T= -0.5

3.3 PROPERTIES OF THRESHOLD GATES

A Threshold gate gets characterized by the weight at the input and the threshold. The weight and the threshold taken together one called weight threshold vector (V)

$$V= \{W_1, W_2 .....Wn; T\}$$

For a function f $\{X_1 X_2 ...Xn\}$ realized by weight threshold vector (V)

$$V1= \{W_1, W_2.....Wj....Wn; T\}$$

If input Fj is complimented (X'j) then the function can be realized by negation. The value of the weight and by taking T- Wj

$$f (X_1,X_2 ...X'j.....Xn)$$

$$V2= \{W_1, W_2.....Wj...Wn, T, -Wj)$$

For a f (X_1, X_2 ...X, j..... Xn) is realized by a single threshold element with weight threshold vector $V_1 = \{W_1 W_2$ .... Wn; T} then the compliment is realized by negating the weights and threshold

$V_2= \{-W_1, -W_2, ...-Wn; -T\}$

Proof for $\sum_{i=1}^{n} WiXi > T$ WHERE f=1

$\sum_{i=1}^{n} WiXi > T$ WHERE f=0

Multiplying both sides by -1:

$\sum_{i=1}^{n} WiXi < -T$ WHENEVER f=1 or f'=0

$\sum_{i=1}^{n} -WiXi > -T$ WHENEVER f=0 or f'=1

By assigning negation observe that it is equivalent to the complimented function.

There are many properties to threshold function which have resulted in wide range use of threshold logic and increased its scope of work. [7]

4. THRSHOLD LOGIC GATES TO REDUCE POWER

A number of methods one present in order to reduce dynamic and leakage power. Many of these designs are incorporated into modern design and tools .as technology states to become compact more efficient the focus shifted to higher levels of design which are power efficient, have greater memory and perform complex operations too. In digital COMS circuits and application specifies integrated circuit (ASIC), in which every node computer a Boolean function of inputs to its outputs. Another subset of unate Boolean function called threshold functions which showed the path for further improvements in designing efficient and compact circuits which would perform on the same level as the other device.

This is achieved by an automated methodology in the design on digital ASIC by a combination of conventional logic gates and threshold logic flops. The circuit will be capable of performing complex functional blocks

	Standard Deviation of Dynamic Power (mW)		
Circuit	Conventional	Hybrid	% Reduction
Multiplier	2.9289	1.7248	41
Filter	8.6197	4.8469	44
FPU	4.5985	3.2108	30
MIPS	6.9563	5.5251	35
AES	3.079	2.0606	33

Table 4.1: variation in the dynamic power

5. THRESHOLD LOGIC ON NEUROMORPHIC COMPUTER

The human brain contains millions of neurons which result in human intelligence and in understanding their decision making. It is due to the behaviour of neurons and its networks. These decision-making unit are arranging in a hierarchy at levels of functional and structural levels, their actions are found to be similar that of threshold processing, since these decisions are enables by threshold in any biological intelligence their scale processing one referred with the terminology of threshnomics.

This idea was exposed by McColloch and Pits. They both together first introduced the first mathematical model of a neuron; the threshold logic gate which is now seen in everyday science.

Any combination signal can be converted into a digital signal using a threshold. The threshold values result in a set of binary signal patterns.

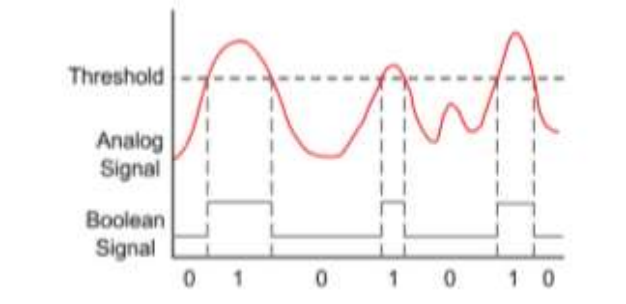


Fig 5.1: Binary Thresholding

By reversing engineering this aspect as an analogue signal reflected as discrete signal is confines within the measurement resolutions and uncertainty limits. Reverse engineering has results in indication that any decision that seems analogue in nature can be comprised of a series of binary decisions. This is the primary ideology behind the primary architecture to development of intelligence systems. [9]

6.CONCLUSION

A wide range of applications exists that use thresholds in different forms. The applicability of a threshold value is tightly coupled to several factors such as the nature of the problem, practical aspects of the system under consideration, and level of understanding about the decision space it's important to note that threshold selection is an emerging science that can lead to better automation and decision systems. The threshold can be applied different decision levels, such as local and global. To conclude, although the threshold operations itself seems trivial, the applicability and identification of optimal threshold values are not a trivial task. The broad range of science surrounds around threshold and it's of paramount interest in several applications

7.ACKNOWLEDGEMENT

This research was supported by SRM INSTITUTE OF SCIENCE AND TECHNOLOGY, Ramapuram, Chennai. We are thank full to our guide Mr. Antony Fernandas F (M. Tech) who provided us with expertise that greatly assisted the research.

REFERENCES

1.logic synthesis for low power, Luca Benini,DEIS - Universita di Bologna-lbenini@deis.unibo.it,Giovanni De Micheli,CSL - Stanford University,nanni@galileo.stanford.edu.
2. overview of the factors affecting the power consumption- David Chinnery, Kurt Keutzer Department of Electrical Engineering and Computer Sciences University of California at Berkeley Berkeley, CA 94720, USA.
3. Singh, D., et al., "Power Conscious CAD Tools and Methodologies: a Perspective," in Proceedings of the IEEE, vol. 83, no. 4, April 1995.
4. Veendrick, H., "Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits," Journal of Solid-State Circuits, vol. SC-19, August 1984.
5. Xanthopoulos, T., and Chandrakasan, A., "A Low-Power DCT Core Using Adaptive Bitwidth and Arithmetic Activity Exploiting Signal Correlations and Quantization," Journal of. Solid State Circuits, vol. 35, no. 5, May 2000.
6. Xanthopoulos, T., and Chandrakasan, A., "A Low-Power IDCT Macrocell for MPEG-2 MP@ML Exploiting Data Distribution Properties for Minimal Activity," Journal of Solid State Circuits, vol. 34, May 1999
7. Lecture 30: Threshold Logic and Threshold Gates- https://youtu.be/Hv4mbqm9Iwk- IIT Kharagpur July 2018-Published on 28 Aug 2018.
8. Reducing Power, Leakage, and Area of Standard-Cell ASICs Using Threshold Logic Flip-Flops Niranjan Kulkarni, Member, IEEE, Jinghua Yang, Member, IEEE, Jae-Sun Seo, Member, IEEE, and Sarma Vrudhula, Fellow, IEEE.